

**Argonne National Laboratory
High Energy Physics Division
Electronics Support Group**

2007 Department of Energy Review

*Gary Drake
Group Leader*

Apr. 26, 2007



Group Personnel

Gary Drake	<i>Group Leader, EE</i>	Bill Haberichter	<i>Engineering Specialist</i>
John Dawson	<i>Senior EE (part-time)</i>	Tim Cundiff	<i>Engineering Assistant</i>
John Anderson	<i>Elec. Eng.</i>	Larry Bryant	<i>Engineering Asst. (temp)</i>
Patrick De Lurgio	<i>Elec. Eng.</i>	Todd Hayden	<i>PCB Layout</i>
Andrew Kreps	<i>Elec. Eng (Software)</i>	Jim Bulka	<i>Instrument Repair</i>
Jim Schlereth	<i>Computer Scientist</i>	Joe Prati	<i>Instrument Repair (p.t.)</i>
		Carolyn Adams	<i>Technician</i>

Total Staff:

- **3.5 Hardware Engineers**
- **2 Software/Computer Sci.**
- **3 Technical Assistants**
- **1 CAD Layout Person (EA)**
- **1.5 Instrument Repair (EA)**
- **1 Technician (Assembly)**

- » **13 People Total (12 FTEs)**
 - ~ 7.5 FTEs Support HEP
 - ~ 4.5 FTEs Support Other Basic Sciences (PHY, CHEM, Mat. Sci., BIO, IPNS, NE, APS (CAD))
- » **Strengthens HEP Program**
- » **Provides Crucial Electronics Support for ANL Science & Research**

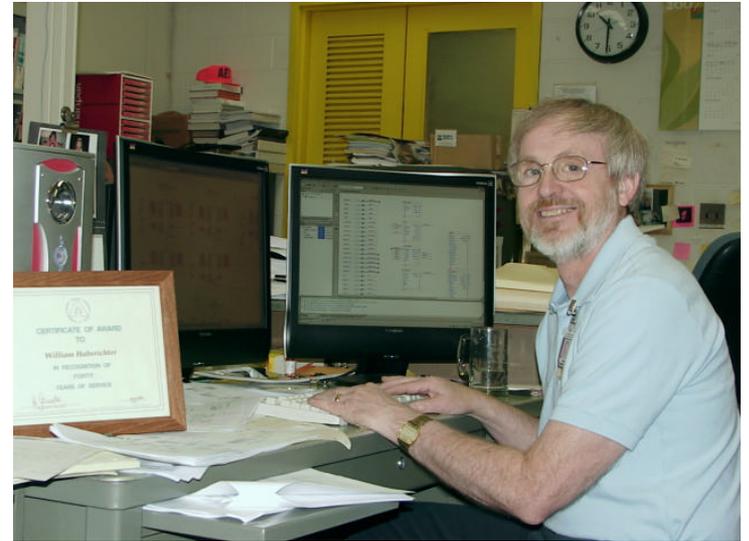
» **Well Rounded Group with High Levels of Expertise, Capable of Taking on a Wide Range of Projects**

Group Specialties & Expertise

A. Design of High Speed Data Processors

- **Types of Projects:**

- ◆ Data Acquisition
- ◆ Trigger Processors
- ◆ Computer Interfaces



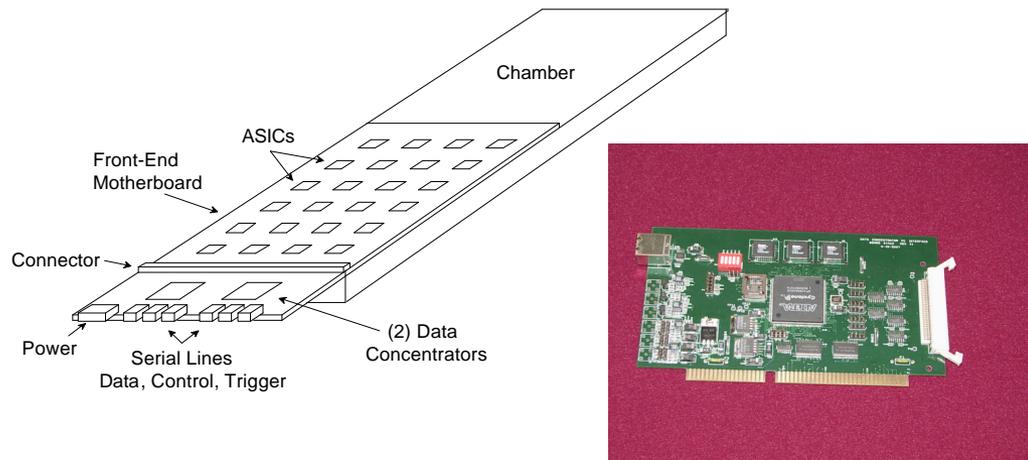
- **Implementation Techniques:**

- ◆ Printed Circuit Board Design (Schematic Capture, PCB Layout)
- ◆ Design of Programmable Logic Devices (PLD)
- ◆ Design of Field Programmable Gate Arrays (FPGA)
- ◆ Designs Using Surface Mount Technology
- ◆ Designs using Ball Grid Arrays (BGA)

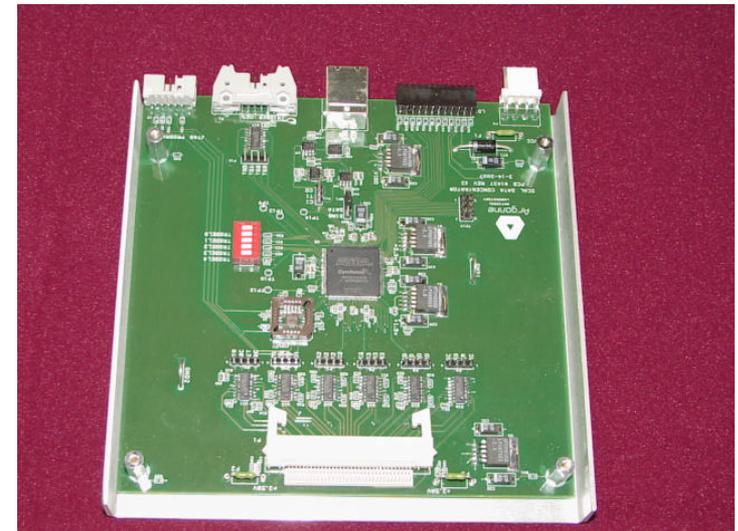
Group Specialties & Expertise

A. Design of High-Speed Data Processors (Cont.)

- **Current Project: Data Concentrator for DCAL (ILC HCAL)**
 - ◆ Receives Data from DCAL ASICs mounted on Chamber
 - ◆ Concatenates Serial Data Streams from 12 Chips into One Serial Output Stream
 - ◆ Prototype Development for “Vertical Slice” in Progress



PC Interface for Testing



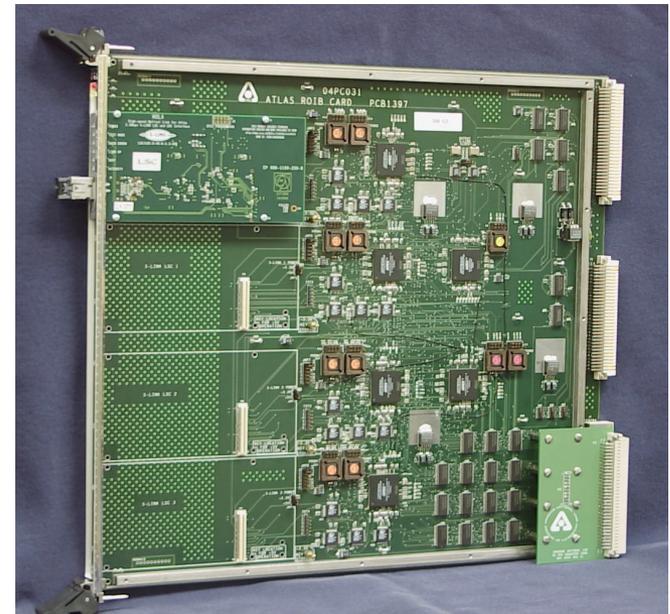
Data Concentrator

Group Specialties & Expertise

A. Design of High Speed Data Processors (Cont.)

- **Recent Project: *Region of Interest Builder***
for Level 2 Trigger System in ATLAS Exp. at CERN
 - » **Key Project for ATLAS Trigger-DAQ**

- ◆ Receives Information from Level 1 Trigger, Forms a “Record,” and Passes it to the Trig. Supervisor for Processing
- ◆ Uses Altera 20K200E
200K Gates/Chip
- ◆ 700 MB/Sec Data Throughput (Max)
- ◆ 100 KHz Output Trigger Rate (Max)
- ◆ Final Version : **18 Layer Board**



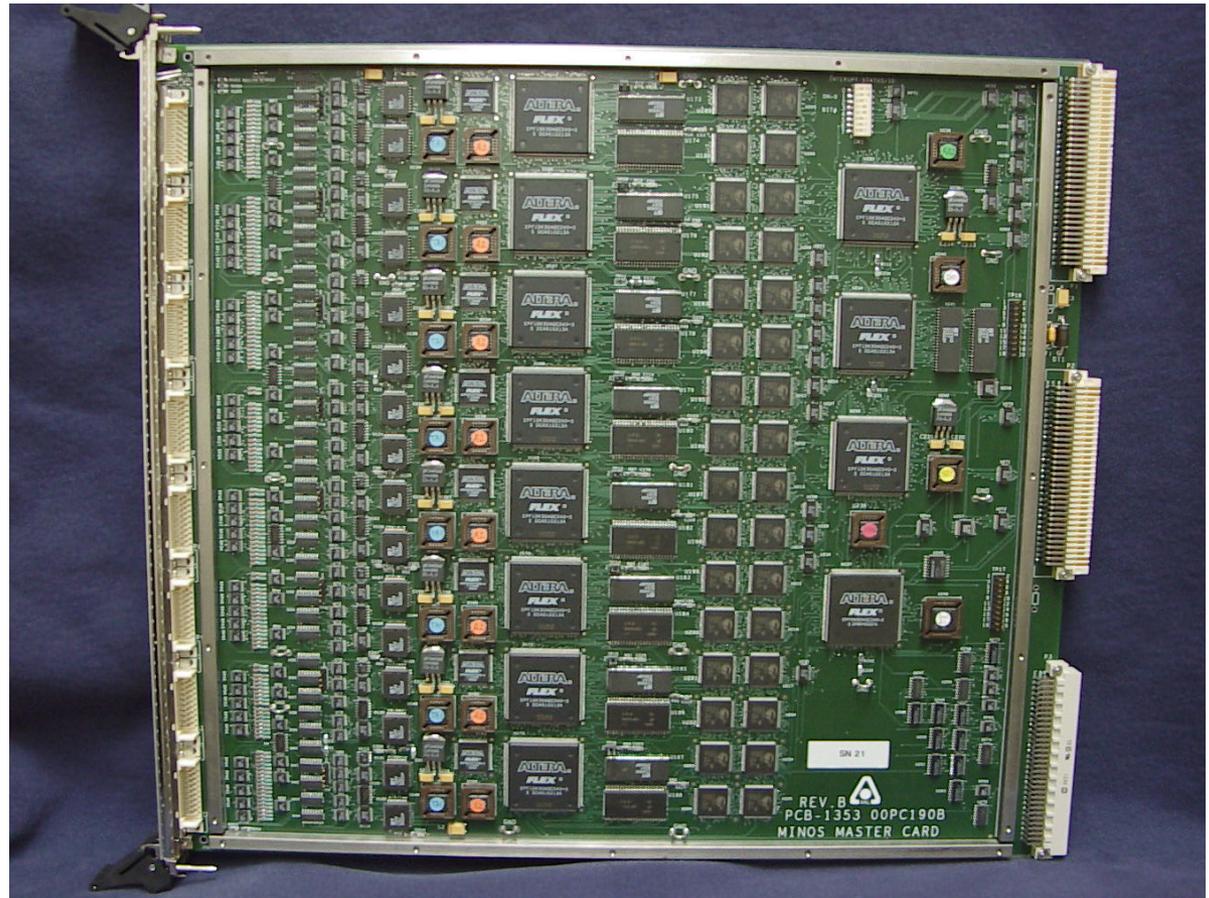
» **Extensive Use of High-Density Programmable Logic**

Group Specialties & Expertise

■ Design of High-Speed Data Processors (Cont.)

- Other Recent Projects:

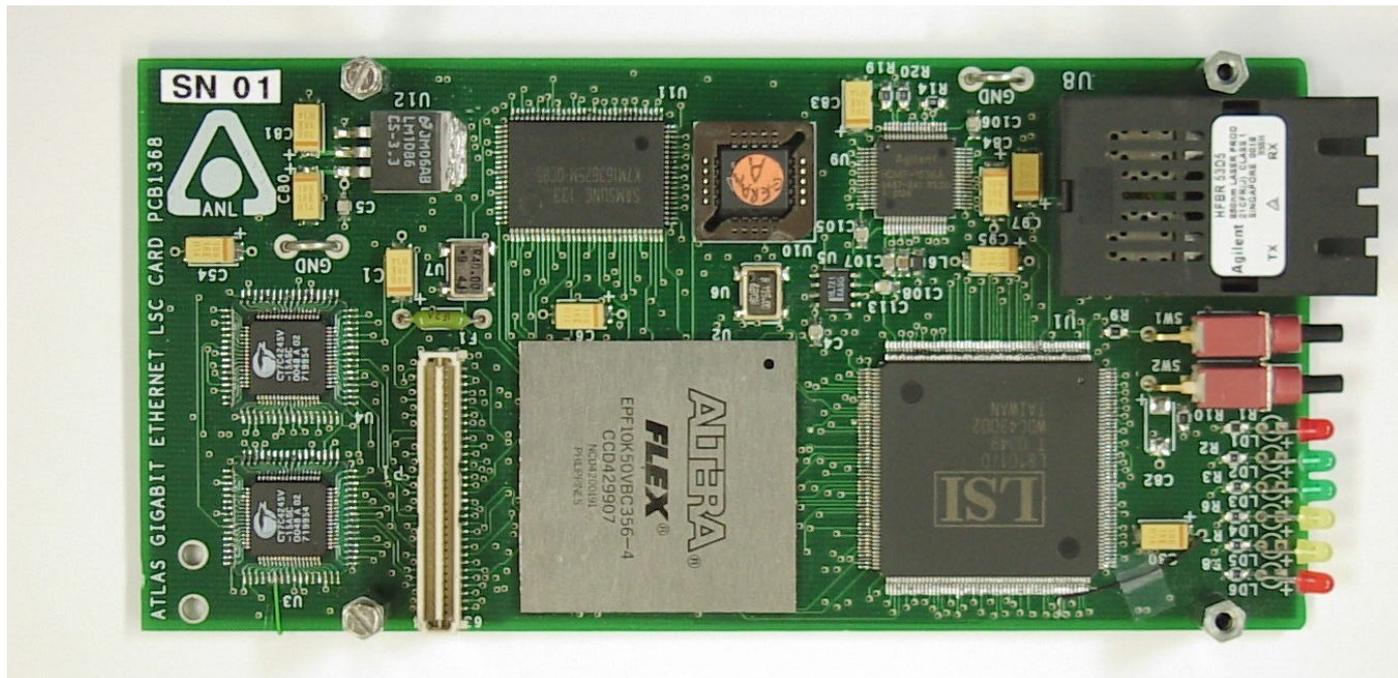
**MINOS @ FNAL
MASTER Module
Data Acquisition
(Near Detector)
100 Modules**



Group Specialties & Expertise

A. Design of High-Speed Data Processors (Cont.)

- Other Recent Projects:



**ATLAS @ CERN
Gigabit Ethernet
Trigger / DAQ**

Group Specialties & Expertise

B. Front End Design

- **Types of Projects:**
 - ◆ Charge Amplifiers
 - ◆ Preamplifiers
 - ◆ Digitizers
 - ◆ Discriminators
 - ◆ Implementation of Custom Circuits (ASICs)
 - ◆ Noise Measurement, Analysis, & Abatement
 - ◆ HV Power Supply Design
- **Implementation Techniques:**
 - ◆ Printed Circuit Board Design
 - ◆ Surface Mount Technology
 - ◆ Custom Circuit Design (Collaborations → FNAL, NU, UC)



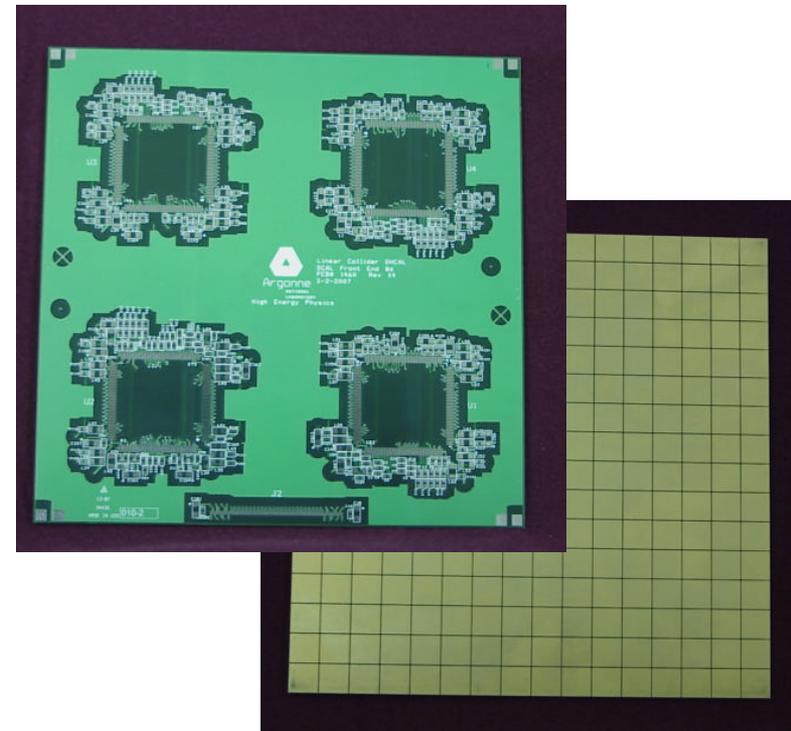
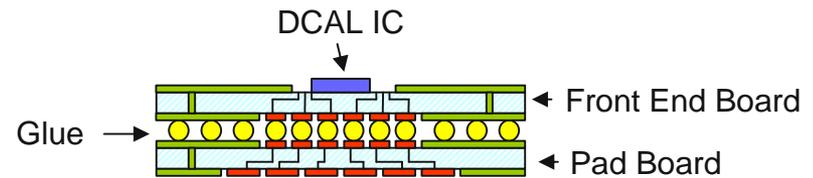
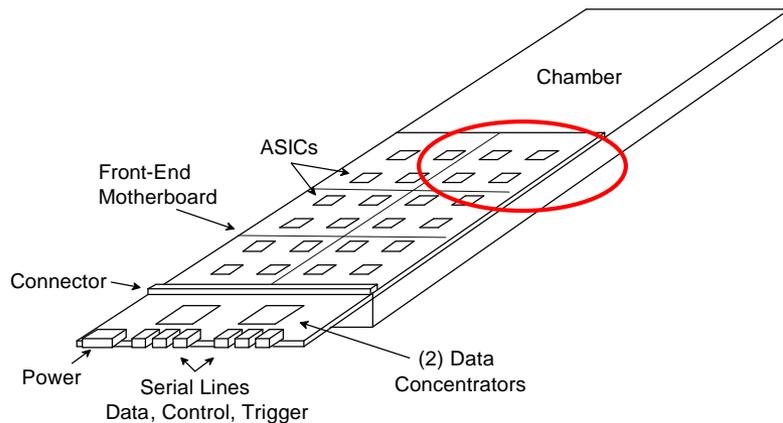
Group Specialties & Expertise

B. Front End Electronics Design (Cont.)

• Most Recent Project: DCAL Front-End Board (ILC HCAL)

- ◆ Hosts 4 DCAL ASICs
- ◆ FEB Mounts on Chamber (RPCs)
- ◆ Internal Layers have Power, Ground, Digital Signals, AND Low-Level Chamber Signals
- ◆ 8 Layers, 3 Layers of Buried Vias
- ◆ Most Complex Board we have ever Built!

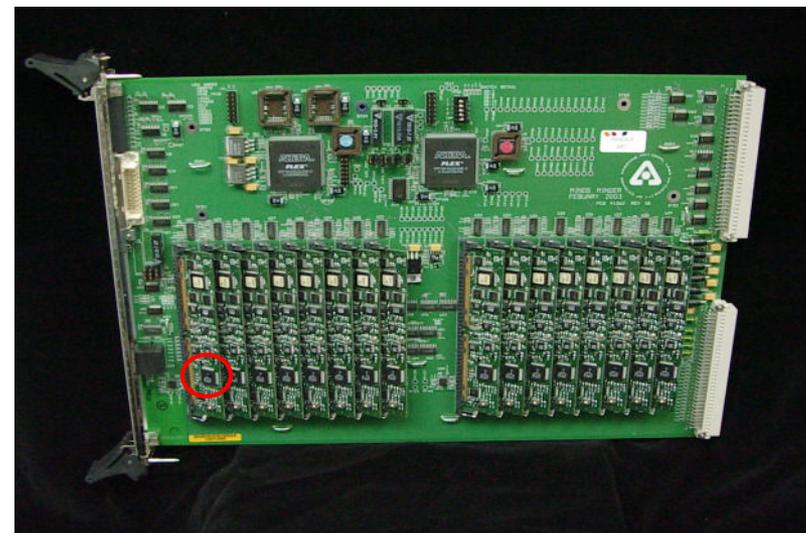
⇒ Digital Lines Next to Charge Signals



Group Specialties & Expertise

B. Front End Electronics Design (Cont.)

- **Recent Project: *MINDER Module* for Data Acquisition in MINOS Exp. at Fermilab (Near Det.)**
 - ◆ Motherboard for Front End Electronics Channels
 - ◆ Host to 16 Daughter Boards Containing Custom Integrated Circuits (FNAL)
 - ◆ 6U x 340mm VME Board
 - ◆ 53 MHz Clock & Digitization
 - ◆ 700 Boards for Production

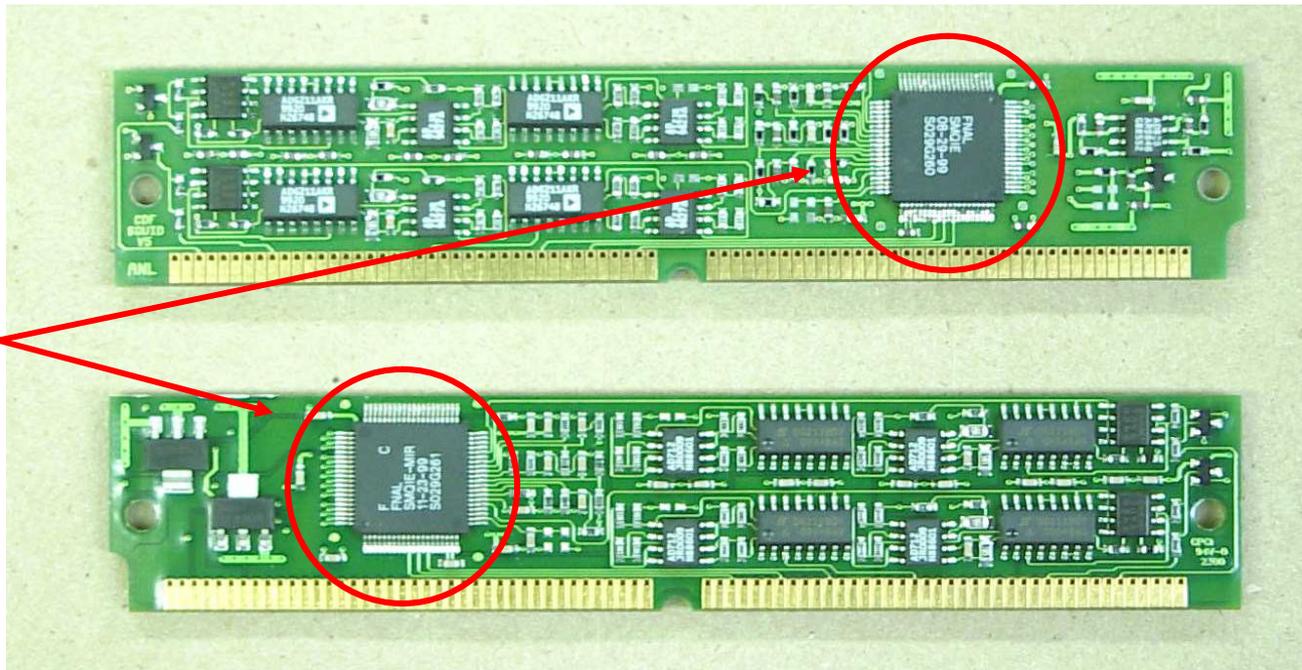


» **High Density Programmable Logic,
Mixed Analog/Digital Processing, Low Noise**

Group Specialties & Expertise

B. Front End Electronics Design (Cont.)

- Other Recent Projects:



CDF @ FNAL
SQUID Module
Front End Electronics
Shower Max

Group Specialties & Expertise

C. System Design

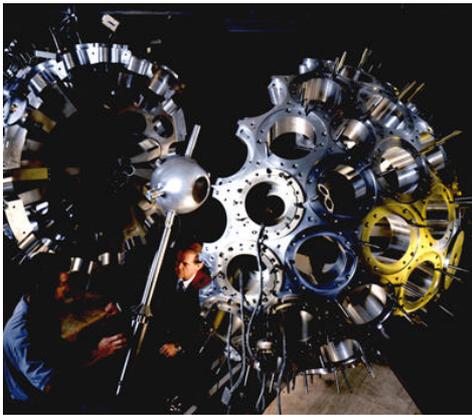
- **Types of Projects:**
 - ◆ **Trigger Systems (HEP: *CDF, ATLAS, ZEUS*)**
 - ◆ **Front End Data Acquisition Systems (HEP: *CDF, MINOS, Linear Collider, ZEUS*)**
 - » **Often Assume Leading Roles in System Design & Project Engineering**
 - » **Form Collaborations & Working Relationships with Other Institutions**
 - » **We Provide Support for Our Electronics (and Often Electronics Built for Others)**
For the Life of the Experiment



Group Specialties & Expertise

D. Detector Design

- **Types of Projects:**
 - ◆ High Resolution CCD Imaging Detectors
 - ◆ Large Area X-Ray Detectors
 - ◆ Ge and BGO Detectors for Gamma Ray Tracking (Gammasphere, Neutrino Detectors)
 - ◆ Silicon Detectors (Time-Resolved Small-Angle Scattering)



**Gammasphere
(Physics)**



**Anger Camera
(IPNS)**

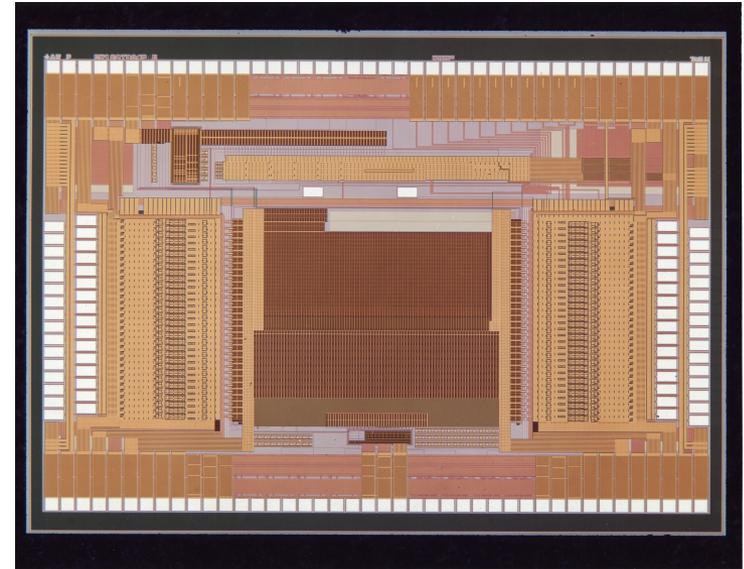


**TRSAX
(Chemistry)**

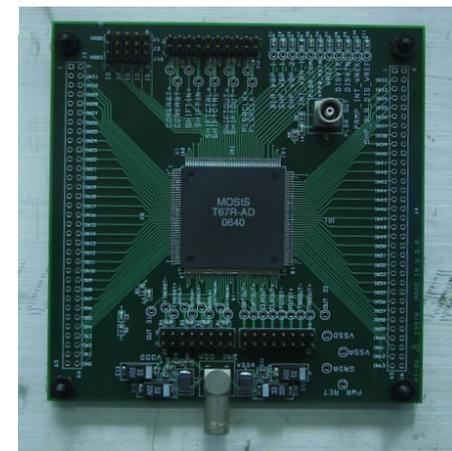
Group Specialties & Expertise

E. Detector R&D

- **Current Projects:**
 - ◆ **Electronics for Linear Collider Digital HCAL Prototype Detector**
 - 400,000 Channels, to Operate in Testbeams
 - DCAL Custom Chip
- Developed with Fermilab*
- ANL: Testing ASIC, Designing & Building Readout System



DCAL Chip – Version 1 (Courtesy Fermilab)

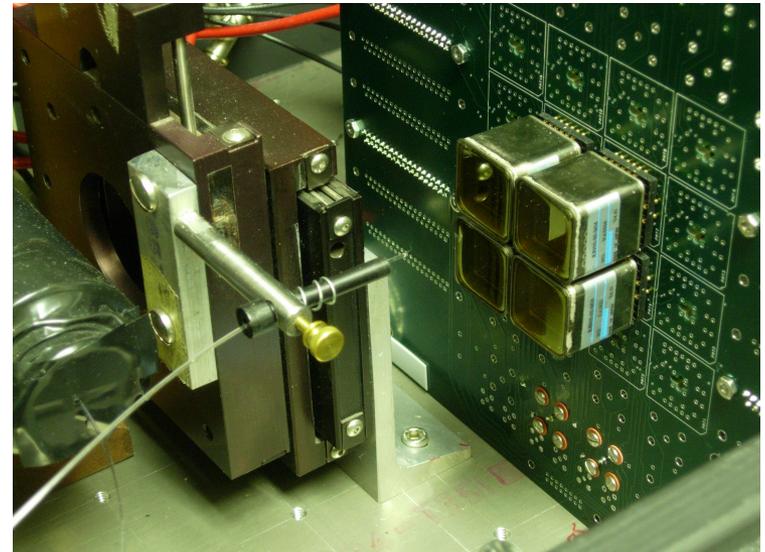


DCAL Test Board

Group Specialties & Expertise

E. Detector R&D (Cont.)

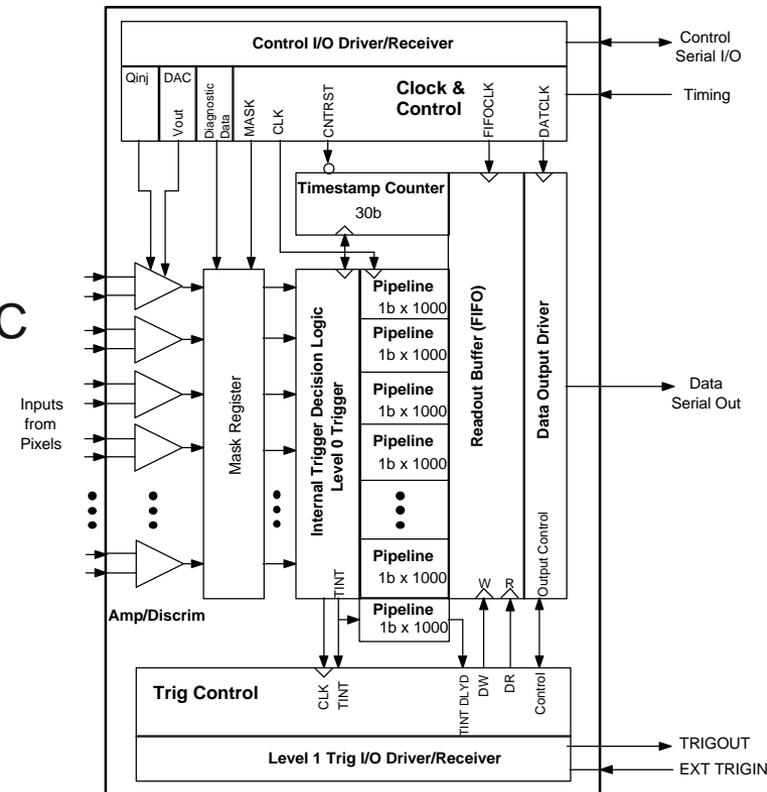
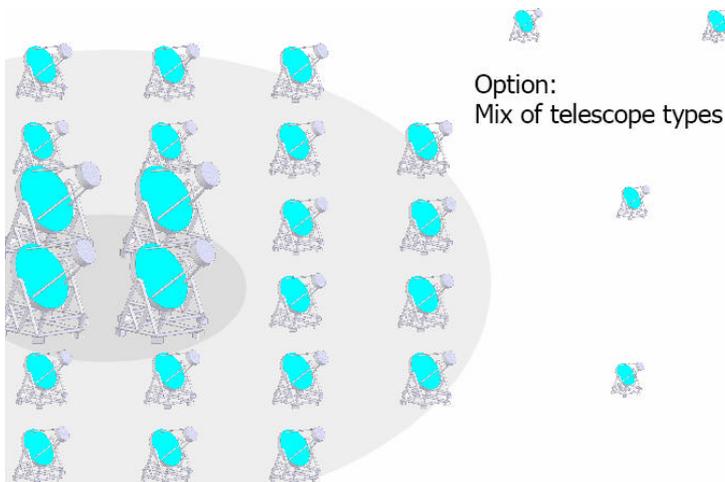
- **Current Projects (Cont.):**
 - ◆ **Telescope Camera R&D for Particle-Astrophysics**
 - Supporting R&D on using Multi-Anode Photomultiplier Tubes
 - *Data Acquisition System for Lab Measurements*
 - *Readout System for TrICE*
 - ◆ **Electronics for Future Telescope Arrays**
 - Developing Front-End Electronics and Trigger for Next-Generation Telescope Arrays



Group Specialties & Expertise

E. Detector R&D (Cont.)

- **Current Projects (Cont.):**
 - ◆ **Electronics for Future Telescope Arrays (Cont.)**
 - DTEL – 1 GHz Photon-Counting ASIC
 - *Collaboration With UC*
 - *Chip Design with Northwestern (Yehea Ismail)*



⇒ This is Leading Edge,
Never Been Done Before

Current Projects

Current Projects:

- ◆ **Electronics & Readout for Linear Collider Detector R&D, RPCs for HCAL, Test Beam Studies**
 - ⇒ **Building 2500 Ch Vertical Slice**
 - ⇒ **Next: 400,000 Ch “Cubic Meter”**
- ◆ **Electronics/Detector R&D for Future Telescopes**
 - ⇒ **Array Trigger (Collaboration with Iowa State University)**
 - ⇒ **GHz Photon-Counting ASIC (Collaboration with Univ. Chicago, Chip Developed with Northwestern Univ.)**
- ◆ **Other Detector R&D (Mentioned Yesterday):**
 - ⇒ **SiPM R&D**
 - ⇒ **Picosecond Timing**
- ◆ **Support for ATLAS TileCAL Power Supplies**
- ◆ **Long-Term Support for MINOS ND Electronics**
- ◆ **Long-Term Support for CDF Shower Max Elec.**

Summary

Our Profile:

- ◆ **We Are A Prolific Group with a Dedicated, Professional Staff**
- ◆ **We Have Provided Electronics for Many ANL HEP Projects in the Last 20 Years**
- ◆ **We Actively Pursue New Projects, and Take on Leadership Roles in Electronics**
- ◆ **We Actively Pursue New Technologies and Design Methodologies**
 - » **The Electronic Support Group is a Major Resource for ANL HEP *and* Other Divisions at ANL**
 - » **We Contribute to HEP Experiments & Research World-Wide**

