Argonne NATIONAL LABORATORY

Detector Development Lunch Seminar

Current Detector R&D And Directions in Particle Physics

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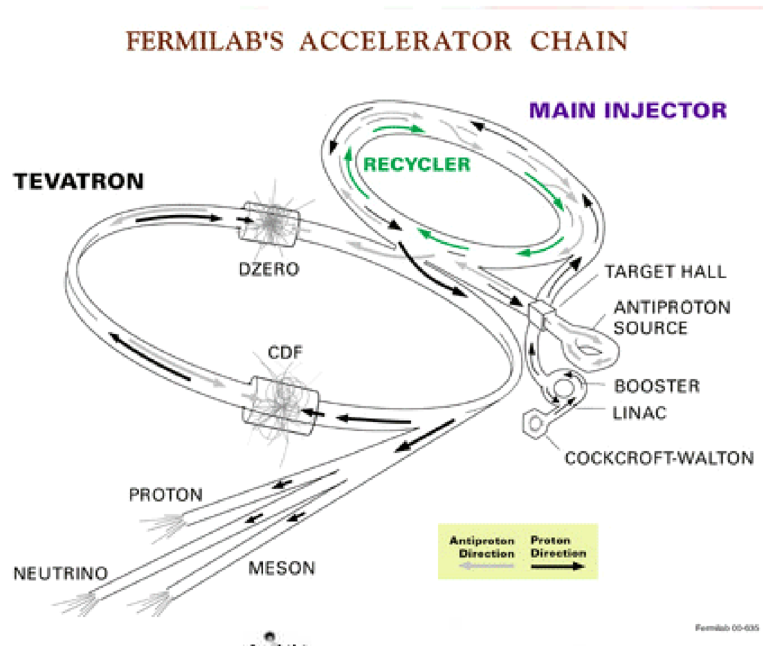
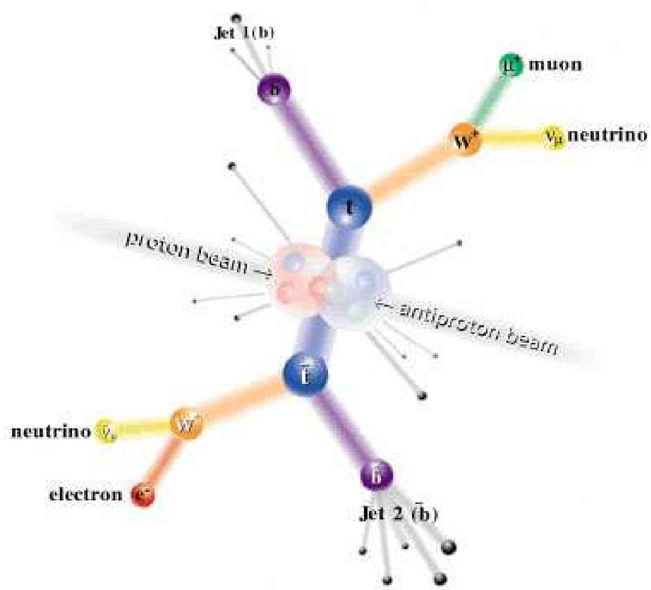
Argonne
Nov. 7, 2006

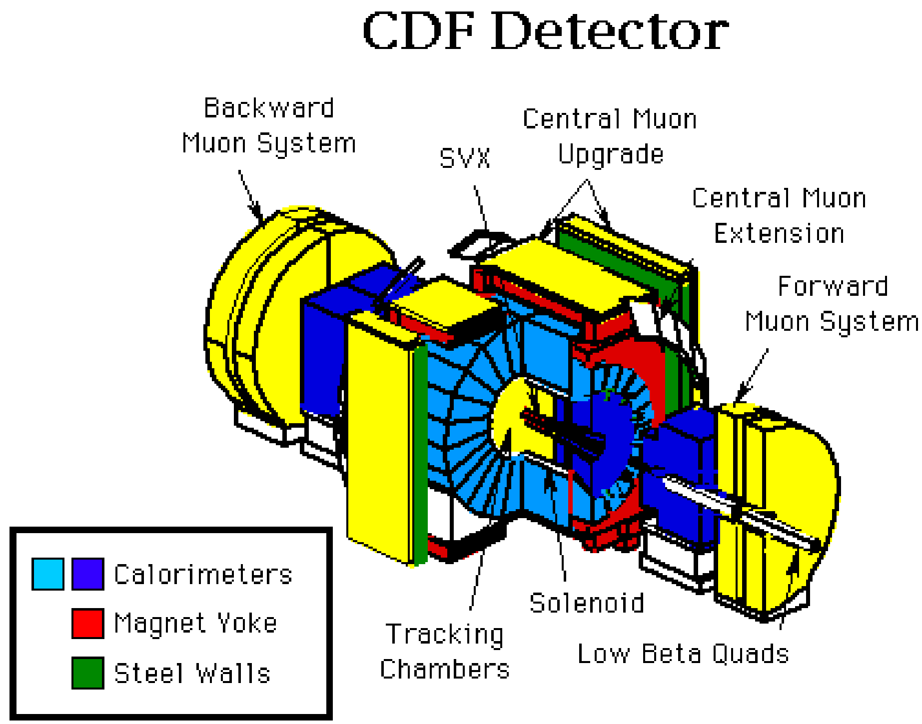
Outline of Talk

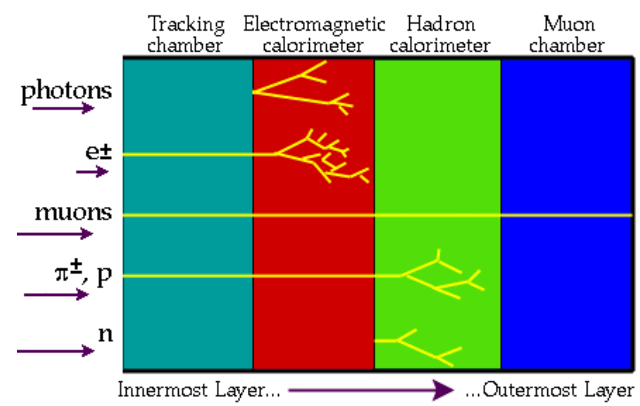
- Quick Look at HEP Detectors
- ILC Detector R&D – Driving Force in the Field
- Detector R&D in Progress at ANL HEP
- Conclusion

Current: CDF Detector – Colliding Beam Exp. at Fermilab









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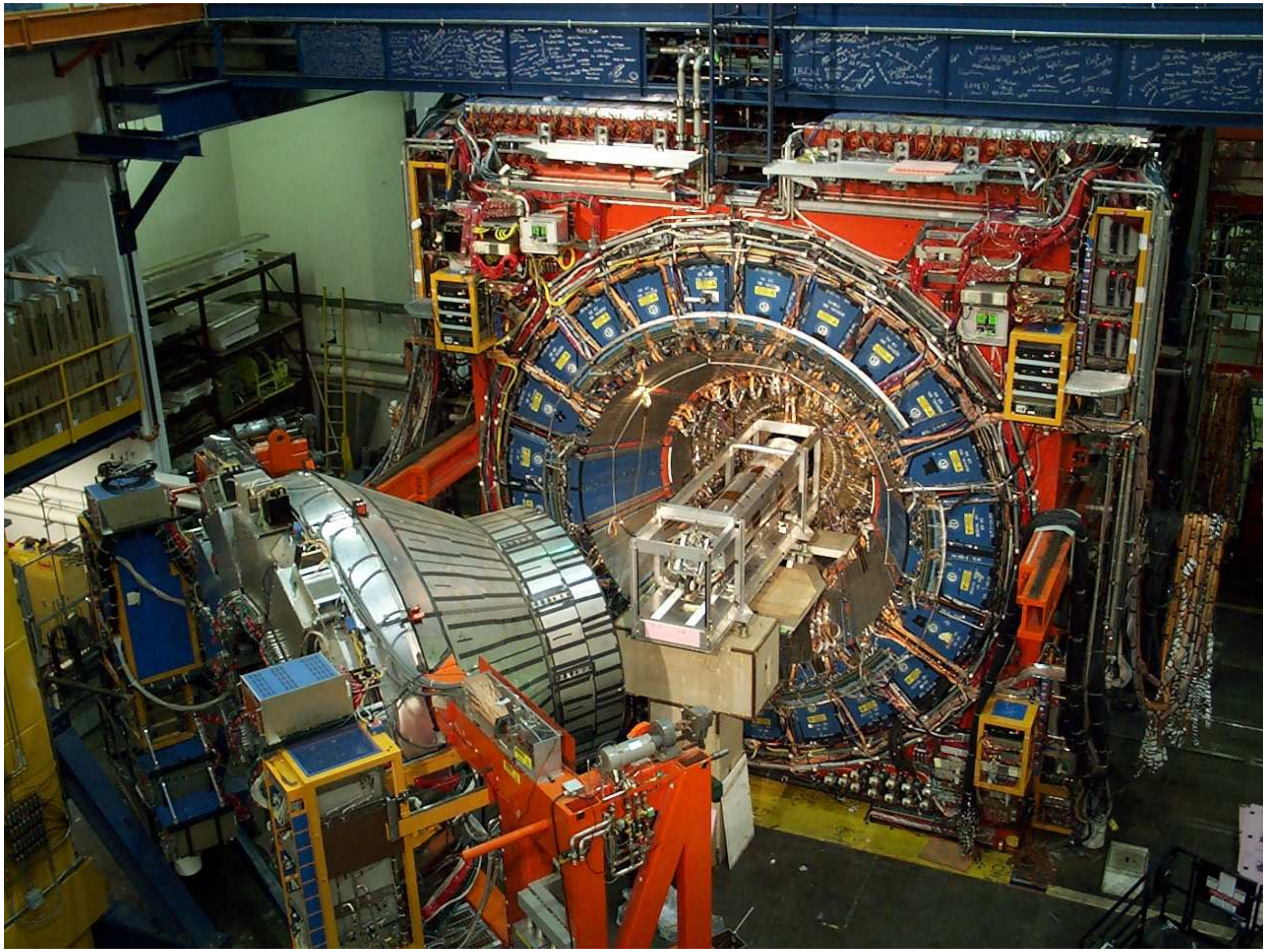
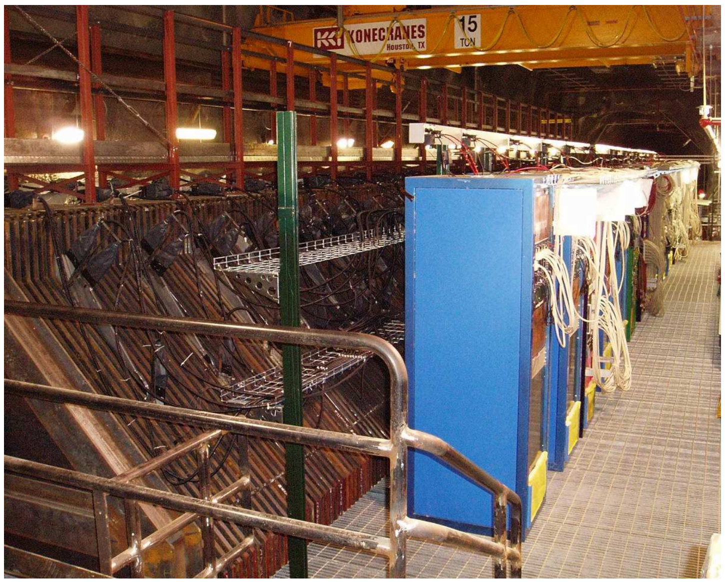


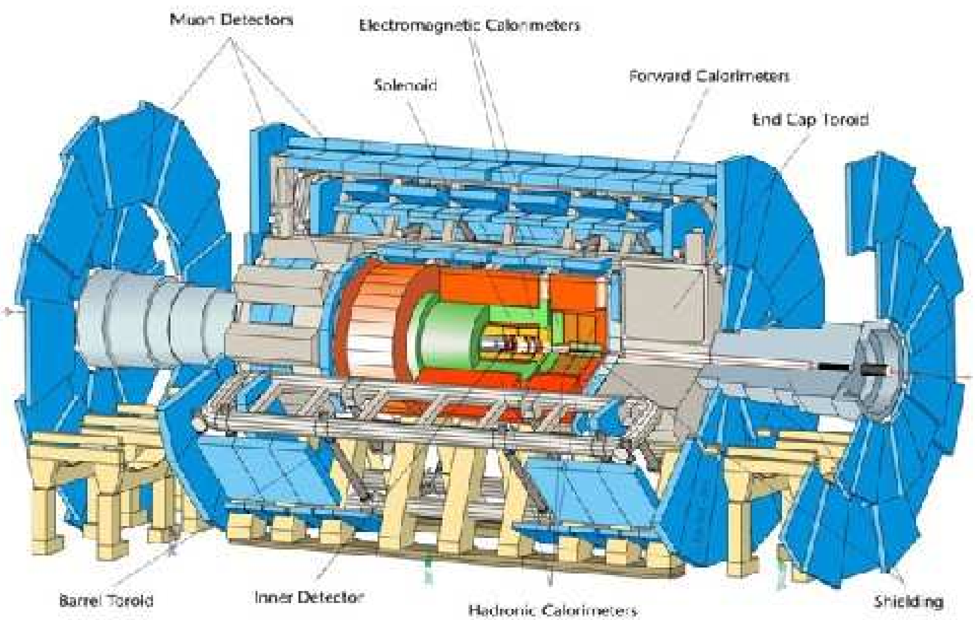
- Silicon Strip Vertex Det.
- Drift Chamber Tracking
- Wire Chambers
- Scintillator & Wave Guides
- Single-Anode PMTs
- Multi-Anode PMTs

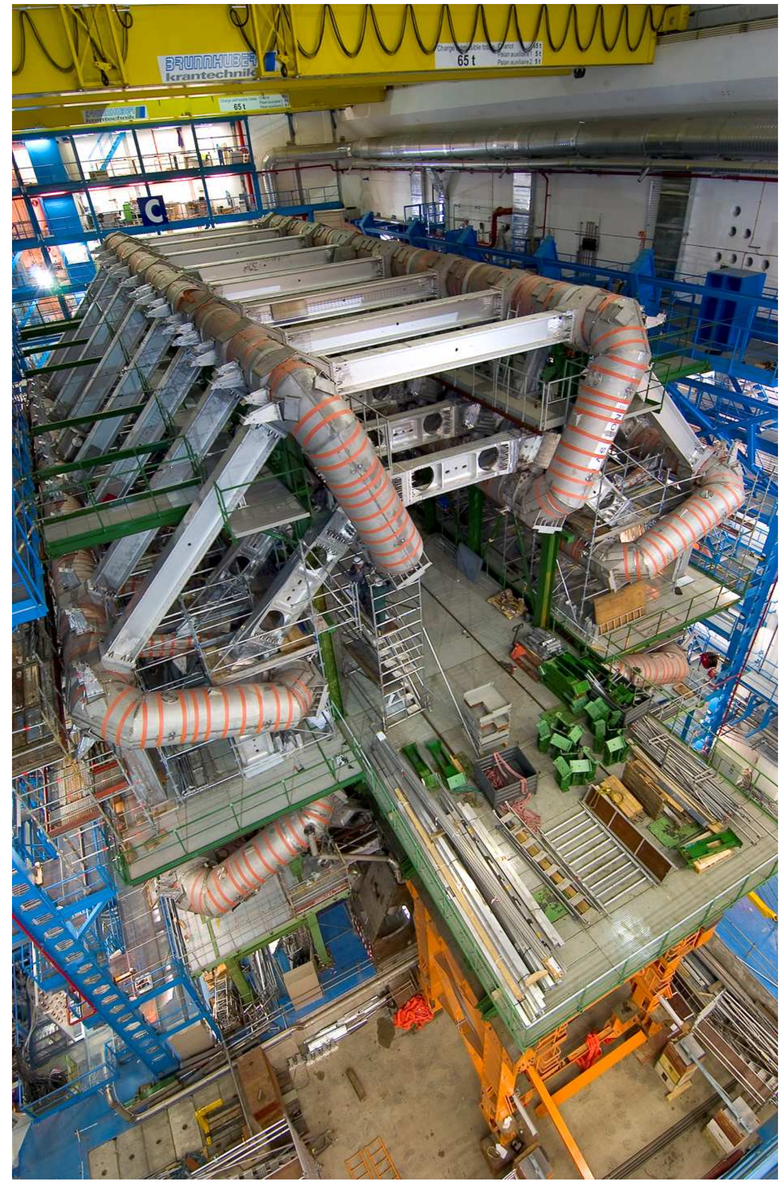
Current: MINOS Detector - Neutrino Experiment at Fermilab



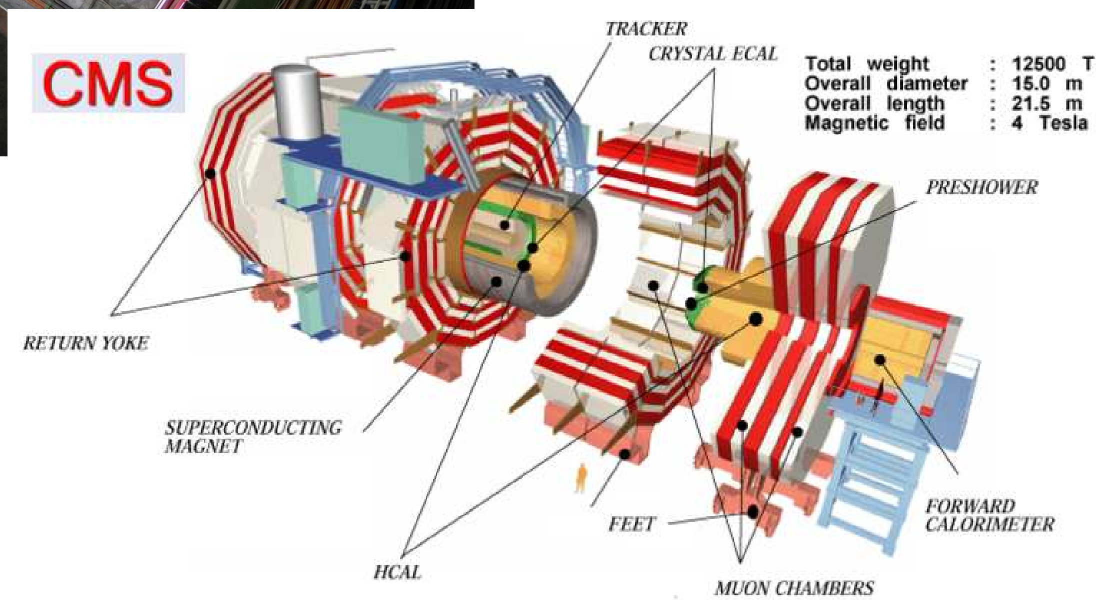
- Scintillator Strips
- Alt. Steel Planes
- WLS & Clear Fibers
- Multi-Anode PMTs

Next Generation: ATLAS Detector – Colliding Beams @ LHC (CERN)

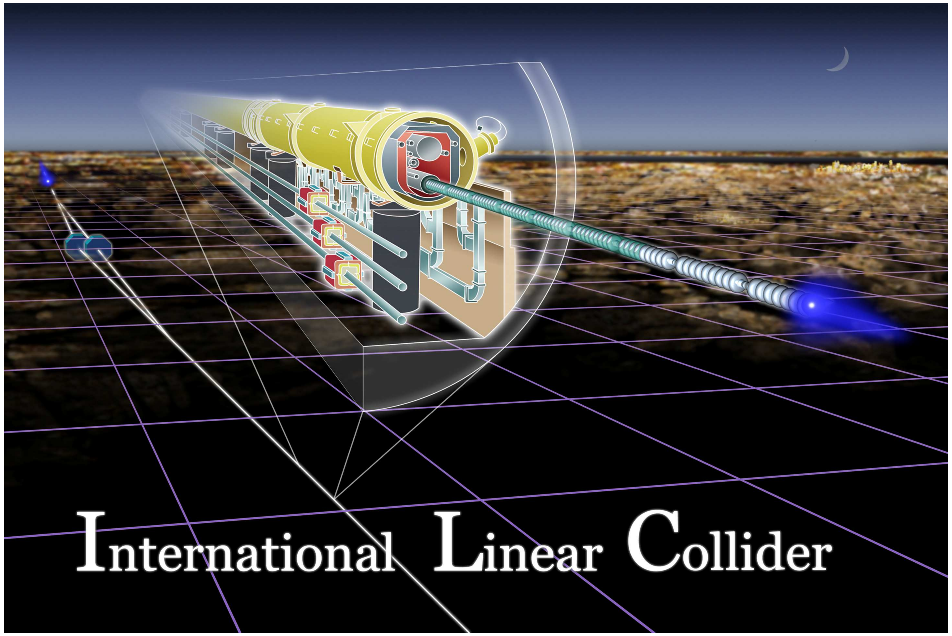




Next Generation: CMS Detector – Colliding Beams @ LHC (CERN)

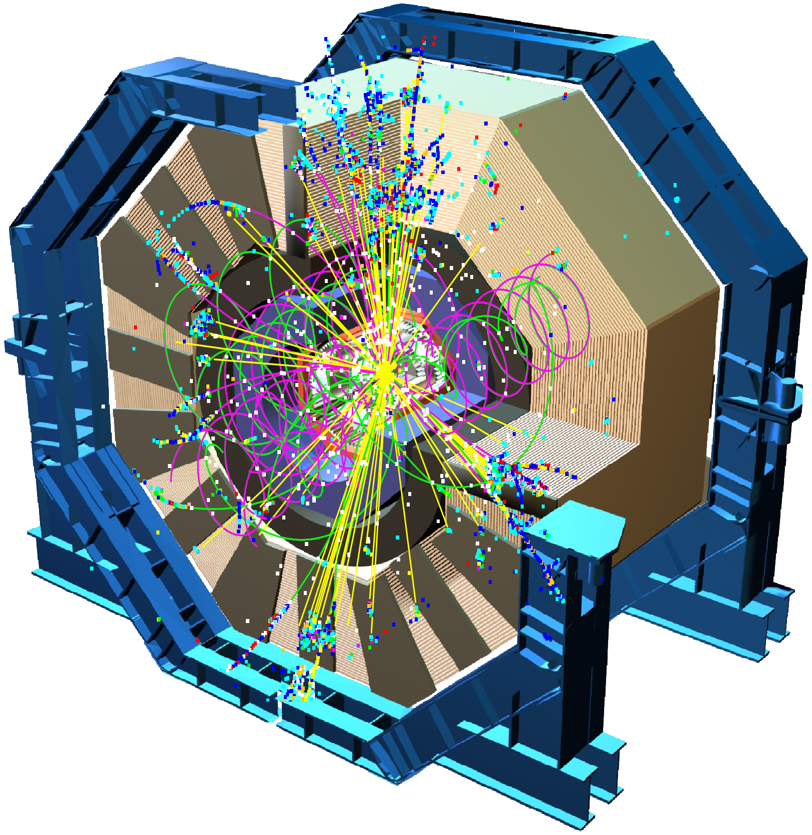


Future: International Linear Collider (ILC)



20 Km e+/e- Linear Collider

LHC will (Likely) Make Discoveries (→ Higgs)
ILC Needed for Precision Measurements



Conceptual View of SiD Detector

ILC Detector Design Criteria

Requirements for ILC

- Impact parameter resolution

$$\sigma_{r\phi} \approx \sigma_{rz} \approx 5 \oplus 10/(p\sin^{3/2}\vartheta)$$

- Momentum resolution

$$\sigma\left(\frac{1}{p_T}\right) = 5 \times 10^{-5}\ (GeV^{-1})$$

- Jet energy resolution goal

$$\frac{\sigma_E}{E} = \frac{30\%}{\sqrt{E}}$$

- ***Detector implications:***
  - Calorimeter granularity
  - Pixel size
  - Material budget, central
  - Material budget, forward

Compare to Best Performance to Date

- Need ***factor 3*** better than SLD

$$\sigma_{r\phi} = 7.7 \oplus 33/(p\sin^{3/2}\vartheta)$$

- Need ***factor 10 (3)*** better than LEP (CMS)
- Need ***factor 2*** better than ZEUS

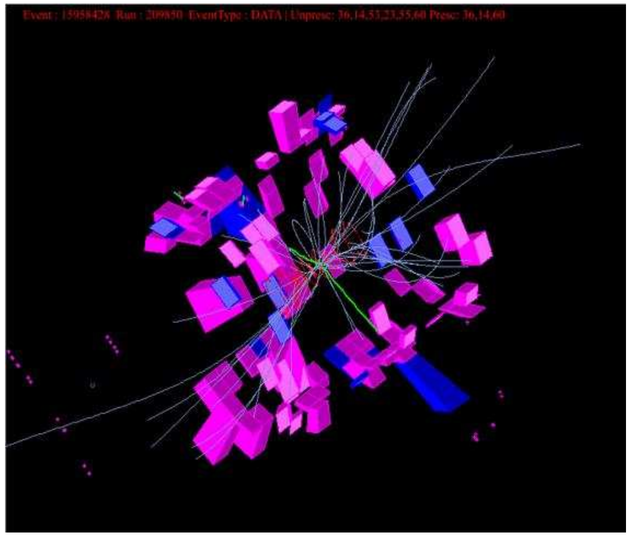
$$\frac{\sigma_E}{E} = \frac{60\%}{\sqrt{E}}$$

- ***Detector implications:***
  - Need ***factor ~200*** better than LHC
  - Need ***factor ~20*** smaller than LHC
  - Need ***factor ~10*** less than LHC
  - Need ***factor ~ >100*** less than LHC

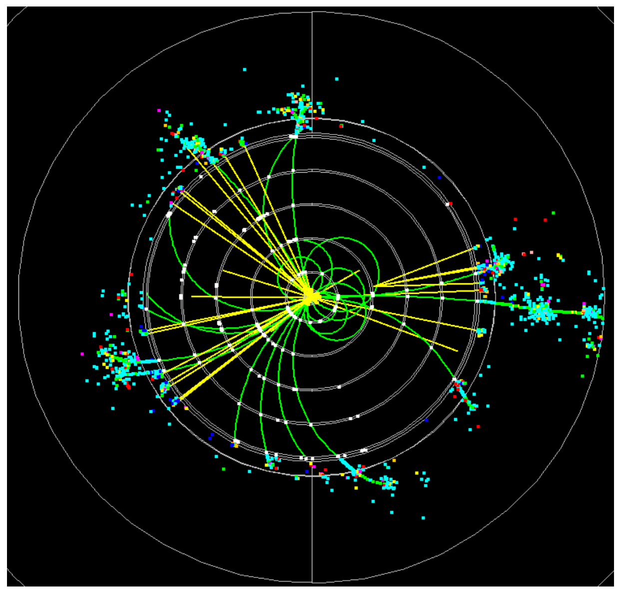
LHC: staggering increase in scale, but modest extrapolation of performance
ILC: modest increase in scale, but significant push in performance

Jet Energy Resolution

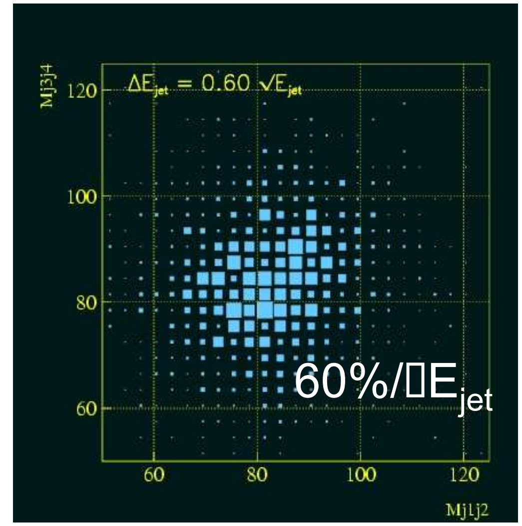
CDF:
Projective Tower Geometry

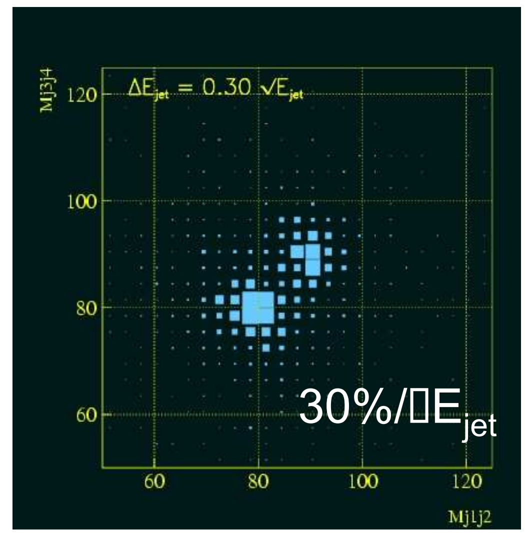


ILC:
Fine Granularity



ILC Simulations:

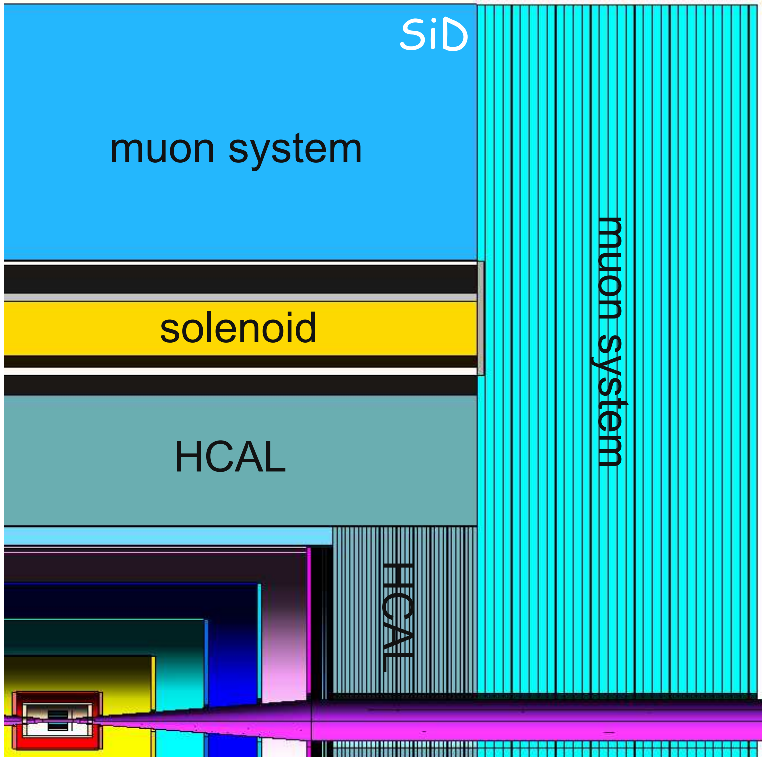




General Goal: Finer Structures, Higher Spatial Resolution

ILC Design Concept

- Calorimetry is the starting point in the SiD design → *"Silicon Detector"*
- Premises at the basis of concept:
  - "Particle Flow" calorimetry will deliver the best possible performance
  - Si/W is the best approach for the ECAL and "Digital Calorimetry" for HCAL
  - Limit calorimeter radius to constrain the costs
  - Boost B-field to maintain BR^2
  - Use Si Tracking system for best momentum resolution and lowest mass
  - Use Pixel Vertex detector for best pattern recognition
- Detector is viewed as single fully integrated system, not a collection of different subdetectors



HEP Detector Development Trends

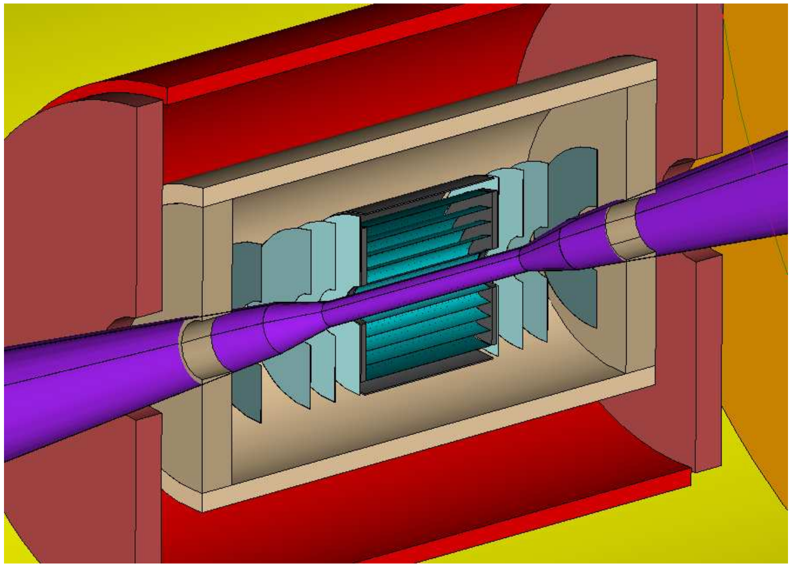
- General Trends (1):
  - Push toward Smaller Feature Sizes → ~10 μm^2
  - Emphasis on Monolithic and Semiconductor Technologies
  - Extensive R&D in Improving Older Technologies
  - Exploring New “Methodologies” → “Particle-Flow Algorithms”
- Consequences:
  - Results in Higher Channel Count
  - High Dynamic Range (Probably) Not Viable
  - *Must Keep Data Volumes Manageable*
  - *Must Keep Inner Mass Low, Power Consumption Low*
  - *Must Keep Costs Down*
- General Trends (2):
  - Exploring “All Digital” Techniques
    - → Trade High Dynamic Range Over Large Fiducial Volume, for Low Dynamic Range (~1 Bit) Over Small Volume
      - → Quantum Counting, Pattern Recognition
  - High Degree of Integrating Electronics with Detectors
    - → ***Custom Integrated Circuits (ASICs)***

HEP Detectors

- Summary of General Properties:
  - Very Large Objects
  - 1E5 → 1E9 Channels
  - Multiple Detector Subsystems, Complex Mechanical Design
  - Very High Data Rates
  - Sophisticated, Multi-Level Trigger Systems
  - Cost \$100M → \$500M
  - 5 – 10 Years to Build
  - Collaborations: 100 – 2000 People

ILC Vertex Detection and Tracking

- Tracking system Requires High-Resolution Vertex Detection → ***Pixel Detectors***
- Detector requirements
  - Spatial resolution: < 4 μm
  - Smallest possible inner radius
  - Transparency: ~0.1% X_0 per layer



- Inner layer 1.6 MPixel sensors
  - Background hits in excess of 1/mm^2 → pattern recognition problems
  - Need ~ 50μs per frame readout speed

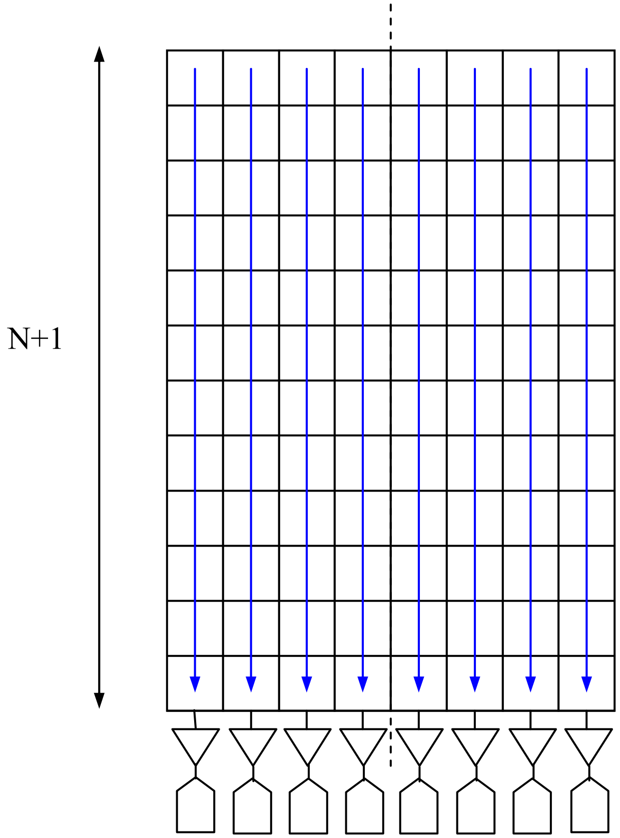
- ***Baseline Design: Fast CCDs***
  - Development well underway
  - Need to be fast (50 MHz)
  - Read out in the gaps

- ***Competing developments:***
  - MAPS
  - SOI
  - 3D
  - Hybrid

(“Detectors for the ILC,” Dec. 16, 2005 -- M. Demarteau, FNAL)

Column Parallel CCD

- R&D carried out by LCFI Collaboration (Bristol, Glasgow, Lancaster, Liverpool, Oxford, RAL) in collaboration with e2v Technology



Column Parallel CCD
Readout time = $(N+1)/F_{out}$

- 20 µm x 20 µm pixel size
- Separate amplifier and readout for each column, compared to 'rolling shutter'
- Designed for 50 MHz clock speed
- Current Results:
  - Operates at clock > 25 MHz
  - Minimum clock of ~ 1.9 V
  - Noise is ~ 100 electrons
- Second generation of CP-CCD's
  - Symmetric clock
  - Goal is to clock at highest frequency at lowest voltage
- CCD design needs separate read-out ASIC

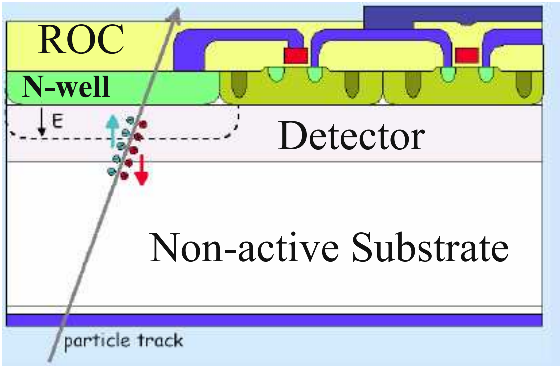
("Detectors for the ILC," Dec. 16, 2005 -- M. Demarteau, FNAL)

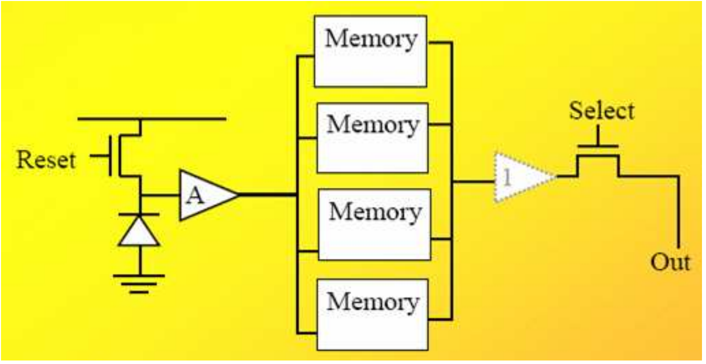
CMOS Monolithic Active Pixel Sensors

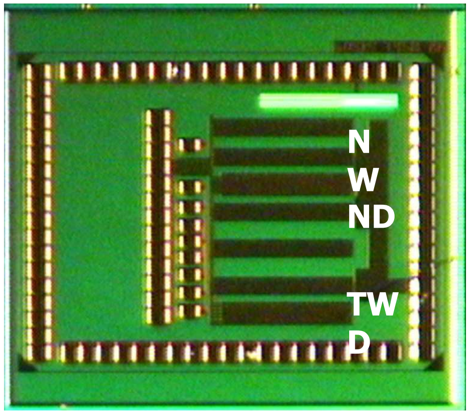
- A MAPS device is a silicon structure where the detector and the primary readout electronics are fabricated on the same substrate
- Basic CMOS architecture is 3 transistor cell
  - signal created in epitaxial layer
  - thermal charge collection (no HV)
  - charge sensing through n-well/p-epi junction
- Example: Development for Super-Belle (Gary Varner, Hawaii):
  - 128x928 pixels/sensor
  - pixel size: 20x20 μm²; 36 transistors/pixel; 5 metal layers; TSMC 0.25 μm process
  - Column select readout, 10μs/frame
  - Signal~300e, Noise ~ 20-35e⁻ → S/N ~ 10-15
- Example: Test Chip at FNAL (Ray Yarema):
  - 80 row x 3 column pixel array
  - Test structures, SEU tests
  - 130 nm chip in IBM CMOS

→ Yarema Talk Nov. 9

(“Detectors for the ILC,” Dec. 16, 2005 -- M. Demarteau, FNAL)

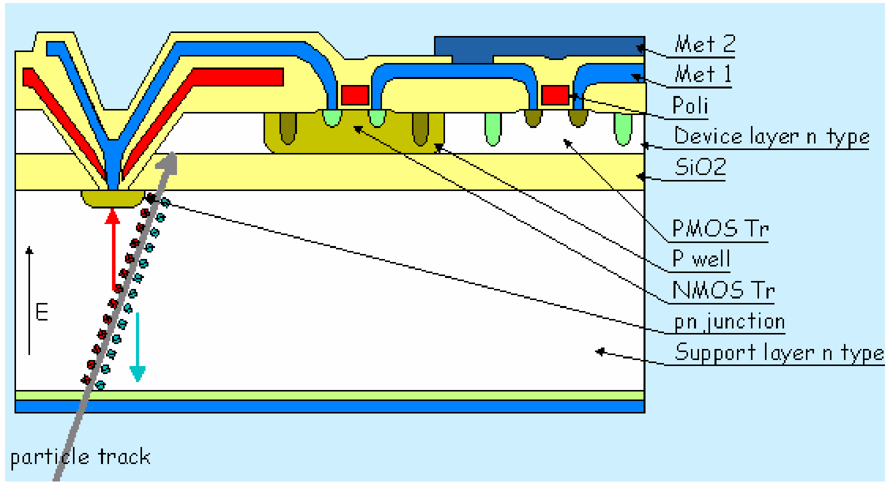






Silicon On Insulator

- Silicon on Insulator (SOI)
  - Non-standard process
  - Handle wafer, normally passive is the detector
  - Signal collected in fully depleted substrate, produce large signals
  - Electronics in the device layer
  - Should be rad. hard; can have NMOS and PMOS transistors



R&D IN Progress at Fermilab

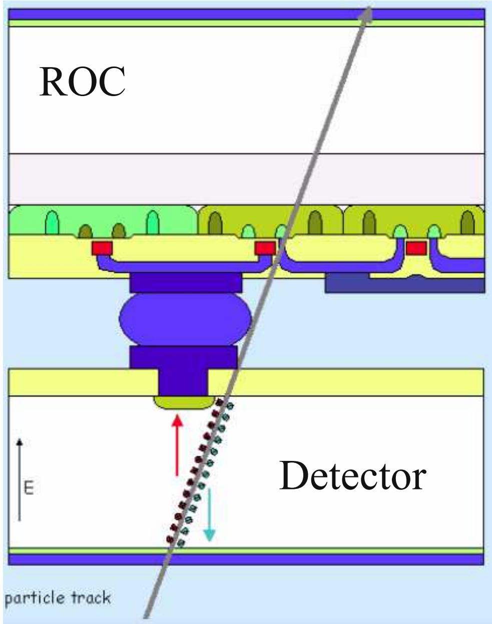
- Process Technology
  - Allows for production of pixel sensors which are thin (<50 microns)
  - Excellent and well controlled charge collection using fully depleted devices
  - Use full CMOS readout without parasitic charge collection
  - High-resistivity handle wafer as detector

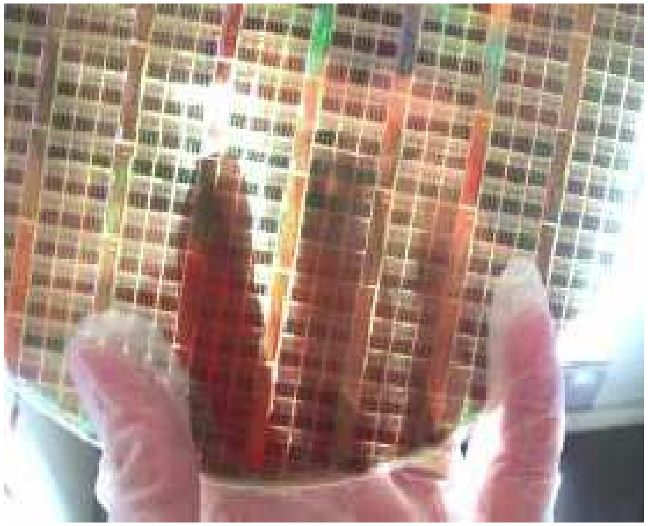
- Collaboration with industry (American Semiconductor) through SBIR grants

("Detectors for the ILC," Dec. 16, 2005 -- M. Demarteau, FNAL)

Hybrid Pixel Detectors

- Hybrid pixel detectors have separate detector and readout chip, connected by bump bond
  - sensor and read-out chip (ROC) can be optimized separately
- Continuing issues with this technology:
  - cooling of detectors under high radiation
  - mass and cost
- Ongoing studies at Fermilab:
  - Thinning of read-out chip down to 80 μm, bump bonded to prototype sensors
    - *Current Best: ALICE: 150 μm*
  - Power management and cooling requirements
  - Efficiency, time resolution, readout speed, zero-suppressed readout.



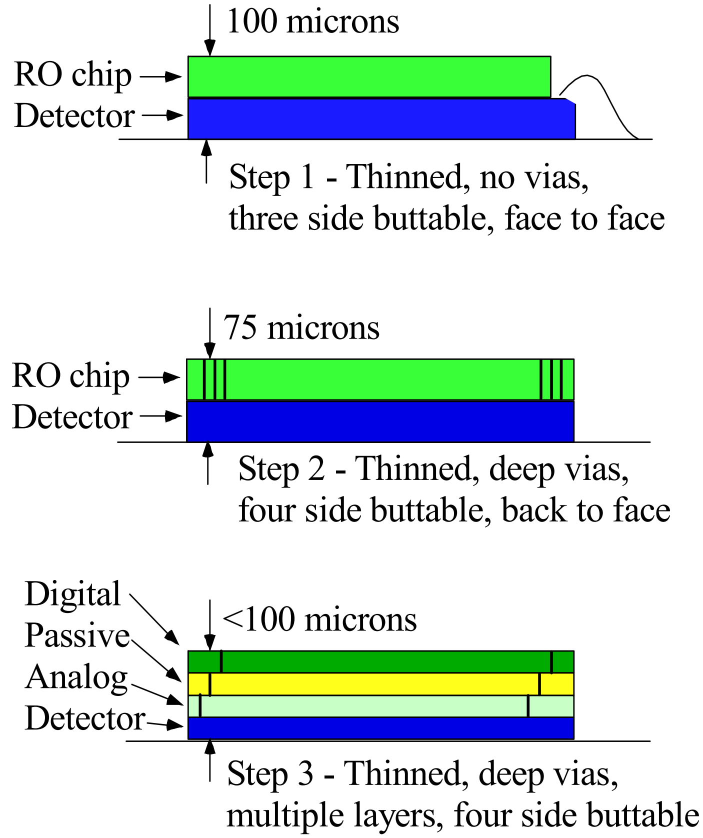


Thinned Wafer Mounted on Glass Substrate

("Detectors for the ILC," Dec. 16, 2005 -- M. Demarteau, FNAL)

3D Processes

- A 3D device is a chip comprised of 2 or more layers of semiconductor devices which have been thinned, bonded, and interconnected to form a monolithic circuit
  - Layers can have devices made in different technologies
    - *Process optimization for each layer*
- Direction in industry
  - Early push for device scaling, circuit integration and packaging density
  - Interconnect and packaging issues are real barriers
  - Push towards planar approach: 3D
- Critical issue is thinning and bonding of the various layers



R&D IN Progress at MIT & Fermilab

→ Yarema Talk Nov. 9

("Detectors for the ILC," Dec. 16, 2005 -- M. Demarteau, FNAL)

Photo-Detector R&D at ANL HEP

- ANL HEP has Long History in Building Calorimeters
  - Traditionally, Scintillator & Photodetectors
  - CDF, ZEUS, MINOS, ATLAS TileCAL

- Active Photodetector R&D is Continuing
  - Advanced Time-of-Flight (LHC or ILC) → Pico-Second Timing
  - Particle Astro-Physics: New Ground-Based Telescope Technologies
  - Medical Instrumentation: PET

- Quick Look at 3 Technologies:
  - Multi-Anode PMTs (MAPMTs)
  - Micro-Channel Plates (MCPs)
  - Silicon PMTs (SiPMs)

- **Other ANL Detector R&D Currently On-Going:**
  - **NOvA Detector - FNAL Long-Baseline Neutrino Experiment**
    - ***Liquid Scintillator, APD Readout***
  - **ILC Detector – Digital Hadron Calorimetery (DHCAL)**
    - ***Resistive Plate Chambers (RPC's) → Repond Talk Oct. 31***

Overview of Photo-Detector Properties
(CCD's Omitted)

Photodetector	Min. Time Resolution	Feature Size	Current Min-Max	Gain	ΔG	QE	Photo Converter
Vacuum PMT	300 pS	1 cm	5 nA-10 mA	10^6	0	20%	Bialkali
MAPMT	300 pS	2 mm	1 nA-100μA	10^6	3:1	20%	Bialkali
MCP	10-30 pS	1 mm	10 nA-10μA	10^6	1:1.5	20%	Bialkali
PIN Diode	1 nS	-	1 μA	1	0	80%	Silicon
APD	1 nS	100 nm	10 nA-100 nA	10^2	small	80%	Silicon
SiPM (MRS)	300 pS	1 mm	?	10^6	small	40%	Silicon

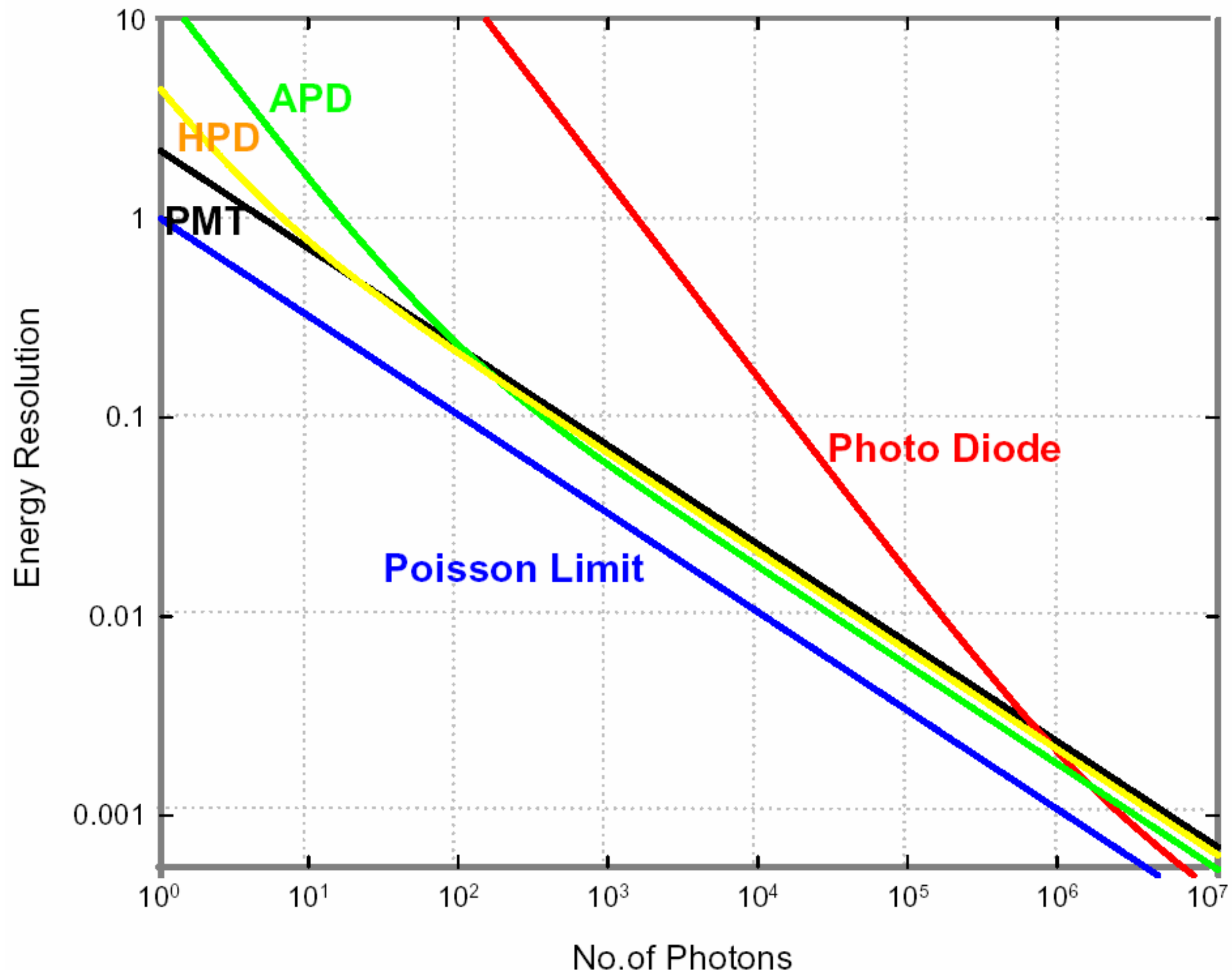
Desirable Properties for Photo-Detectors

- High Gain
- High QE, 300-600 nm
- No After Pulsing
- Dynamic Range > 1000
- Good Linearity
- Low Dark Noise
- Single pe Resolution
- Fast Signal

Inexpensive would be Nice…

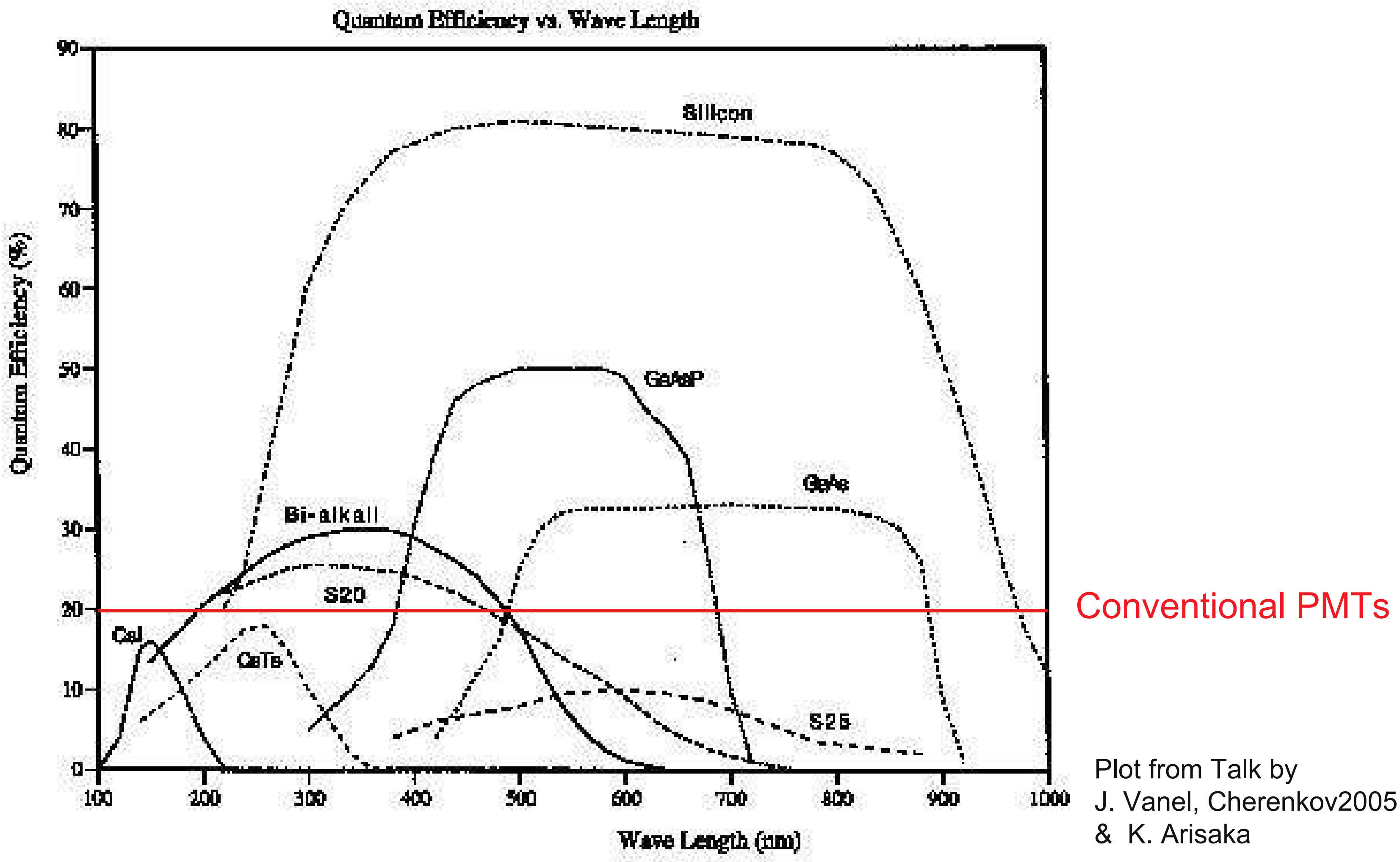
Adapted from
J. Vanel, Cherenkov2005

Overview of Photo-Detector Properties



Plot from Talk by
J. Vanel, Cherenkov2005
& K. Arisaka

Overview of Photo-Detector Properties



Plot from Talk by
J. Vanel, Cherenkov2005
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Multi-Anode PMTs

Principle of Operation

Very Similar to Conventional PMT

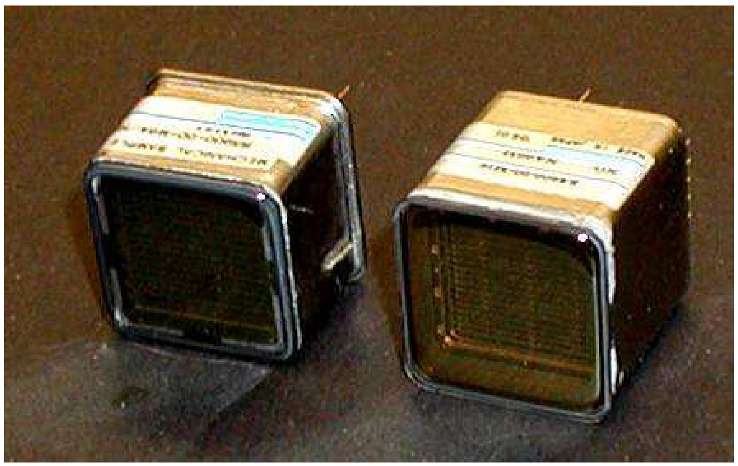
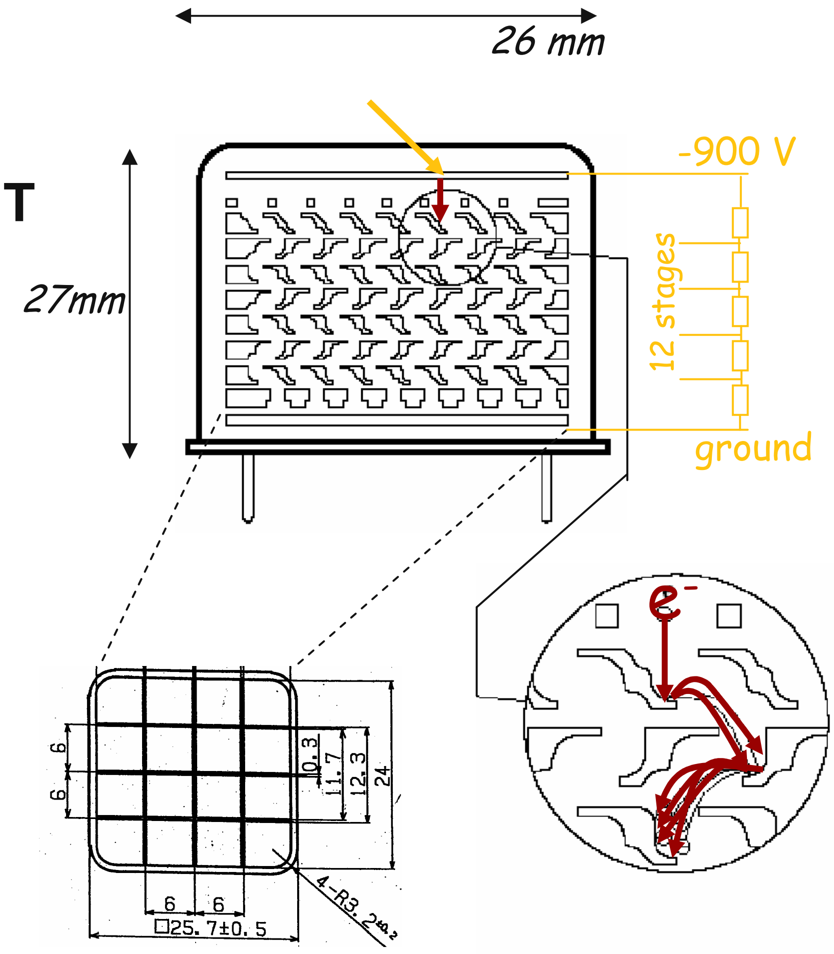


Photo & Drawing from Talk by
Tomasz Skwarnicki, BTeV



MAPMT: Hamamatsu R8900-M16

Multi-Anode PMTs

Photo from Talk by
Tomasz Skwarnicki, BTeV

HAMAMATSU

PRELIMINARY DATA SHEET
Jun.2003

PHOTOMULTIPLIER TUBE

R8900-00-M16

4 x 4 Multianode, Small Dead Space ,Fast Time Response
26 mm Square,Bialkali photocathode, 12 stage, Head-on Type, UV window

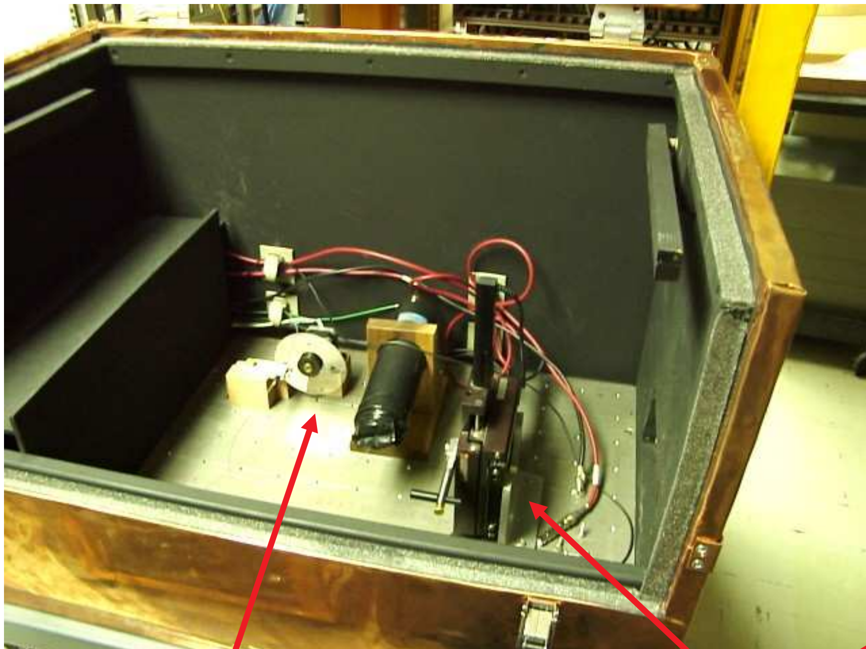
General

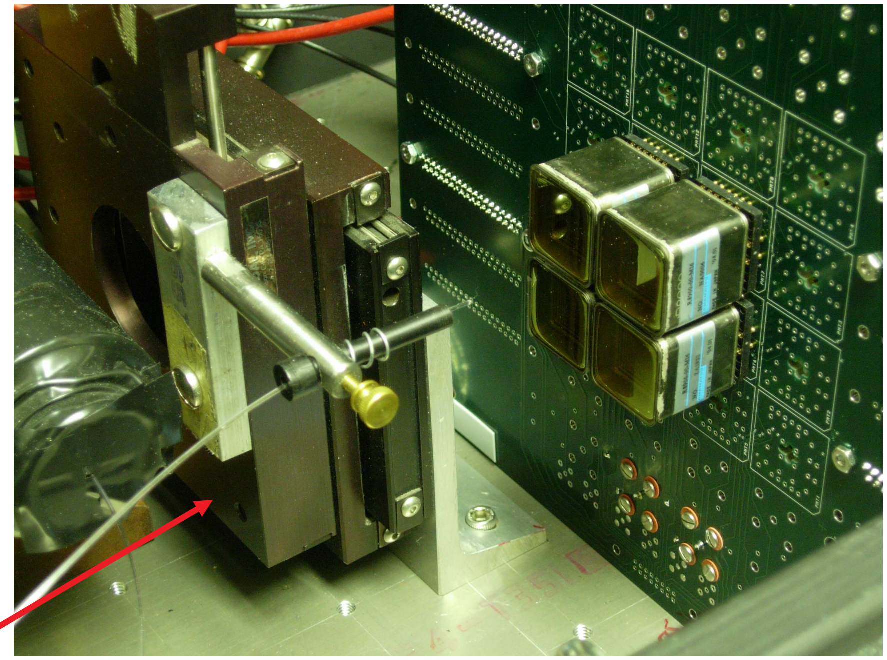
Parameter		Description	Unit
Spectral response range		185 to 650	nm
Window material		UV glass	-
Photocathode	Material	Bialkali	-
	Minimum Effective Area	24 x 24	mm^2
Dynode structure		Metal channel dynode	-
Number of stages		12	-
Weight		Approx 28	g
Operating Ambient Temperature		-30 to +50	deg C
Storage Temperature		-80 to +50	deg C

Maximum Ratings (Absolute Maximum Values)

Parameter	Value	Unit
Supply voltage Between Anode and Cathode	1000	V dc
Average anode current	0.1	mA

Multi-Anode PMTs



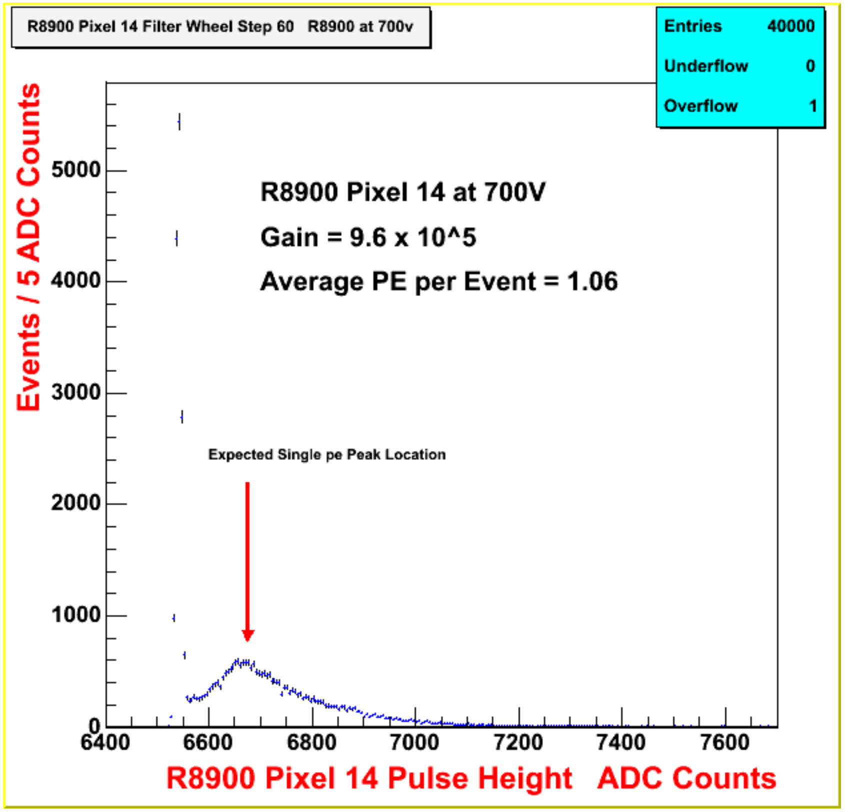


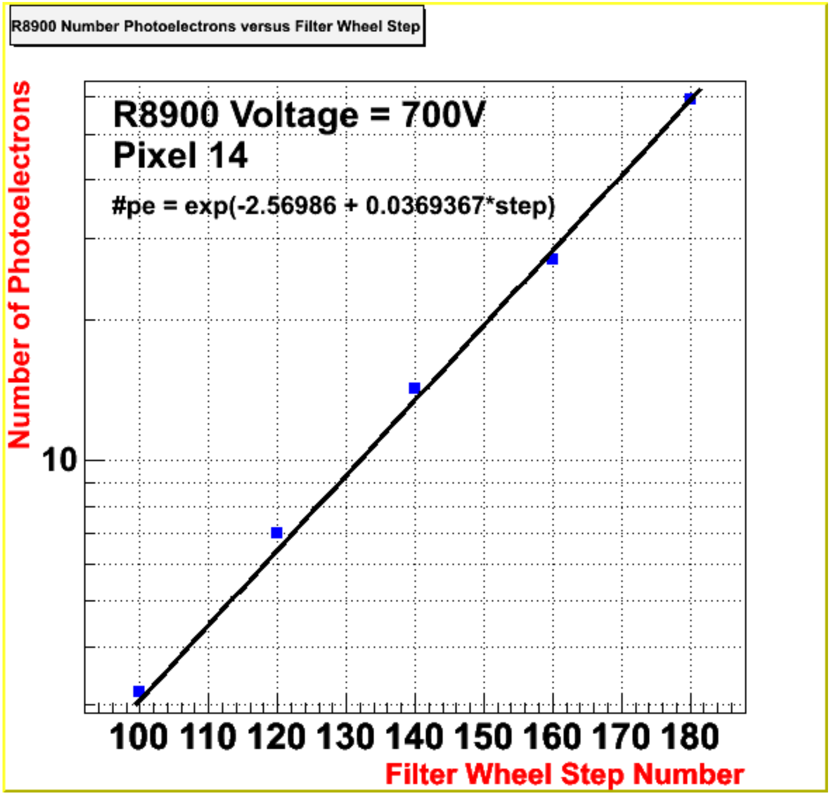
4-Decade Filter Wheel

XY Stage

Test Stand & Evaluation of R8900 at Argonne
For Use in Trice Telescope R&D

Multi-Anode PMTs





Test Results of R8900 at Argonne
(Courtesy Bob Wagner, ANL)

Multi-Anode PMTs

HAMAMATSU

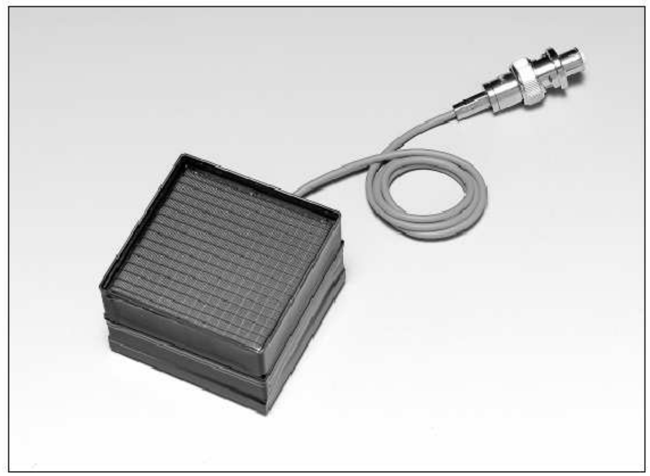
PRELIMINARY DATA
APR. 2004

FLAT PANEL TYPE
MULTIANODE PHOTOMULTIPLIER
TUBE ASSEMBLY
H9500

52 mm Square, Bialkali Photocathode, 12-stage,
16 × 16 Multianode, Small Dead Space, Fast Time Response

APPLICATIONS

- Small Animal Imaging
- Compact Gamma Camera
- Scinti-mammography
- 2D Radiation Monitor
- Ring Image Cherenkov Counter



Another MAPMT Candidate – 256 Channels
(Not Evaluated Yet)

Multi-Anode PMTs

- **Nice Features:**
  - High Gain
  - Good Pixel Size
  - Good pe Response
  - Good Linearity & Dynamic Range
  - Good Dark Count Rates
  - Fair Packaging,
    Some Improvement of Dead Space Needed
- **Not-So-Nice Features:**
  - Pixel Non-Uniformity 2:1 – 3:1 Requires Calibration, LUTs
  - Triggering from Dynode Incurs
    Pixel Non-uniformity Penalty
  - Gains Limited to ~1E5 for High-Rate Environments,
    Reduces Resolution of Single pe Peak
  - Quantum Efficiency ~20%, Could Use Improvement

Micro-Channel Plates

MCP BASICS

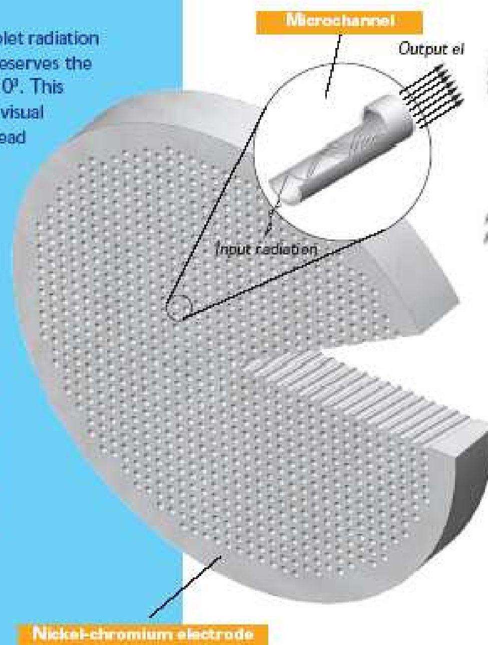
A microchannel plate (MCP) is an electron multiplier for detecting X-rays, ultraviolet radiation and charged particles. The output is a two-dimensional electron image that preserves the spatial resolution of the original input radiation, but with a linear gain of up to 10^3. This may be used for exciting a phosphor screen placed close to the output, giving a visual representation of the radiation pattern. Alternatively, the electron image can be read out by, for example, a wedge-and-strip or fast delay-line anode array.

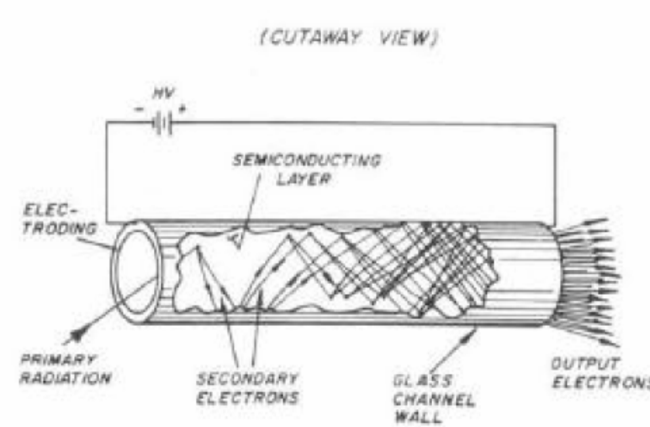
Important features of MCPs are:

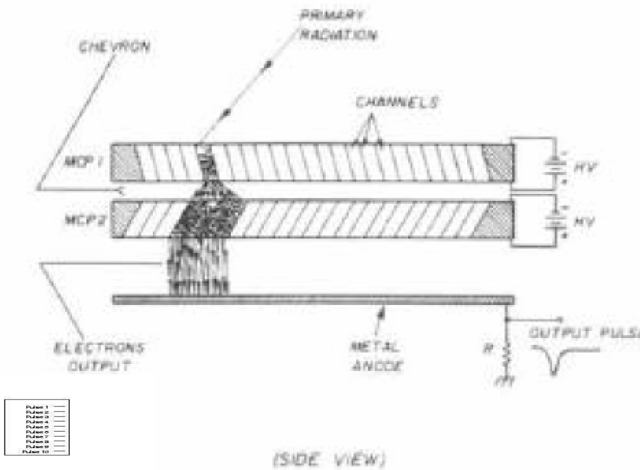
- high electron gain
- immunity from magnetic fields
- fast response
- low noise
- low power consumption
- high spatial resolution
- small size and ruggedness.

Each plate consists of an array of tiny glass tubes fused together to form a thin disc. Both faces of the disc are metallized to provide parallel electrical connections to all channels. In a vacuum, and with a potential difference (usually 800 to 1400 V) across the plate, each channel becomes a continuous dynode electron multiplier, operating on the same principle (electron avalanche) as its cousin – the single-channel electron multiplier.

Battery viewed through an MCP demonstrating the high open area.

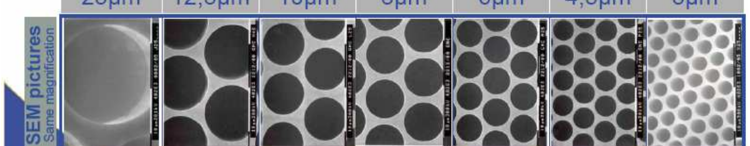




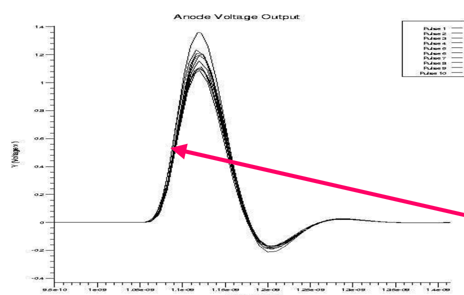


Drawings from Paper by
J. L. Wiza, NIM 162, 1976

Standard channel diameter						
25µm	12,5µm	10µm	8µm	6µm	4,5µm	3µm



PHOTONIS imaging sensors



Jitter on Leading Edge
0.86 psec

Micro-Channel Plates

PLANACON™ PHOTOMULTIPLIER TUBE ASSEMBLY 85021-600

BURLE

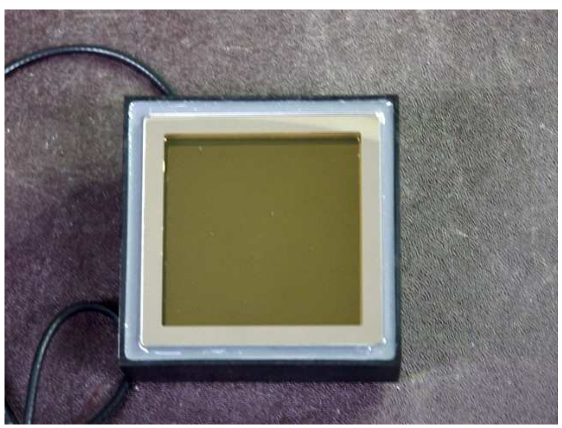
July 2005

GENERAL

Parameter		Value	Unit
Spectral Response		185 to 660	nm
Wavelength of Maximum Response		400	nm
Active Area		51 × 51	mm
Photocathode Material		Bialkali	--
Window	Material	UV Grade Fused Silica	--
	Thickness	2.0	mm
Multiplier	Structure	MCP (25μm pore, 40:1 L:D)	--
	Number of Stages	2	--
Anodes	Number	1024 (32 x 32)	
	Size / Pitch	1.4 / 1.6	mm

Maximum Ratings (Absolute Maximum Values)

Parameter		Value	Unit
Supply Voltage	Cathode:MCP_{in} MCP_{in}:MCP_{out} MCP_{out}: Anode	500 2000 500	VDC
Average Anode Current, sum of all anodes		3	μA
Ambient Temperature		- 15 to + 50	°C



Testing in Progress ANL
Looking at Fast Timing (~1 pSec)
Large-Area TOF
(Collaboration with Univ. of Chicago)

Micro-Channel Plates

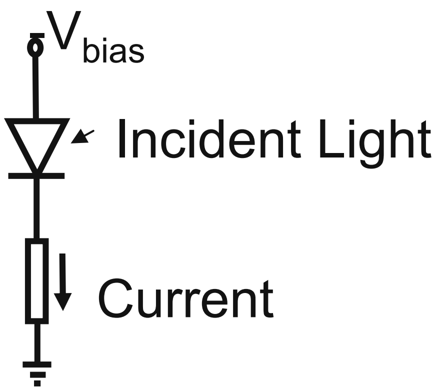
- **Nice Features:**
  - Custom-Tailor Your Pixel Size
  - Good Single pe Response
  - Good Linearity & Dynamic Range
  - Good Pixel Uniformity, Might Still Need Calibration
  - Low Dark Count Rates
  - Excellent Timing Resolution

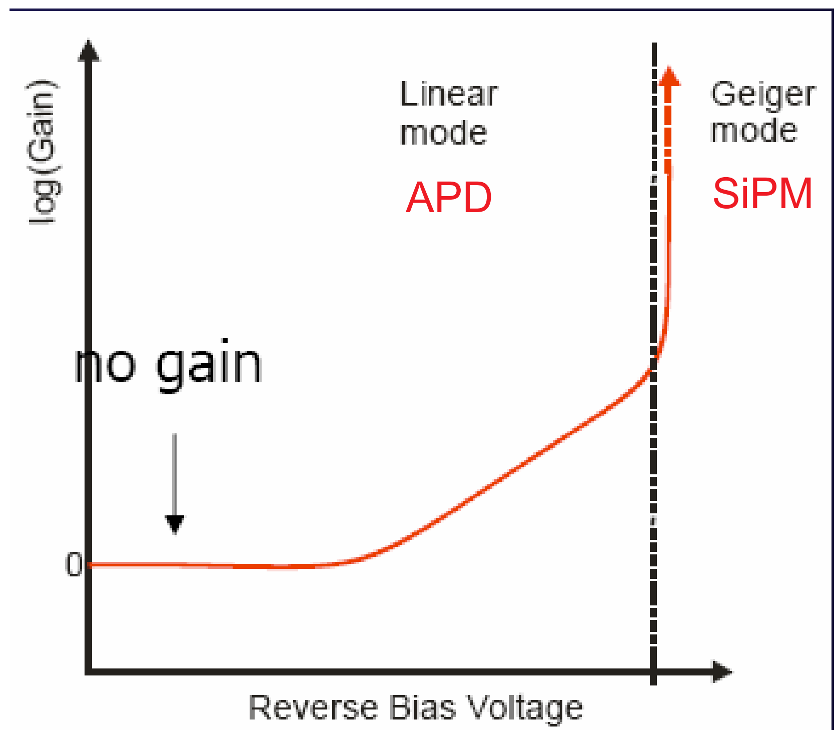
- **Not-So-Nice Features:**
  - No Dynode for Trigger
  - Current-Return Path Not Well Defined Presently…
  - Slow Recovery of Individual Channels, ~mSec
  - Quantum Efficiency ~20%, Could Use Improvement
  - Packaging Needs Improvement for Dead Space
  - Operates on 2000V

Silicon Photo-Multipliers

Principle of Operation

Single Photodiode





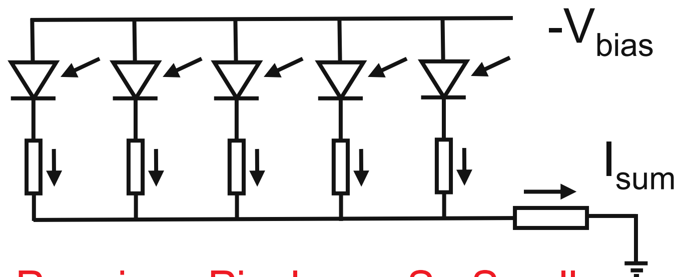
Adapted from Talk by
Nepomuk Otte, SNIC06

- Mode of Operation Depends on
  - Doping & Purity of Silicon
  - Bias Voltage
  - Geiger Mode Needs Quenching

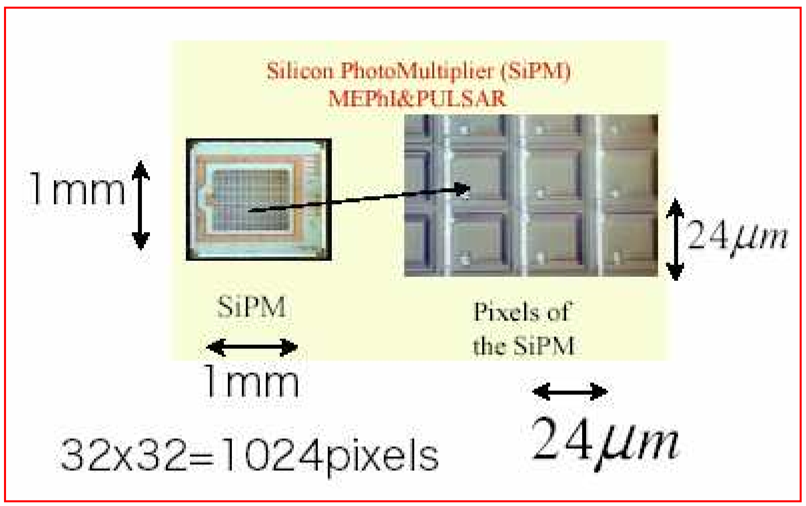
Silicon Photo-Multipliers

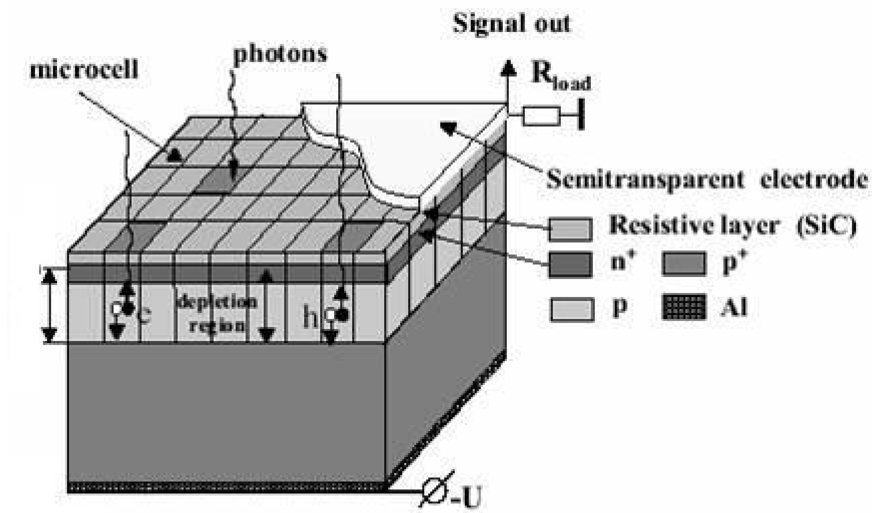
Principle of Operation

Photodiode Array – Sum Individual Pixels



Premise: Pixels are So Small That 1 Pixel = 1 pe

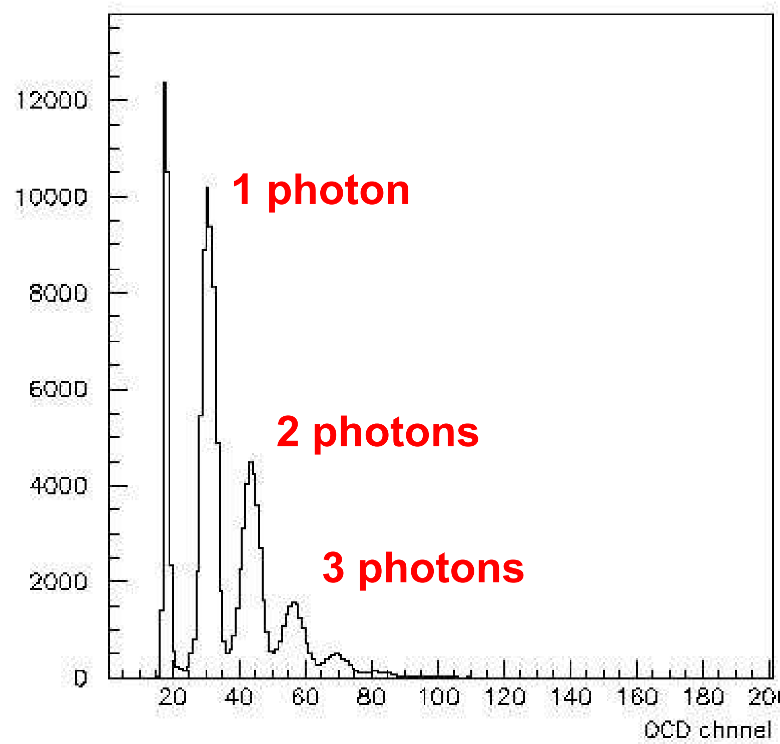




Photos from Talk by V. Saveliev, 5/4/06

Silicon Photo-Multipliers

- **SiPM Main Features**
  - Sensitive Size 1x1 mm^2
    24x24 = 576 pixels
    32x32 = 1024 pixels
    2x2 mm2, 4x4 mm2 Possible
  - Operating Voltage : 40 to 60V
  - Gain : 10^5 up to 10^6
  - Single Pixel Time Resolution : ~ 100ps
  - Single Pixel Recovery Time : ~1 μs
  - No Sensitivity to Magnetic Fields

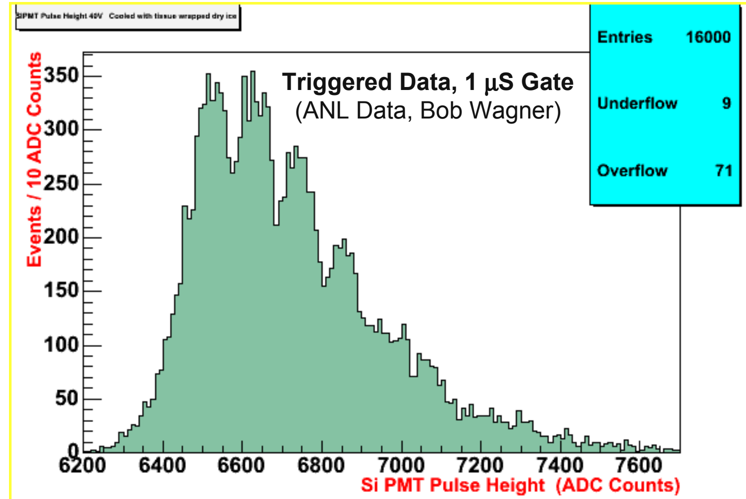


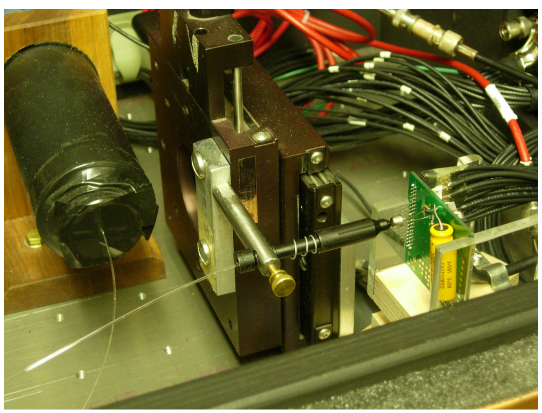
Triggered Data, ~50 nS Gate

Adapted from Talk by
V. Saveliev, 5/4/06

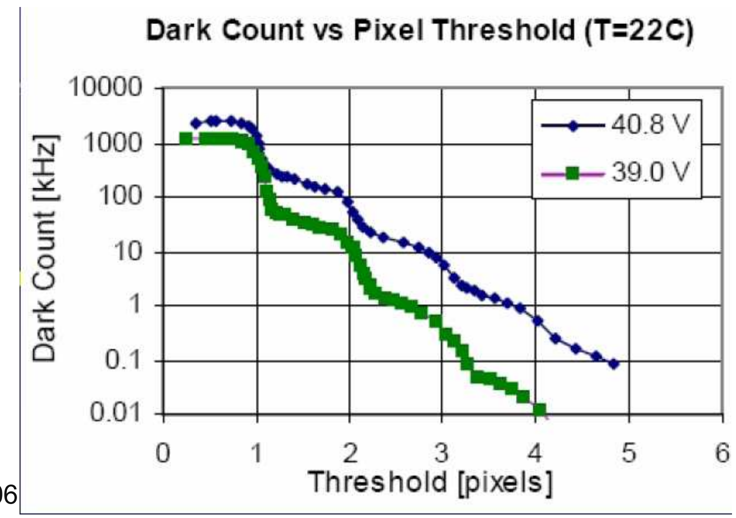
Silicon Photo-Multipliers

- **SiPM "Features"** Adapted from Talk by J. Vanel, Cherenkov2005
  - Dark Noise Rate:
    - ~1 MHz/mm^2 @ Room Temp
    - ~1 KHz/mm2 @ 100⊕K
  - Optical Crosstalk
    - Hot-Carrier Luminescence
    - Improvements with Trenching
  - Dynamic Range
    - 1 pe/pixel → Limit # Pixels





ANL Teststand



Adapted from Talk by Nepomuk Otte, SNIC06

Silicon Photo-Multipliers

- **Nice Features:**
  - Small Size
  - Low Operating Voltage
  - Good pe Resolution (If Do It Right…)
  - Good Linearity, Fair Dynamic Range
  - Good Timing Resolution
  - "Potential" for Good QE (20% → 40% → 60%)
  - "Potential" for Cheap Production (Hamamatsu: ~$100/mm^2)
  - Large Arrays, Direct Integration of Electronics Possible
- **Not-So-Nice Features:**
  - Dark Current Rate is Significant
    → Needs Cooling, or Coincidence Trigger, or High Thresh.
  - Optical Crosstalk Potentially a Problem
  - QE Needs Improvement (Hamamatsu: ~80%, but PDE ~40%)
  - No Dynode for Trigger

→ Not Quite in Production Yet…
Samples Now, Production '07

Summary of 2006 IEEE NSS

- 45 Sessions, Including:
  - (4) Dedicated Sessions on Custom Circuits
    - (3) Oral Sessions, (18) Talks
    - (1) Poster Sessions, (24) Talks
  - (8) Dedicated Sessions on Semiconductor Detectors (All Types)
    - (5) Oral Sessions, (32) Talks
    - (3) Poster Sessions, (44) Talks

- Specific Subject Areas:
  - (31) Talks on New Custom Chips
  - (12) Talks on Silicon PM's, + Hamamatsu "Announcement"
  - (30) Talks on New Silicon Strip or Pixel Detectors
  - (4) Talks on APD's
  - (6) Talks on 2D/3D Detectors

Conclusions

- **Active Detector R&D Programs in Many Technologies**
  - HEP R&D Being Driven by the ILC
  - Many Innovative Ideas being Pursued
  - Many Groups Active World-wide, in Development & Evaluation
  - Quite an Exciting Time for This Area

    → ***Many Fields Can Benefit from this Development Activity***

- **Still Too Early to Tell Which Technologies Will be Viable**
  - Many Innovative Ideas being Pursued

    → ***With New Approaches, Need to Choose Technologies Carefully***

- **General Trends:**
  - Smaller Feature Sizes
  - Emphasis on Monolithic and Semiconductor Technologies
  - High Channel Count
  - High Degree of Electronics Integration → ***ASICs***

- **Photodetector R&D at ANL HEP:**
  - MAPMTs are Friendly & Familiar; Need Better QE, & Uniformity
  - MCPMTs Great for Fast Timing; Need Additional Study
  - SiPMs Promising; Noise, Recovery, & Production Issues