

A New High-Speed Pattern Recognition Trigger for Ground-Based Telescope Arrays Used in Gamma Ray Astronomy

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Abstract— Modern imaging atmospheric Cerenkov telescopes (IACTs) are often configured as an array of individual telescopes, each having 500 pixels or more, where stereoscopic views of gamma ray air showers using two or more telescopes operating in unison improve the measurement of the location of the source in the night sky. The gamma-ray showers of interest have significant backgrounds, including cosmic-ray showers from protons and heavier elements, muons, and fluctuations in the night sky background that generate noise events in the photodetectors. It is desirable to lower the thresholds on individual pixels, as this reduces the energy threshold of the instrument and facilitates observation of more distant cosmological objects. However, lowering the threshold also increases the noise and background rates. System aspects ultimately determine how low the threshold can be, including the depth of memory in the front end electronics, the speed of the data acquisition, and the sophistication of the trigger. Gamma-ray showers have a distinct but not unique signature compared to the background signals. We have developed a three-stage, high-speed trigger that can recognize patterns from gamma-ray showers and correlate them across all telescopes in the array to form a stereoscopic real-time pattern recognition trigger. Our goal is to process the ~10 MHz individual pixel rate on 500+ channels of each telescope (Level 1), and produce a camera trigger rate of 10 MHz (Level 2), and an array trigger rate of less than 1 kHz (Level 3). This is a significant increase in performance over current IACTs that operate typically at a 1 kHz Level-2 and at 300~Hz event acceptance rate. We describe the architecture of this new sophisticated trigger, present first measurements of the prototype system, and describe plans to test this system in an existing IACT as a proof of principle for a future IACT array that might consist of hundreds of telescopes.

I. INTRODUCTION

The field of gamma ray astronomy using ground-based telescopes has made exciting discoveries since the late 1980's when the Whipple collaboration made the first unequivocal detection of the Crab Nebula [1]. The instrumentation and analysis techniques of these imaging

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atmospheric Cerenkov telescopes (IACTs) have become highly sophisticated, and there now exists several around the world, including H.E.S.S. [2], MAGIC [3], and VERITAS [4]. The results of these experiments suggest that the night sky is rich in TeV gamma-ray sources. More than 70 sources have been discovered to date, including supernova remnants, pulsar wind nebulae, x-ray binaries, active galactic nuclei and “dark sources” with no known counterpart at other wavelengths. Improvements in sensitivity will almost certainly yield many more.

Current IACTs generally use an array of individual telescopes, typically between two and four, and make use of stereoscopic imaging techniques to improve the identification and location of sources in the night sky. The VERITAS array has four telescopes, each of which has a camera that consists of order 500 pixels, implemented using 1-1/8" photomultiplier tubes (PMTs). When a gamma ray interacts in the earth's atmosphere, it produces an air shower that emits Cerenkov light. The light is focused onto the telescope cameras, where the images appear as tightly-formed ellipses. The intersection of the major axes of these ellipses is used to determine the arrival direction of the gamma-ray primary. See Fig. 1.

While the technique works well, there are significant backgrounds. Cosmic rays also produce showers, but the images are generally less-well defined and more chaotic in nature. Muons produce images that appear as rings and arcs, which can also be confused with gamma-ray showers. Noise from night sky background fluctuations can also appear as a small number of hit pixels, isolated spatially and temporally. Current IACT trigger systems typically trigger on a multiplicity of grouped pixels above threshold in a small time window, with event identification done off-line. This penalizes the measurement in terms of efficiency and dead-time. As the energy threshold is lowered, the background rates increase. This can stress an instrumentation system to limits that make lower energy measurements impractical. Factors include finite depth of memory in the front end ends for holding events pending a trigger, the digitization speed, readout-speed, and dead-time. It is desirable to be able to control the acceptance of gamma ray events at the trigger level.

The current generation of IACTs operates efficiently with energy thresholds in the TeV energy regime, down to 100-200 GeV. However, observation of the more distant objects of interest requires energy thresholds in the 20-100 GeV range, which is not easily achieved in the present systems. The use

of a sophisticated, efficient, pattern-recognition trigger can greatly improve the on-line event selection capability, and may allow existing instrumentation systems to operate at lower energy thresholds. Discussion and planning are now in progress around the world to build larger arrays of telescopes, such as AGIS [5], having of order 50-100 telescopes, to further improve angular coverage, sensitivity, pointing accuracy, etc. The capability to perform real-time identification of gamma ray events will be especially important for these larger instruments. In this paper, we present our work on a new technique for implementing a sophisticated pattern recognition trigger that facilitates lowering the energy threshold of the measurements, to achieve observation of objects more distant than can currently be achieved in the current instruments.

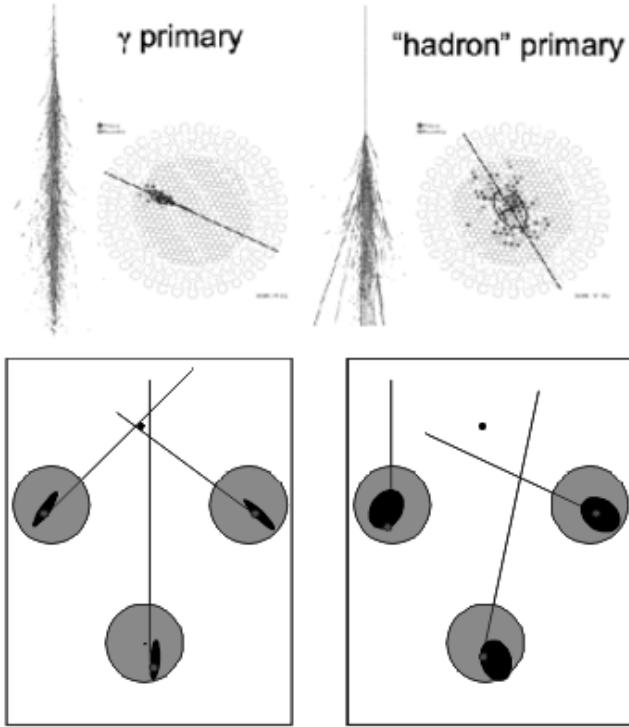


Fig. 1. Illustration of the use of parallactic displacement for hadronic background suppression. The shapes of the electromagnetic component of a γ -ray and a proton induced shower are shown, and the effect on the shape and orientation of Cherenkov light images in the cameras is depicted in a schematic view. The shower core on the ground (black dot in lower figure) for a γ -ray primary can be reconstructed by extrapolation of the line between image centroid and the arrival direction (known point source at center of field of view). Proton showers exhibit on average a large transverse spread limiting the accuracy of the core reconstruction.

II. OVERALL METHODOLOGY

In existing telescopes, a trigger decision is usually achieved in a three step process: first, individual pixels have to exceed a preset threshold typically expressed in photo-electrons. This is generally called the Level 1 (L1) Trigger. Secondly, the gamma ray image topology requires a camera level coincidence between several neighbor pixels. A final and

strong constraint arises from the time coincidence between several telescopes of an array, requiring telescope triggers to occur within 40 - 100 ns of each other.

Our approach in performing a real time image analysis uses the concept of parallactic displacement of Cherenkov light images to discriminate between gamma rays and hadron-induced air showers. Referring to Fig. 1, the basic idea is to calculate the convergence of the lines from the image centroids from each camera, using the discriminated Level 1 signals [6]. The figure of merit, called "parallaxwidth," is defined as:

$$\text{Parallaxwidth} \approx \sqrt{\frac{\sum_{i=1}^n (r_i - \langle r \rangle)^2}{n}}$$

$r_i = \text{location of intersection point } i$

$\langle r \rangle = \text{averaged core location}$

Whereas Cherenkov light images from gamma ray showers point with their major image axis in the direction of the physical shower axis in 3-dimensional space, similar images from hadronic showers exhibit large fluctuations in the light distribution perpendicular to the major image axis. This is due to fluctuations in the hadronic cascade and the large transverse momenta of the neutral pions feeding the electromagnetic component. These fluctuations translate into a large spread in the shower core reconstruction in the telescope plane. The consequences of these fluctuations and their effect on the parallactic displacement of images with application to stereo array analysis were pointed out previously [6].

A topological trigger system based on parallactic displacements of the individual telescope images can provide gamma/hadron separation capabilities at the trigger level while also rejecting single photo-electrons from night sky background fluctuations. A Monte Carlo simulation of the cosmic ray rejection using this technique with an array of 19 10-meter telescopes spaced 60 meters apart is shown in Fig. 2. The method appears to work, providing 90% rejection of cosmic ray events while retaining 90% of the gamma ray events using the parallax width as the acceptance parameter. Our goal is to implement this trigger in hardware, and operate it in real time.

III. SYSTEM ARCHITECTURE

To test this concept, we have designed a trigger system based on the above concepts. We are building a system which we hope to test in one of the existing IACTs, and are assuming default parameters of four 500-channel telescopes. In the description that follows, some of our design choices are related specifically to being compatible with an existing IACT. A further constraint is that our test may not interfere with the normal operation of that experiment. We will identify those aspects in the discussion. However, the basic principles of the architecture are applicable to a larger array, possibly having of order 50-100 telescopes, each of which

may have 10,000 channels. We intend for this work to be a basis for R&D for such a future system.

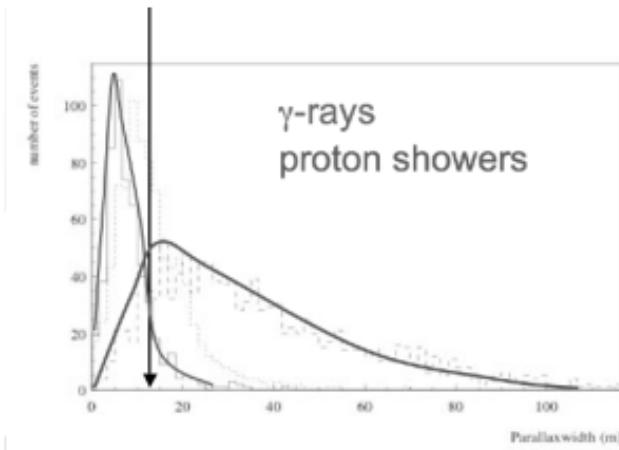


Fig. 2. Result of Monte Carlo simulation of gamma/hadron separation in an array of 20 telescopes using the method of parallax displacement. The result rejects 90% of the cosmic rays while retaining 90% of the gamma ray signals.

A high-level block diagram of the system is shown in Fig. 3. Each camera has local processing of the images that it receives, which includes the calculation of the first and second moments of the image. These results are sent to a central array trigger, which performs the parallax width calculations. When the proper criteria are met, the array trigger sends an accept signal back to the front-ends, to capture and read out the event of interest, which is stored in local front-end pipelines. For our purposes, the accept signal must occur within 64 microseconds of the time of the event.

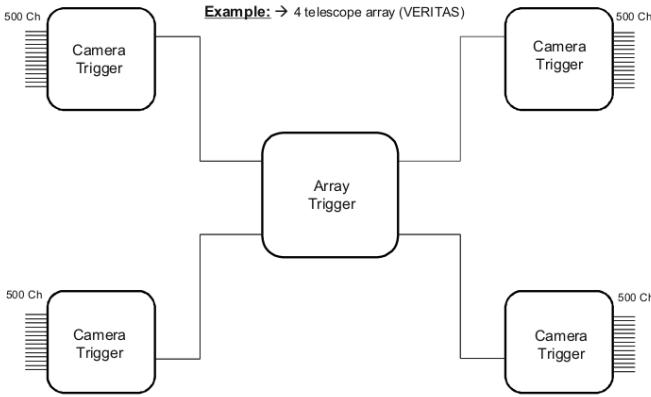


Fig. 3. High-Level block diagram of the trigger system.

Looking deeper, the system that we have designed has three levels of triggering. A block diagram is shown in Fig. 4. Level 1 is the discriminated outputs of the front-end electronics. At low thresholds, the individual pixel rates approach 10 MHz, dominated by single photo-electrons from PMT noise and the night sky background. For a telescope camera having 500 channels, the aggregate Level 1 rate is then of order 5 GHz. The Level 2 trigger does the pattern recognition and centroid calculation processing for each

individual telescope. Our goal is to achieve a 10 MHz output rate from Level 2. This is the most challenging part of the system, as it must process a large number of channels at very high speeds. Note that in our system architecture, we have incorporated an intermediate level of triggering, Level 1.5, to aid in the signal processing. This functionality will be described shortly. Level 3 is the array trigger, receiving results from the Level 2 Processor for each telescope, and performing the parallax calculations to look for correlations. For atypical modern IACT, the maximum Level 3 accept rate is ~1 KHz, but we have set a goal for performance up to 100 KHz for the future applications.

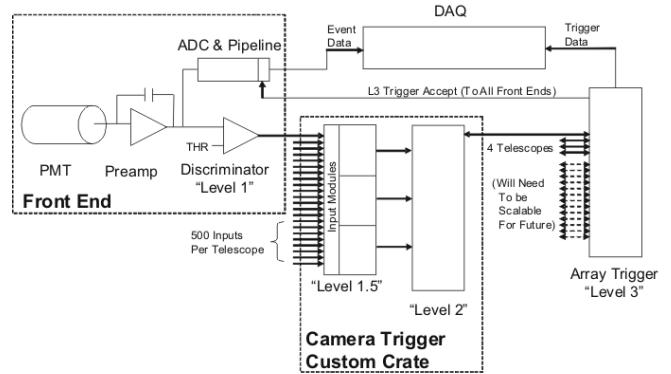


Fig. 4. Block diagram of the trigger and read out system.

The physical configuration for our application is shown in Fig. 5. We assume a 500-channel telescope, and divide it into 3 regions, each of which has a small overlap region with its neighbor. The signals from the front ends are received by I/O Modules that reside in a 9U x 160 mm crate. The input signals are converted to low voltage differential signals (LVDS) on the I/O Modules, and sent across the backplane using point-to-point routing to a corresponding Level 1.5 Processor. The Level 1.5 Processors look for 3-fold coincidence of neighboring pixels in a cell of 7 pixels within a programmable time window, as shown in Fig. 6. When this criterion is met, the pixel coordinates and a timestamp for the event are captured, which are then sent from the three Level 1.5 Processors to a single Level 2 Processor that resides in the crate over point-to-point cable connections on the front panels. The Level 2 Processor sorts the data based on the timestamps, counts the number of pixels hit, and calculates the first and second moments of the hit pixels. This information, along with the timestamp, is then sent to a central Level 3 processor – the array trigger, over fiber some distance away at a data rate of 2 Gbps. The Level 3 Processor then calculates the vector r and the angle ϕ from for each telescope in the array, and then determines the parallax width parameter. If the event is accepted, the Level 3 Processor uses the timestamp to calculate the delay needed in sending the event accept signal to the front ends. The individual components of the system will be described next.

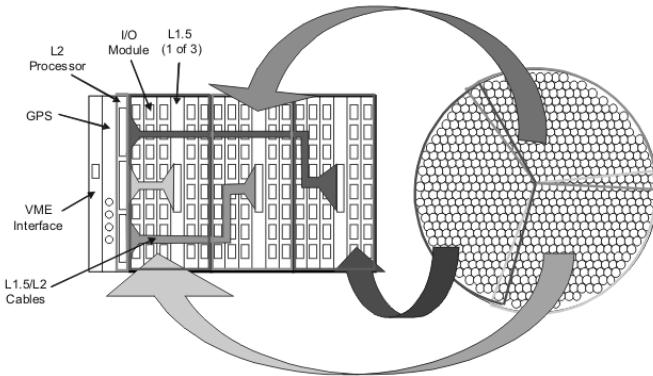


Fig. 5. Physical configuration of the Level 2 Trigger for a 500-channel telescope camera. The camera is divided into 3 regions with small overlaps. Each region is processed separately in a custom Level 2 crate.



3-Fold Coincidence

Fig. 6. Each pixel in the telescope camera forms the primary (center) pixel in a 7-pixel cell. The Level 1.5 Processor contains logic that looks for the center pixel to be hit plus any two neighbors. When this condition is satisfied, the addresses of the hit pixels are saved for further processing. Pixels that reside on the edges of regions are processed specially.

IV. SYSTEM COMPONENT DESCRIPTION

A. I/O Module

The Level 1 signals in our system are differential ECL signals. The I/O Module has an input and an output for these signals, through which ECL receivers can spy on the signals. This allows the existing Level 2 system of the experiment may operate autonomously. The signals come in to the module on one 10-pair connector, are routed to an ECL receiver, and are immediately routed to an output connector so that the existing cabling for the experiment can be used. A block diagram of the card, and a picture of the module, is shown in Fig. 7. There is no termination on the ECL lines on the I/O Module, and careful layout techniques are employed to ensure that the 100-ohm characteristic of the input cables is maintained. The input signals are converted to LVDS on the I/O Modules, and sent across the backplane using point-to-point routing to a corresponding Level 1.5 Processor. In order to handle the overlap region, each Level 1 signal is copied twice: once for processing as part of the primary region, and a second time in case that pixel is part of the overlap region. In order to avoid

having customized I/O Modules, we do not identify those pixels that are part of the overlap regions on the I/O Modules; all pixels are duplicated and processed in the same way, so that all I/O Modules can be fabricated identically. The specific routing of signals from the I/O cards to the L1.5 Processor is handled on the backplane, which is described next.

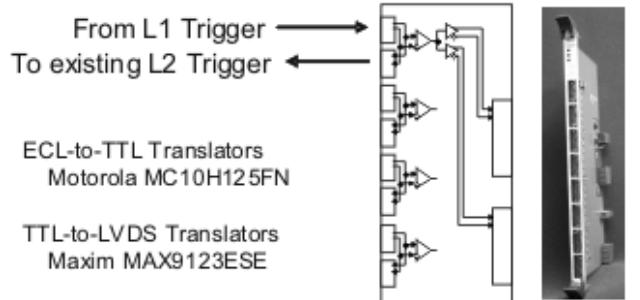


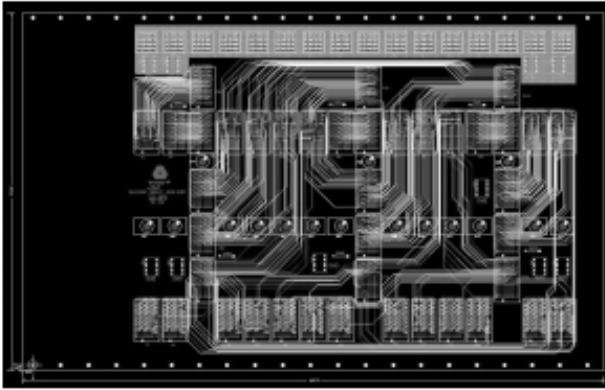
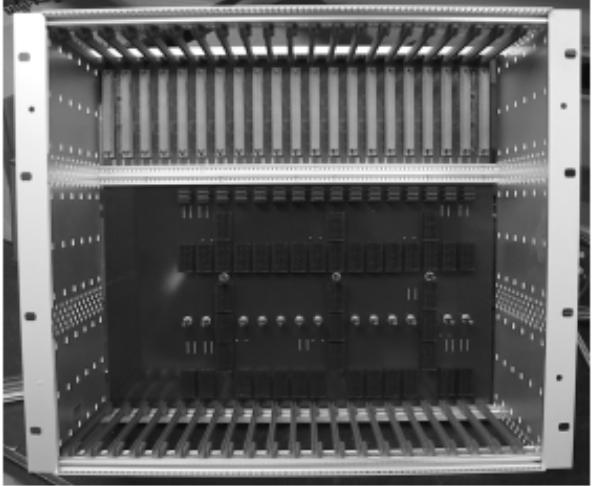
Fig. 7. I/O Module block diagram and picture.

B. Custom Crate and Backplane

The crate that we have designed is 9U x 160 mm. It is a hybrid design, which uses a commercial VME backplane for J1, and a custom design for the J2-J3 portion. The J1 VME is used to access the Level 1.5 and Level 2 Processors in the crate, primarily for setup configuration and diagnostics. The J2-J3 backplane is custom, and handles the point-to-point routing of signals from the I/O Modules to the respective Level 1.5 Processors. A picture of the crate, along with a graphic of the layout of the J2-J3 backplane, is shown in Fig. 8.

As mentioned earlier, each L1 signal is copied to the backplane twice – once for the primary region, and once “in case” that particular pixel is part of the overlap region. It is on the backplane where the decisions were made as to which signal was part of an overlap, and which were not. In the case where a given signal is part of an overlap region, the second copy is routed to the neighboring processor. Otherwise (which is the case for most of the pixels), the signal is terminated using a resistor that is added to the back side of the backplane. While this results in wasted power in the crate as well as higher costs in unneeded circuitry, it made the I/O Module easy to design and manufacture, and it was a conscious design decision to solve the problem in this way.

The connections to the J2-J3 backplane use high-performance MultiGIG connectors to transmit the high-speed LVDS from the I/O Modules to the respective Level 1.5 Processors. These connectors are specified for 3 Gbps performance, and are ideally matched for the ~2 nS timing precision that we require for the processing of the Level 1 signals. Extreme care was taken in the design of this backplane so that the signal integrity of these high-speed signals was not spoiled, maintaining 100-ohm characteristic impedance, with no vias other than at the source and the destination.



10-Layer Circuit Board Layout of Backplane

Fig. 8. Picture of the crate, and a graphic of the layout of the J2-J3 backplane. The crate uses Multigig connectors for the high-speed signal transmission.

C. Level 1.5 Processor

The Level 1.5 (L1.5) Processors receive the Level 1 signals from the backplane. Each receives a unique set of signals from the camera, approximately 180 signals each, corresponding to the pixel map shown in Fig. 5, with only the overlap pixels shared between different processors. The signals are received and processed by a Xilinx Virtex-5 Field Programmable Gate Array (FPGA), model XC5VLX50, running at 400MHz. In the FPGA, each pixel is stretched by a variable width one-shot, from ~ 4 nS up to 40 nS, before entering the pipelined coincidence logic. The algorithm first registers the signals to the 400 MHz clock, and process them looking for the 3-fold coincidence of neighboring pixels as described earlier. Each pixel is processed as a primary (center) pixel in a cell of 7 pixels (see Fig. 6), and also as a secondary pixel in up to six neighboring cells. When the coincidence criterion is met, the L1.5 Processor latches all pixels that become active during the next few time slices following the coincidence. This provides a variable width acceptance window to allow for pixels that arrive slightly later than the others, depending on the nature of the wave front, night sky background, etc. The processor also latches a 32-bit

timestamp along with the active pixels. The latched pixel bit pattern and timestamp are stored in an event FIFO. When the FIFO becomes not empty, the active bits in the bit pattern are converted to virtual pixel addresses, which are then sent to the Level 2 Processor, along with the timestamp. The transmission is accomplished using a ribbon cable across the front panels, operating at 50MHz.

The 400 MHz clock is created internally by the Xilinx Digital Clock Manager (DCM) from a 50MHz source distributed in phase to each L1.5 Processor by the Level 2 Processor. The timestamps are synchronized not only across the three L1.5 Processors, but across the system as well, and are used by the Level 3 Processor later on to bring the event fragments together from across the system. The timing system is described later. A block diagram and picture of the L1.5 Processor are shown in Fig. 9. A close-up view of the FPGA is shown in Fig. 10. Note that we elected to not use the internal LVDS receivers inside of the Virtex-5, but instead use external receivers. We made this choice since the L1 LVDS signals come in over the backplane, a potentially hostile environment, and we were concerned about potential damage to this expensive FPGA due to mishap. The transmission lines are carefully designed to maintain the 100 ohm impedance, with the signals terminated directly at the receivers.

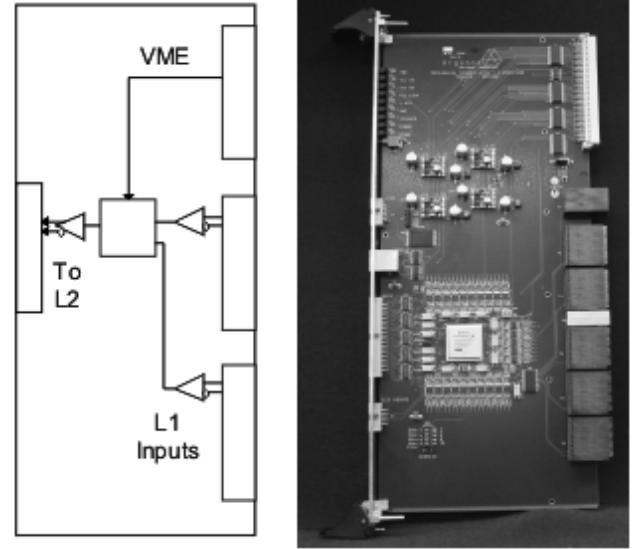


Fig. 9. Level 1.5 Processor block diagram and picture.

The L1.5 Processor has access to the J1 VME backplane. This is used to program setup parameters such as the one-shot width, masking of bad channels, etc. We also plan to incorporate skew adjust for the L1 signals received from the backplane, since the traces have different lengths, and we seek an accuracy of ~ 2 nS. The L1.5 Processor also has a diagnostic state machine, where data can be loaded that mimics L1 signals, and can operate at 400 MHz. Some of our preliminary test results using this feature will be presented later. Lastly, we have incorporated a diagnostic mode, where results from the L1.5 processing can be stored in an on-board memory that is accessible from VME.

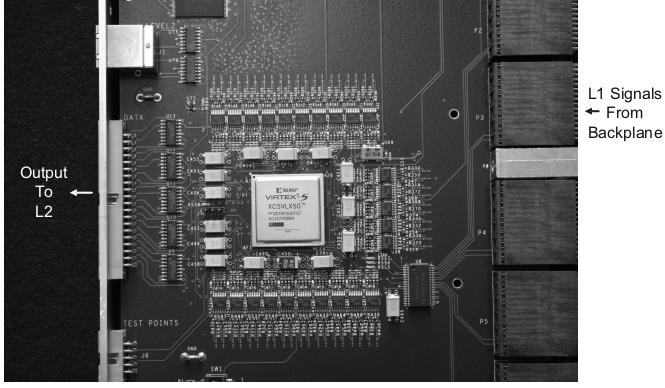


Fig. 10. Close up view of the FPGA used on the Level 1.5 Processor.

D. Level 2 Processor

Data from the L1.5 Processor is received by the Level 2 (L2) Processor via the front-panel connections, and is stored in internal buffer FIFOs implemented within a Xilinx XC4VLX40 FPGA. This FPGA contains 18,432 logic slices and can implement up to 288kbits of RAM. Multiple 48-bit DSP logic blocks are available for numeric processing. Logic clock rates in excess of 200MHz are easily achieved. Each L1.5 Processor sends lists of hit pixels when an event occurs, along with a timestamp for the event. Note that once the data is time stamped, the system allows latencies and fluctuations in later processing (within limits.) The L2 FPGA collects the list of all pixels whose timestamps fall within a programmable range and converts all pixel numbers to X-Y coordinates using lookup tables. A pipeline sums all the pixels together, forming the moments traditionally used in linear regression analysis (sum of X, sum of Y, sum of X-squared, sum of Y-squared and sum of X*Y). After counting how many pixels were in the event, a data record of the moments, plus the timestamp associated with the event, is transmitted over a 2Gbps fiber optic link to the L3 Processor where the data is merged with that of other L2 Processors. The fiber optic link is bi-directional. The link from L3 to L2 provides the reference clock, the once-per-second synchronization pulse to reset the timestamp counters in the L1.5 Processors, and allows for distribution of commands including error detection and system reset. A picture of the L2 Processor is shown in Fig. 11.

The L2 Processor receives and re-distributes the master 50MHz clock to the three L1.5 cards that share the same crate. The clock may either come from the fiber optic link from Level 3 or may be synthesized from the 10MHz output of a GPS receiver connected to the front panel. A phase-locked-loop clock distribution chip with skew control allows for compensation of delays so that all L1.5 Processors within a crate are matched in phase. The physical connection between L1.5 and L2 consists of a four-pair RJ45 cable for the clock distribution plus a 20-pair short ribbon cable for the pixel data. A 1 Hz synchronization signal is sent from L2 to all L1.5 Processors for timestamp synchronization.

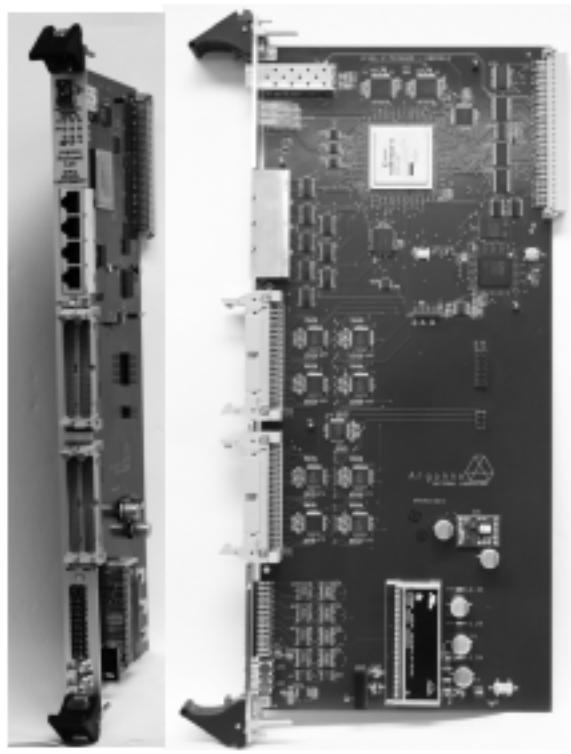


Fig. 11. Pictures of the Level 2 Processor.

Like L1.5, the L2 Processor also has access to the J1 VME backplane. This is used primarily to load a diagnostic state machine, where data can be loaded that mimics L1.5 input data. As was done in the L1.5 Processor, the L2 also has a diagnostic mode, where results from the L2 processing can be stored in an on-board memory that is accessible from VME.

E. Level 3 – The Array Trigger

For our present purposes, we are implementing the Level 3 Processor using a commercial PCI card from Faster Technology, Model P6 [7]. The card has four fiber SFP optical transceivers, and is ideal for our demonstrator application where we ultimately will process triggers from the four telescopes. It has an SATA channels through which the L3 Accept signals can be fanned out to the front end electronics. A picture of the card is shown in Fig. 12.

The card implements logic in a Xilinx Virtex-4 FPGA, model XC4VFX60. Data records received from multiple L2 cards are used to calculate a projected point in space based upon the known position of the telescopes. If the set of records within a timestamp range from multiple L2 cards all point to the same place, the event is assumed to have been generated by an atmospheric Cherenkov event; if the projections do not form a consistent result the event is rejected. The telescopes all have digitizers with a pipeline for storing the data pending a trigger decision. The buffer depth is sufficiently long to allow for the calculation time within L3. Should an event be accepted, the average timestamp value of those received from the L2 cards is placed within a register. When the L3 timestamp counter matches that register value the trigger signal is sent to the digitizer buffers to save

that event for further analysis. This allows for variable L3 processing time, so long as the maximum time is not exceeded.

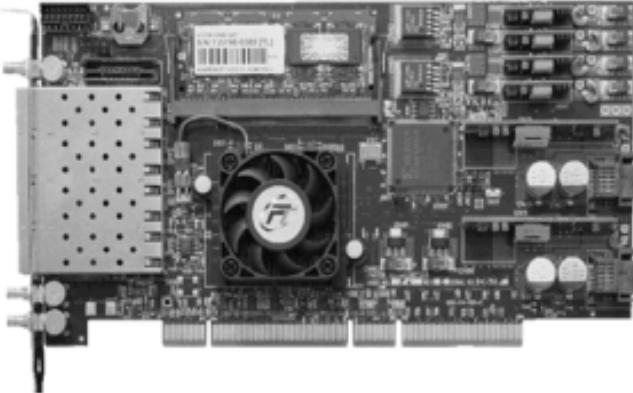


Fig. 12. Picture of the Level 3 Processor from Faster Technology.

V. PRELIMINARY RESULTS

We have assembled prototypes of each component in the system, and have begun the process of debugging and test measurement. Our test stand is shown in Fig. 13.

To date, we have performed two important tests of the system. The first was to drive fast differential ECL signals into the I/O Module, and look at the signal integrity as received by the L1.5 processor after the signals travelled across the backplane. A picture of the signals from a scope trace is shown in Fig. 14. The rise time is approximately 1.6 nSec, nearly the same as our driving source. The ringing is minimal, and there was no sign of impedance mismatches.

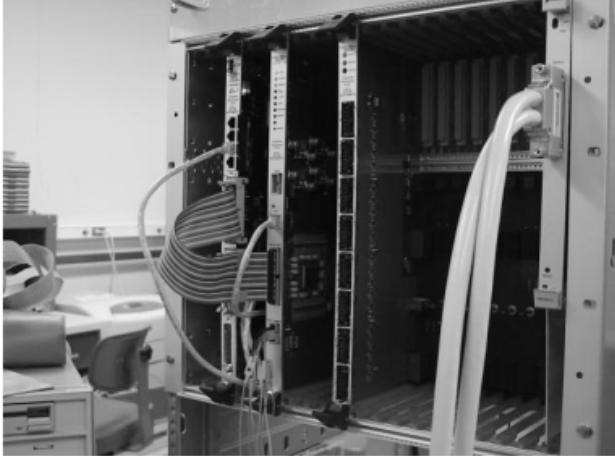


Fig. 13. Picture of the test stand at Argonne.

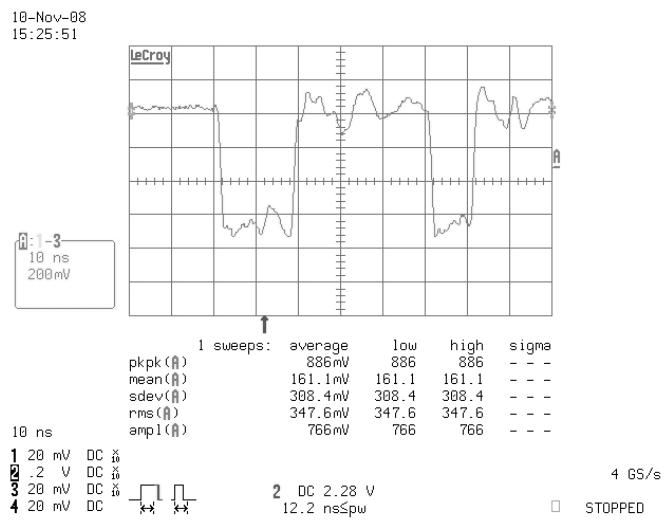


Fig. 14. Scope trace of the LVDS L1 signals, sourced from the I/O Module, and received on the L1.5 Processor.

In the second test, we operated the state machine on the L1.5 Processor at 400 MHz, loading in patterns that contained random isolated hits, along with patterns that would satisfy the 3-fold coincidence criteria. We configured the FPGA so that we could see the coincidence signal on an output pin. The result of this test is shown in Fig. 15, which is a screen capture of a logic analyzer. The picture shows the coincidence of three neighbor pixels, and the resulting coincidence signal as generated by the FPGA. We have run the pattern in a loop for several hours, and observed no errors.

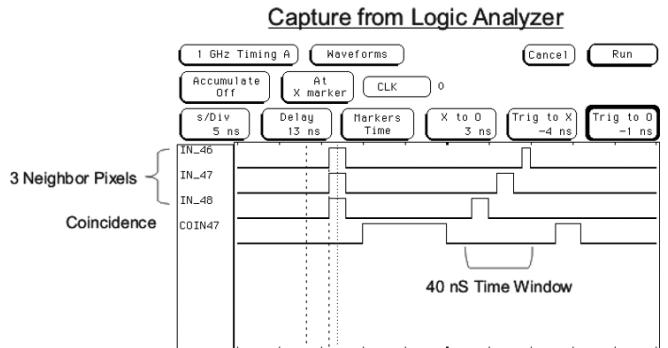


Fig. 15. Screen capture from a logic analyzer showing the coincidence of three neighbor pixels and the resulting coincidence signals generated by the FPGA.

VI. SUMMARY

We are building a sophisticated pattern recognition trigger for use in ground-based gamma ray telescope arrays. While we are just beginning our debugging and commissioning and have a long way to go to demonstrate the capabilities of this trigger, our simulations suggest that this technique and implementation will offer a significant performance over that of current IACT trigger systems. Our immediate plans are to complete the debugging of the prototypes that we have built, and to continue to develop the firmware. We will then continue building the components to instrument an entire

Level 2 Trigger crate. We plan to propose the testing of the system in one of the existing IACTs. We look forward to publishing the results of this work in future proceedings.

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