

Design Report
“A Fast Topological Array Trigger
For Real Time Analysis of
Nanosecond Time Scale Phenomena”

K. Byrum, J. Dawson, G. Drake, C. Duke, W. Haberichter, D. Horan, A. Imran, F.
Krennrich, A. Madvahan, M. Schroedter, A. Smith

1. Abstract

This document describes the design of a topological array trigger for a future imaging atmospheric Cherenkov telescope array system. Most of the layout of individual components have been completed and the purpose of this document is to evaluate the design before the production of boards will be approved. This report gives an overview of the ideas, the designs and the layout of a proof-of-principle system that will be built to test the performance of the real time stereoscopic imaging analysis to form an array trigger decision. We intend to field test the system at the VERITAS observatory.

Contents

1	Introduction/Overview	2
2	Physics Motivation	3
3	Concept: Real Time Stereoscopic Imaging	7
4	Trigger Rates	8
5	General Design Specifications	10
5.1	Camera Trigger Specifications	11
5.2	Array Trigger Specification	12
6	Overall Implementation	13
7	Camera Trigger Design	15
7.1	I/O Cards	15
7.2	L1.5 design	17
7.3	L2 design	19
8	Array Trigger Design	21
8.1	L3 design	21
8.2	Solution A: Custom protocol and data push driven L2 - L3 communications:	22
8.3	Solution B: PCI bus protocol and data push or poll driven L2 - L3 communi- cations	23
9	Appendix A: Algorithm	26
10	Appendix B: Technical Details	28
11	References	29

1 Introduction/Overview

This document describes the motivation, the concept, the design and specifications for a topological array trigger. This system will be built on state-of-the-art FPGA technology and our primary initial scope of this project is to build and test a proof of principle system. This includes tests in the laboratory and field tests in the VERITAS telescope array. We are also cognizant of possible implementations of this instrument in a next generation gamma-ray telescope, such as AGIS (Advanced Gamma ray Imaging System) where a high clock frequency (400 MHz), a large number of pixels, a low cost per channel and an easily scalable design are relevant considerations.

The scope of this project is defined as follows:

- design, built and test a camera pattern recognition camera trigger that calculates properties of Cherenkov light images in real time at a clock frequency of 400 MHz for making a subsequent array trigger decision at the array level within a few microseconds.
- design, built and test an array (Level-3) trigger that processes image properties of a Cherenkov telescope array and performs a stereoscopic analysis within a few microseconds for generating a trigger decision.
- design and built all boards as described above so that they are suitable for field testing on VERITAS. This includes a fast optical fiber communication link between the Level-2 and Level-3 trigger.
- Evaluate and measure the efficiency of the topological trigger for night sky background reduction, cosmic-ray rejection and for lowering the energy threshold of imaging atmospheric Cherenkov telescope arrays.

The scope of the project described here is stage-1 of the development of a topological trigger system. Stage 1 will lead to a proof-of-principle system and tests of the individual components. A full prototype system with four camera trigger systems and a fully implemented array trigger is subject to further consideration for funding. However, we will discuss the general considerations for a complete topological array trigger system in this document.

2 Physics Motivation

Gamma Ray astronomy with ground-based telescopes has made dramatic advances over the last decade with the detection of more than 50 astrophysical gamma-ray sources at TeV energies. The primary technique in this field uses imaging atmospheric Cherenkov telescopes (IACTs), which measure the Cherenkov light produced from interactions of gamma-rays in the upper atmosphere. The current generation of IACTs are able to observe gamma rays of 100 GeV - 100 TeV from galactic and extragalactic sources with large photon statistics and perform high quality spectroscopic, temporal and morphological studies. Observations with these instruments address many of the key science questions in High-Energy Astrophysics, Astroparticle Physics, Particle physics and Cosmology. Specific topics include: Understanding the accretion processes onto a supermassive black hole, jet formation and what is the nature of cosmic accelerators (HE Astrophysics/Astroparticle Physics), what is dark matter (Astroparticle Physics, Particle physics and Cosmology), and what is the cosmic history of star and galaxy formation (Cosmology).

A key technology driver for the future of this field is to expand the IACT technique to energies below 100 GeV, perhaps as low as 10 GeV. This largely uncharted territory¹ can be explored with the highly sensitive IACT detection technique with collection areas the size of a football field. A first step could be to expand the sensitivity of existing instruments down to 50 GeV. This would constitute a breakthrough as the opacity of the universe to gamma rays arising from cosmic infrared background drops rapidly below 100 GeV. As a consequence, the number of extragalactic sources is expected to dramatically increase. The success of this expansion in energy would have strong implications for cosmological studies using active galaxies and Gamma Ray Bursts (GRB): a detection of a GRB afterglow at 50 GeV would be a major discovery, the detection of jets from active galactic nuclei at redshifts of $z=1-2$ would allow us to study supermassive black holes, their evolution and formation history. The use of gamma ray sources as cosmological probes also provides a test of the star formation history of our universe and constraints to quantum gravity theories near the Planck energy. As in many other recent efforts in observational astrophysics, the ability to see further back in time (to higher redshifts) is critical to understanding cosmological source populations, the history of our universe and for discovery potential of all related subjects including dark matter and dark energy.

This work seeks to develop a technique using state-of-the-art field programmable gate arrays to dip into this new energy regime with existing arrays of IACTs. This technology would also facilitate the goal of reaching the 10 GeV regime with future arrays, a photon energy at which the universe is transparent. We have started to design a prototype of a fast topological pattern trigger using field reprogrammable gate arrays (FPGAs). While this technique has been used in HEP experiments for some time, the significant challenge in this application is that the data processing speed must be on order of 400 MHz. This is an order of magnitude faster than state-of-the-art HEP triggers, clearly putting the technology

¹HESS and VERITAS have an energy threshold of 100 - 200 GeV, MAGIC has its peak sensitivity around 180 GeV, much higher as previously intended! Satellite based pair conversion telescopes are photon count limited by their small collection area of less than 1m².

and engineering component of this work at the cutting edge. The immediate beneficiaries of this development would be imaging detectors which rely on off-line analysis to extract signal from measurements that are dominated by background. This trigger development is a cost effective method of significantly lowering the energy threshold of IACT arrays. Other ideas involve substantially larger telescopes, going to high altitude sites and high quantum efficiency photodectors. A combination of these concepts are likely to become an integral part of next generation instruments. The trigger development could be done within 2 years time.

Fast Cherenkov flashes from air showers lasting 5 - 30 ns are used to detect gamma rays at Very High Energies (0.1 - 10 TeV). This technique has been greatly advanced with imaging telescopes over the last 15 years. More recently the use of stereoscopic arrays using telescope coincidences and stereoscopic views has played a key in improving the sensitivity. In addition it will be possible to substantially reduce the energy threshold of these arrays by making trigger decisions based on the stereo view. In order to achieve this, a fast topological trigger with the capability of carrying out a basic stereo image analysis in real time is required and promises to provide:

- a substantially (factor of 2 to 3) reduced trigger and detection threshold
- a substantial reduction of cosmic-ray background event rate
- a large reduction of accidental rate from the night sky background
- operation of IACTs optimized for different observing modes/targets
- the flexibility to add physics trigger modes running in parallel, e.g., microsecond bursts²

The morphology of typical hadron and gamma-ray initiated air showers at VHE energies differ substantially with regard to their lateral and longitudinal particle distributions. The resulting Cherenkov light image properties are the basis for an array trigger that reaches a decision based on the parallactic displacement of the Cherenkov light flashes at different viewpoints. This trigger could be used to suppress a large fraction of cosmic-ray background showers and reduce the chance coincidences from night sky background fluctuations by 3 orders of magnitude, hence lowering the trigger threshold and improving the low energy response substantially.

Figure 1 illustrates the basic idea of using the parallactic displacement of Cherenkov light images to discriminate between gamma-ray and hadron induced air showers utilizing the different viewpoints in an IACT array. Whereas Cherenkov light images from gamma ray showers point with their major image axis in the direction of the physical shower axis in 3-dimensional space, the Cherenkov light images from hadronic showers exhibit large fluctuations in the light distribution perpendicular to the major image axis. This is due to fluctuations in the hadronic cascade and the large transverse momenta of the neutral pions feeding the electromagnetic component. These fluctuations translate into a large spread in the shower core reconstruction in the telescope plane. The consequences of these fluctuations and their effect on the parallactic displacement of images with application to stereo array analysis were pointed out by Krennrich & Lamb (1995a). They introduced the parameter

²This was first realized in the SGARFACE experiment developed, built and operated for the last three years by the P.I. at the Whipple 10 m telescope (LeBohec, Krennrich & Sleege 2005).

”Parallaxwidth”, that is a measure of the spread in the reconstructed shower core location³.

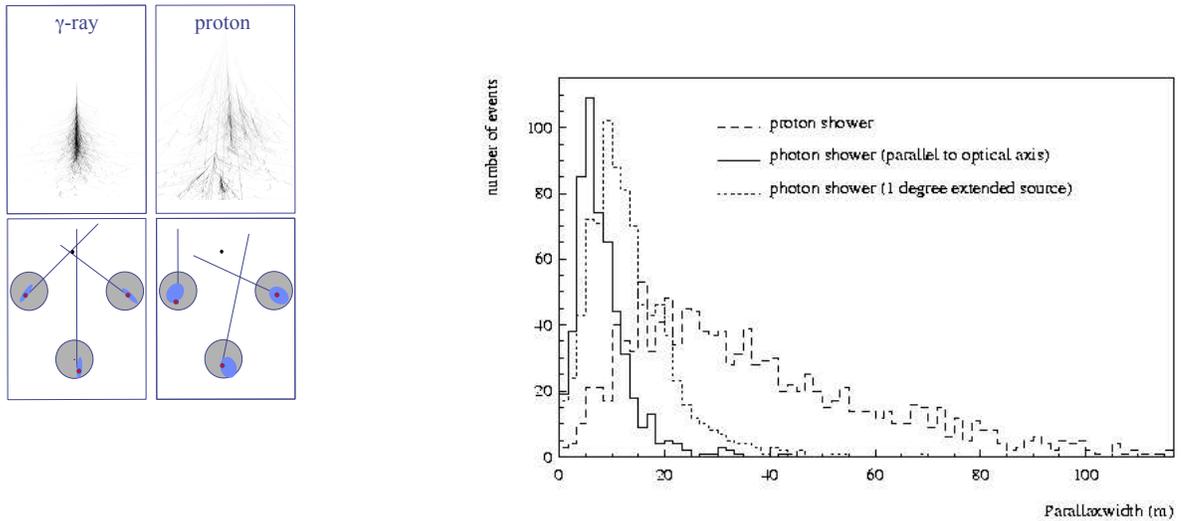


Figure 1: **Left** - Illustration of using parallactic displacement for hadronic background suppression. The shapes of the electromagnetic component of a gamma ray and a proton induced shower are shown, and the effect on the shape and orientation of Cherenkov light images in the cameras is depicted in a schematic view. The shower core on the ground (black dot in lower figure) for a gamma-ray primary can be reconstructed by extrapolation of the line between image centroid and the arrival direction (known point source at center of field of view). Proton showers exhibit on average a large transverse spread limiting the accuracy of the core reconstruction. **Right** - The Parallaxwidth distribution events in an array of 19 telescopes is shown for gamma-ray (solid line) and proton (dashed line) induced showers. Also gamma-ray showers for an extended gamma-ray source is shown (dotted line). These results are based on array configuration with an average of 4-5 telescopes participating in the reconstruction.

Figure 2 shows the Parallaxwidth distribution for simulated 80 GeV gamma-ray events and proton showers sampled from a cosmic-ray spectrum. The average number of telescopes participating in the reconstruction is between 4 and 5, showing that arrays of 4 telescopes are sufficient to make use of this technique (for further details see Krennrich & Lamb 1995b). The separation power can be expressed in the figure of merit, the Q-factor⁴: the application of Parallaxwidth for 80 GeV gamma ray showers gives a Q-factor between 2 and 3 depending on the number of telescopes used. This directly translates into sensitivity improvement. It is apparent that the reconstruction of the shower core requires at least two telescopes, however, with three telescopes the core reconstruction is overconstrained, providing the spread in its estimation. Those telescope coincidences using the parallactic displacement also allow the

³(Parallaxwidth = $\sqrt{\sum_i \frac{(r_i - \bar{r})^2}{n}}$, with $r_i - \bar{r}$ = distance between individual intersection point i from averaged intersection point, n = number of intersection points.)

⁴ $Q = \frac{\epsilon_\gamma}{\sqrt{\kappa_{\text{hadron}}}}$, with ϵ_γ = gamma detection efficiency, κ_{hadron} = hadron detection efficiency.

rejection of accidentals from night sky fluctuations randomly occurring in the field of view.

Utilizing parallactic displacement could significantly advance the IACT technique. There are two key aspects to this technique: reducing the energy threshold of an IACTs array and suppressing hadronic background at the trigger level. Both could lead to a substantial sensitivity/versatility improvement of IACT arrays. For example the low energy mode could be used for the study of gamma ray pulsars and follow-up observations of GRBs, whereas the "low background" mode could be extremely useful for a search for transient phenomena in a fast sky survey mode, making maps of excess events in real time! Also, for large future arrays it is important that the field of view of several tens of telescopes can be spread out so that a combined field of view of the entire instrument can be projected onto the sky, while some field of view overlap provides stereo reconstruction. Once an excess has been detected, the array trigger could be rapidly reprogrammed to point the entire array into this region of the sky probing the phenomenon with maximum sensitivity and lowest threshold. The rapid reprogramming of such an array trigger could substantially enhance the versatility, performance and scientific output of a future array.

Given the threshold energy dependent intergalactic absorption, the different morphology and time scale properties of sources, a versatile trigger that can be optimized for individual observing targets. This makes a fast and intelligent array trigger an important centerpiece of any future IACT array.

3 Concept: Real Time Stereoscopic Imaging

The overall concept of a topological array trigger is outlined in Fig. 2. The system consists of 2 main components: a camera trigger, providing information about the image pattern in the focal plane of an individual telescope. Secondly, a central array trigger or Level-3 trigger unit, that combines the camera patterns and analyzes the image parameters in real time.

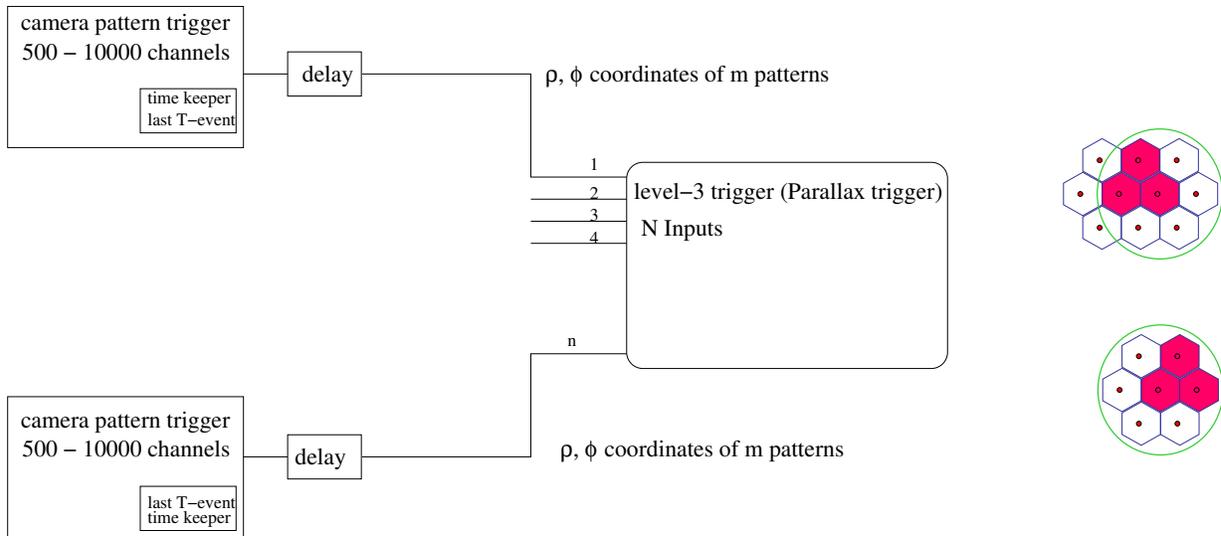


Figure 2: **Left** - The basic structure of a Parallax Trigger/Camera trigger for an IACT array is shown. The camera trigger and the array trigger could be used in any other application using multiple nanosecond imaging systems for combining information for subsequent pattern recognition. **Right** - The pixel algorithm is carried out for each camera pixel requesting that at least two neighbors have also exceeded the trigger threshold.

A camera (Level-2) trigger will be issued once a pixel or more is found to have at least two neighbors (see Fig. 2). The centroid position for each trigger pattern will be calculated and transmitted for further processing in the array trigger. A maximum number of N pairs pixels can be used for the centroid calculation and subsequent processing by the Level-3. We calculate the first moments of images, the number of neighbor pixels and the total number of triggering channels. However, the info for a second moment analysis will also be send to Level-3. A time stamp will be produced locally for each Level-2 trigger so that it can be referenced later to calculate (or adjust) the lookback time for the readout system, after a Level-3 trigger has been issued.

A key input parameter is the trigger rate that will be involved at the camera level of each telescope. The trigger rate of course depends on the number of pixels, field of view and telescope mirror area. However, the shower physics sets a limit to the maximum camera trigger rate.

4 Trigger Rates

The night sky background poses the principal limitation of the air Cherenkov technique and one of the main goals of the topological array trigger to reduce the trigger rates associated with accidental triggers from the night sky. Short time coincidences are effective means to reduce the chance probability for night sky events favoring the shortest possible camera coincidences possible. The Cherenkov light pulse width of 2- 5 ns for gamma ray showers at the lowest energies is one limitation and should be fully explored at the telescope level. At the array trigger level, there are also limitations to the technique of forming stereo coincidences that arise from the physics of air showers. The shower front here defined as the Cherenkov light front is not a plane wave of infinitesimal thickness. The Cherenkov light front has a conical shape and the time dispersion of the individual photons is in the order of several nanoseconds.

Since the shower core location is not a priori known, it is not easily possible to compensate for the conical shape of the shower front and the most conservative approach is to use a gate width that allows for the shower front to fall well within the trigger gate. This results in an array coincidence width of ≈ 40 ns. Therefore, the individual trigger rate from the L2 (camera trigger) cannot exceed 10 MHz or otherwise the L3 trigger resides permanently in a high state.

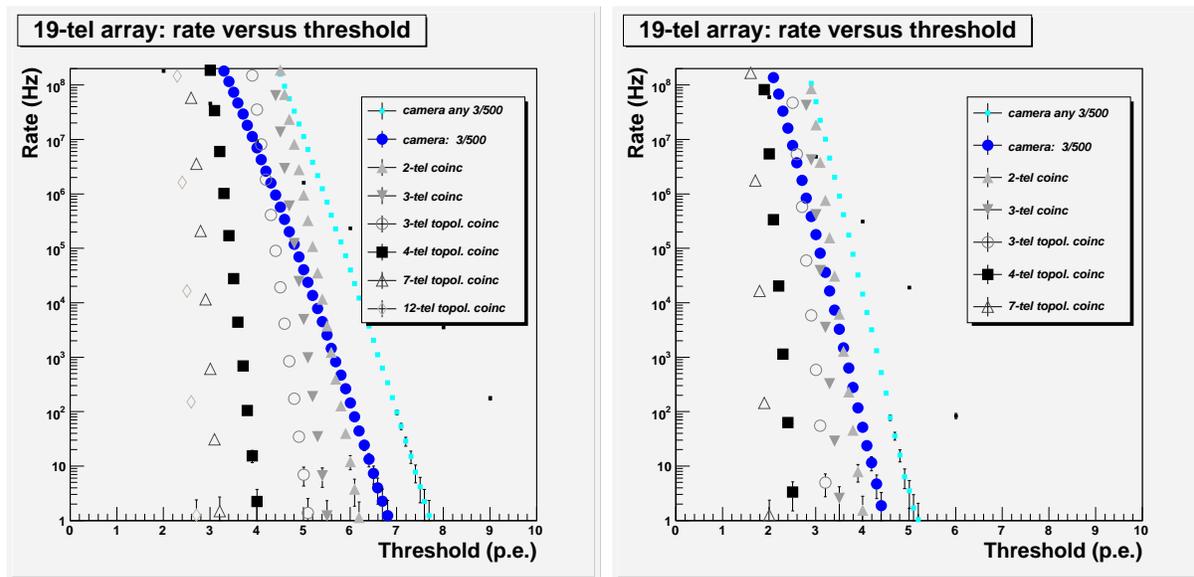


Figure 3: **Left** - The bias curve for a 19 telescope array using various trigger conditions. The camera trigger requiring a 3-fold neighbor criterion is shown with filled circles. The most basic array coincidence requiring two telescopes is shown as filled triangles (upward pointing). **Right** - The same bias curve as before except that the camera coincidence window has been reduced from 7 ns to 2 ns. The topological trigger criterion assumes that the centroids are measured and fall within 0.2 degrees of a projected shower geometry.

Fig. 3 above represent simulated bias curves showing the rate due to night sky as a

function of trigger threshold in photoelectrons. The camera rate should not exceed 10 MHz (blue line) therefore also limiting the array coincidence threshold. A fast camera trigger with 2 ns gate width (figure right) substantially reduces the trigger threshold (left plot uses 7 ns), emphasizing the advantage of a fast pattern trigger when compared to the existing VERITAS system (10 - 13 ns).

It may be possible to reduce the array coincidence width below 40 ns using an L3 trigger that uses a template consisting of relative arrival times and imaging to fit a cone to the Cherenkov light front, at best one might get down to 10 ns or so (needs to be verified!).

The current VERITAS system uses a coincidence gate width at the telescope level of 10 -13 ns. Furthermore, no image information is used at the array level in making an array trigger decision. With the FPGA based pattern trigger the coincidence gate width could be reduced to 4 ns and the event topology could be used to reduce array chance coincidences. As illustrated in Fig. 4, this could lead to a threshold reduction from 6.6 p.e. to 3.4 p.e.. The absolute numbers depend somewhat on the night sky background and assumptions on light collection efficiencies of the telescopes. However, going from a gate width of 10 ns (Fig. 4 left) to 4 ns (Fig. 4 right) combined with a topological trigger, could allow to reduce the trigger threshold by 50%.

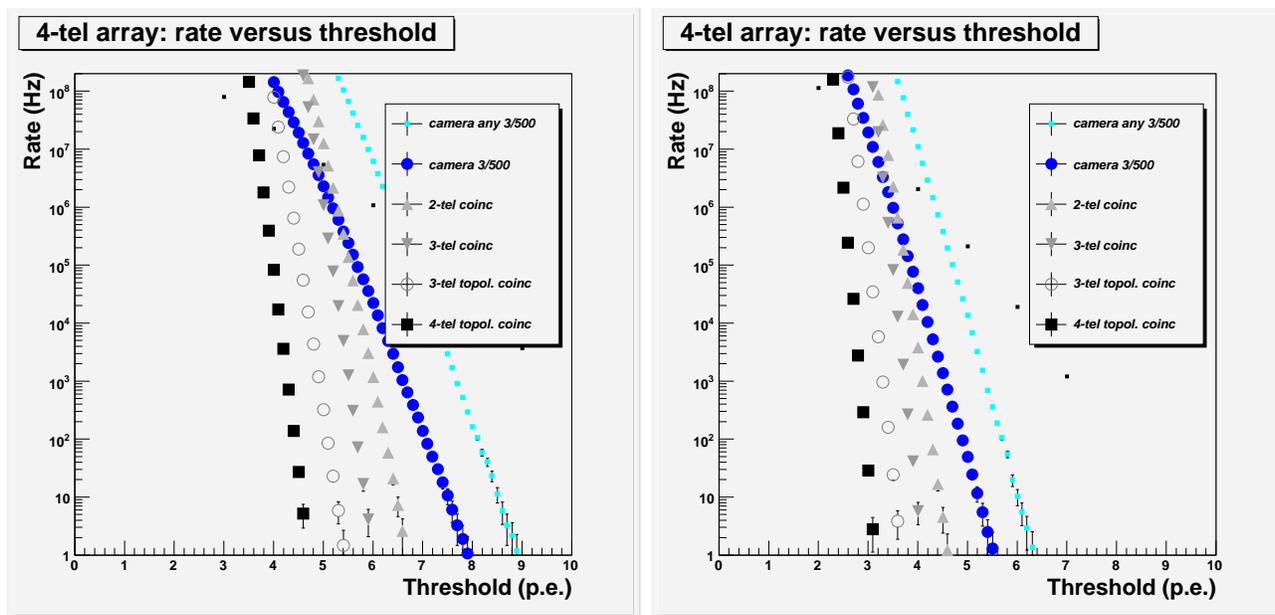


Figure 4: **Left** - The simulated bias curve for a 4 telescope array using various trigger conditions. **Right** - The same bias curve as before except that the camera coincidence window has been reduced from 10 ns to 4 ns.

In summary, two important design specifications arise from the air shower physics and night sky considerations: the camera trigger rate is required to be less than 10 MHz and a camera coincidence gate 2 - 4 ns will be important to reduce the accidentals rate. In the next section we discuss the general design specifications for the trigger.

5 General Design Specifications

The Parallax-Trigger concept will be most effective for a large array of IACTs, where air showers are mostly fully contained within the array boundaries and in the order of 5 - 10 telescopes are available to participate in a local array trigger. The prototype design is for 4 telescopes and can be tested at currently existing telescope array systems. The prototype will consist of 4 identical camera trigger units, one at each telescope, and a centrally located array parallax trigger unit receiving information from each telescope camera trigger. Note that one requires at least 3 telescopes to get a constraint from parallactic displacements of air shower images, and four telescope are required to reconstruct the arrival direction for poorly defined images.

The following specifications are a guideline for the requirements of the camera and array trigger units. The overall design specifications are as follows.

- 500 - 10,000 input channels per camera trigger: It would be desirable to develop a design that can process the order of 10^4 pixels to make it applicable to future arrays of IACTs such as "AGIS". Therefore it is important that the prototype can be scaled up to large numbers of pixels.
- Trigger Decision time $5 - 10 \mu\text{s}$. This is a non-critical specification and must be tuned for a specific application. Modern IACT arrays have trigger latencies on the order of several microseconds. The basic data processing of the trigger will be pipelined, and require some minimum time, depending on the nature and sophistication of the algorithm. This specification sets an upper limit on the processing time. The specification may become critical if the FIFOs or ring buffers used to store the pulse shape information are limited to a few microseconds. Furthermore, one has to be careful when choosing the communications protocol between the L2 and the L3. Only few systems, e.g., 10 GBit Ethernet, and PCIe are suitable commercial networks that can keep the overall latencies to the order of $10 \mu\text{s}$ or less.
- maximum rate of the array trigger with ≥ 3 telescopes participating in the trigger: 10 kHz. This specification is high and therefore uncritical for an array of just 4 VERITAS type telescopes, however, it maybe low for an array of 50 - 100 telescopes or a smaller array of large telescopes, it could be as high as 50 - 100 kHz for a 1 km^2 array. The array trigger design for a very large array will depend on the size of the array and the number of the telescopes and likely be partitioned into sub-array and will be studied separately at a later stage. The prototype to be tested in VERITAS-4 could certainly do with 1 kHz as a maximum rate. After all, we are trying to reduce accidental from the night sky and the cosmic-ray background with this system. Furthermore the data acquisition of VERITAS is limited to a design spec of 1 kHz. The maximum rate of the array trigger will be limited by the trigger latencies of all elements involved. The implication of the maximum array trigger rate of 10 kHz also sets a limit to the time its takes to get a trigger decision: $10 \mu\text{s}$ would be acceptable. However, the maximum

trigger rate will most likely be limited by any data acquisition system to be used in the individual telescopes.

- Data Processing Bandwidth of FPGA logic: ≥ 400 MHz. A Cherenkov light flash from an air shower has a typical pulse width of 4-8 ns and depends on primary energy and shower core location. Isochronous modern telescopes used for IACT arrays achieve better than 2 ns absolute timing resolution, which should be matched by the Parallax-trigger. Such high timing accuracy is useful at the camera trigger level for forming fast coincidences of neighbor pixels and is technologically the most difficult part. At the array trigger level one would still like to maintain this accuracy, however, the air shower physics suggests that array coincidences will be more likely in the 10-15 ns regime.

5.1 Camera Trigger Specifications

With the general guidelines as mentioned above we now turn to the specifications for the camera trigger.

- Maximum input rate per channel: 10-100 MHz. This is motivated due to the fact that a photomultiplier in a typical modern large Cherenkov telescope (100 m² mirror and pixel size 0.15°) has a singles rate from the night sky fluctuations of 1 MHz (4 MHz) at a threshold of 5 (4) photoelectrons. Lowering the trigger threshold to 3 photoelectrons per pixel when using a pixel size of 0.15° would result in a substantial energy threshold reduction of 40%⁵. These numbers are based on a night sky background as is found in a dark location, e.g., at major observatories for optical astronomy (N.S.B = 2×10^{12} photons m⁻² sr⁻¹ s⁻¹ (Mirzoyan et al. 1994). The VERITAS CFDs can handle singles rates of up to 100 MHz. A target number of 100 MHz is useful for exploring the full potential of the array trigger to reduce chance coincidences from to the night sky. High singles rate capability would also allow us to consider a special low energy trigger for part of the camera (using lower CFD settings), e.g., for the central 0.6° around a point source.
- For a possible test of the trigger in VERITAS-4 we will need a Connector splitter/transition box required to go from a 26-pin ribbon cable connector (as provided by the CFD/FADC module) to higher density connector to allow 500 - 1000 input channels for the trigger module. The splitter is also necessary to minimize interference with the standard VERITAS operation.
- Timing precision of the individual camera trigger decision: 1-2 clock periods (2 ns). This is important so that the coincidences can be properly superimposed in subsequent image analysis at the array level. To adjust for delays in the system, an additional delay line should be available for tuning the trigger to the shortest possible gate width.

⁵Note that for different pixel size the absolute value of photoelectrons would change the absolute numbers, but not the effect of lowering the trigger threshold.

- The maximum output rate of the camera trigger should be less than 10 MHz. This would allow one to run deeply into the noise while still avoid saturation of the array trigger. Higher camera trigger rates would lead to substantial deadtime at the array trigger level due to the relatively wide array trigger coincidence window. However, a more sophisticated array trigger algorithm might allow a reduction in the array trigger coincidence gate width and will be explored.

5.2 Array Trigger Specification

- Coincidence gate width for array trigger decision: adjustable between 4-60 ns. Since the shower front of the Cherenkov light is conical and the arrival direction not known a priori, the coincidences from several telescopes may require a wider time window than one would expect from the width of individual Cherenkov flashes. The arrival time of Cherenkov light as a function of shower core distance is shifted by 10 - 15 ns making a gate width of 20 - 40 ns mandatory (Karle 1994).
- The array trigger should be scalable to a large number of telescopes considered in array coincidences. The array trigger should also be able to process several combinations of telescopes in parallel.

6 Overall Implementation

The Pattern Array Trigger will be implemented as shown below in Fig. 5. The signals from the camera are routed to the Topological Trigger Crate at telescope i . The crate contains three kinds of cards: the I/O Cards, which receive and forward the Level 1 signals from the front-end electronics; the Level 1.5 Cards, which process the neighbor logic and look for 3-fold coincidences; and the Level 2 Card (one per crate), which receives all hit pixels associated with a given event that pass the trigger criteria. Each telescope camera trigger unit will be situated in a 9U VME crate housing 9U x 160 mm I/O boards that interface to discriminator signals from the camera pixels. These interface cards (I/O cards) are specific to the VERITAS tests of this proof-of-principle system. The I/O cards are essentially a signal splitter to spy on the VERITAS discriminator signals (CFD signals) for testing and operating the trigger system in parallel to the existing VERITAS camera trigger.

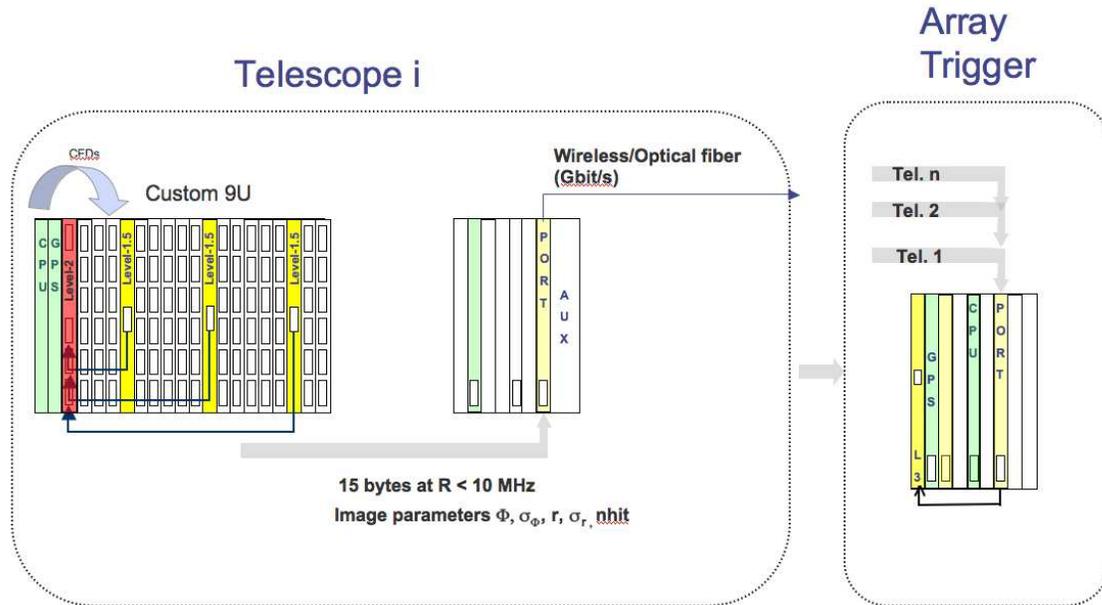


Figure 5: **Left** - The arrangements of modules and crates is shown for a camera trigger. The CFD signals are fed into high density I/O card that distribute the signals to the Level-1.5 cards. The L-1.5 trigger cards receive the CFD signals from approximately 1/3 of the camera (see also Fig. 8) and search for neighbor coincidences including overlapping regions within the 3 sections of the camera. **Right** - The crate containing the L3 trigger is shown.

The CFD signals are then distributed to a set of three separate L1.5 cards which process the neighbor trigger logic. Each L1.5 card can process up to 168 signals which corresponds to about 1/3 of a VERITAS camera with 500 pixels (see Fig. 8). The combination of the three camera regions occurs in the L2 card which makes the final camera trigger decision.

The Level 2 Card (one per crate) receives all hit pixels associated with a given event that pass the neighbor logic criteria from L1.5, and performs calculations to analyze the topology of the hits. The result of these calculations is sent out of the Level 2 Card to a Level 3 processor. The main VME crate or a second VME minicrate also contains a GPS module, which handles the timing needed by the system.

The use of a 2-stage camera trigger with the L1.5 processing sub-regions of a larger camera makes this design scaleable to much larger numbers of pixels while the L1.5 design can be identical and pretty generic cards. The topology of the camera is mapped onto the L1.5 cards by a custom backplane design. The first proof-of-principle system for the VERITAS camera layout has design that is based on a J2 VME backplane with multi-GIG connectors which are suitable for GHz signals. It is important to note that the L2 and L1.5 cards are adaptable to different future telescope designs, the L1.5 cards could be partitioned to a different topology and therefore be integrated into compact cameras designs. The L2 card could either be near the L1.5 cards or be at a different location for final processing. e.g. at the base of a telescope since the pre-trigger information from the L1.5 is transmitted via LVDS. The implementation in Fig. 5 shows the structure for the proof-of-principle system and the possible prototype implementation in VERITAS.

The L2 board communicates via the J1 backplane with a crate computer housed in the main VME crate. A separate VME mini crate is available for testing purposes to house an AUX module that generates trigger patterns. etc. To the right in Fig. 5, the crate is shown for the array trigger logic (L3) and contains an L3 module (PC or FPGA board), a fiber module and a GPS clock. The transfer of L2 triggers, containing 15 bytes of data, could be done by optical fiber or by wireless transmission. We are currently considering both options and further details are given in section 8 describing the array trigger design in detail.

7 Camera Trigger Design

The camera trigger consists of 3 types of boards: the I/O cards, the L1.5 cards and an L2 card. Details of the design of these boards are given in section 7.1, 7.2 and 7.3. Fig. 6 shows the functional diagram of the L2 trigger. Communication to the crate computer and L2 is also established by ethernet. The CPU will be able to write hit patterns to the L2 module directly (selfcheck for debugging L2 when deployed at a telescope), read the camera trigger info generated by L2 (R, phi, nhit, time stamp) and enable/disable L2. Furthermore, we need to have the capability to read array triggers as they are send back including information about the individual telescope triggers. This will facilitate the debugging of array events, e.g., to test whether the correct time stamps of the camera triggers are send back correctly.

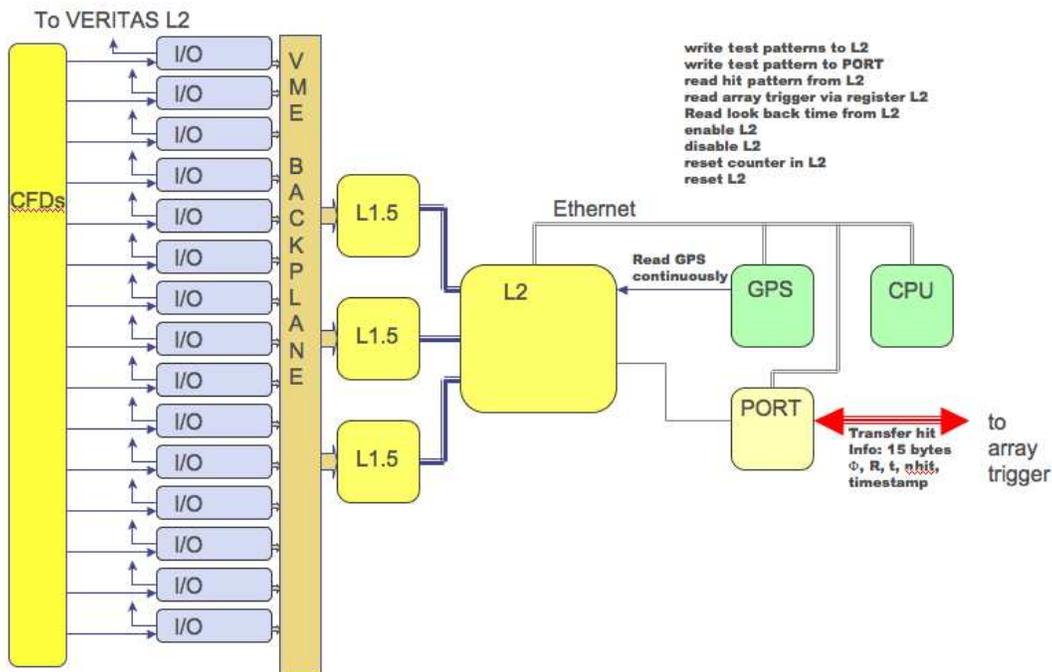


Figure 6: The connections between the VERITAS CFDs, the I/O cards, the VME Backplane interface to the L1.5 cards and furthermore the L2 card are shown. The L2 card can be addressed via Ethernet by a CPU and basic trigger patterns can be written and read out. Note that the 15 bytes to be transferred will contain $\langle x \rangle$, $\langle y \rangle$, $\langle x^2 \rangle$, $\langle y^2 \rangle$, $\langle xy \rangle$, the number of pixels with a hit and a time stamp.

7.1 I/O Cards

The Level 1 signals from the front-end electronics are discriminated signals from the camera pixels. They are sent from the front-end electronics using differential ECL, on 20-conductor,

unshielded, Twist-N-Flat cables. Each cable contains 10 signal pairs, 20 conductors total. The mapping of pixels to signal cables is shown in Appendix B. Each I/O Card accommodates four Level 1 cables, or 40 signals from the front-end electronics. Because of the requirement that the Topological Trigger be capable of operating within VERITAS environment without affecting operation of the existing Level 2 system, each signal cable has an input connector and an output connector. The I/O Card spies on the signals, receiving the signal source using a high impedance buffer, and then allowing the signal to propagate to the output connector.

Careful attention is given to the routing of the traces in an attempt to maintain signal impedance at 110 ohms (matching the Twist-N-Flat cables.) A block diagram is shown in Fig. 7. The I/O cards are specific to testing the camera trigger system in VERITAS. These cards essentially convert the ECL signal of the CFDs into LVDS signals that are more suitable for fast signals to be used. Furthermore, a copy of the ECL signal is routed for continued use in the existing VERITAS L2.

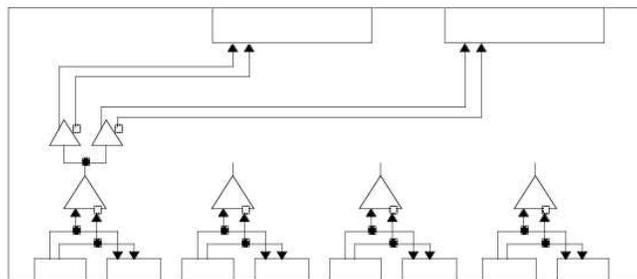


Figure 7: - The I/O card design is shown.

The receiving circuitry on the I/O Card is an ECL-to-TTL Translator (National, part number ???). The output of this chip is received by two identical TTL-to-LVDS translators (National, part number ???) One signal pair goes to the primary backplane connector, where the signals are routed directly to the L1.5 Card associated with that partition. The other signal pair is routed to the secondary backplane connector, which are used in the overlap logic. The signal from every camera pixel is handled this way. However, not all signals are used as overlaps. In order to facilitate easier fabrication of the relatively large quantity of I/O Cards needed in a system, the selection of signals for use in the overlap regions is handled by special routing on the backplane. While this results in some loss of efficiency and optimization due to wasted power and extra parts, it is countered by the simplification offered in the system construction, configuration, and maintenance. The key to the connectivity lies in the backplane. A given I/O Card does not know which signals are being processed. All signal routing is handled by the backplane. The signals from the primary connector are

routed to the associated Level 1.5 Processor. Only those signals used for the overlap logic are routed on the backplane to the affected Level 1.5 Processor. The unused signals on the backplane routed to the secondary connector are terminated on the back of the backplane. A consequence of this scheme is that each signal cable from the front-end electronics has a very specific connection in the crate. This was also deemed as an acceptable compromise in order to achieve simplification in the design and operation of the system.

7.2 L1.5 design

The actual camera trigger decision is reached by two units, the L1.5 trigger that operates on a subsection of a camera, and the L2 that combines the individual triggers from the subsections. This design is therefore also applicable and scalable to large numbers of pixels ($\mathcal{O}(10^4)$) for which in the order of 60 L1.5 cards and one L2 processor would be required.

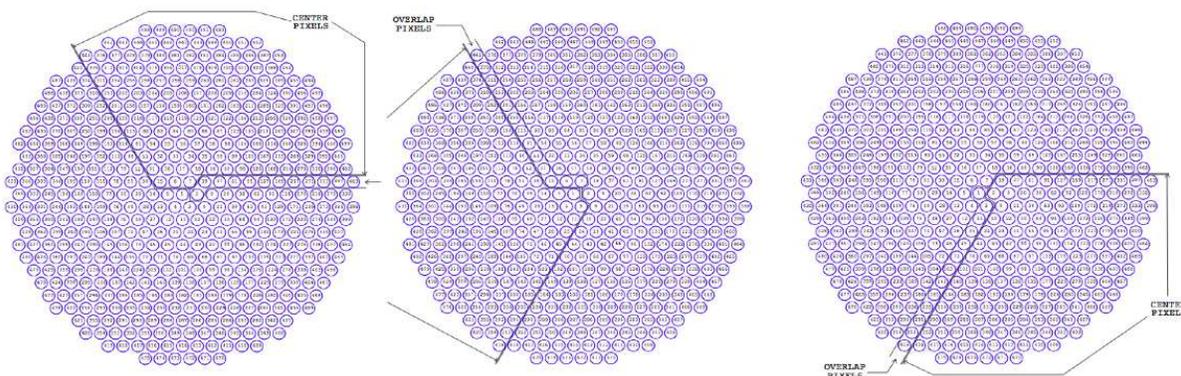


Figure 8: **Left** - The partitioning of the camera into three overlapping regions is shown. Each third of the camera is mapped into one L1.5 card that is used to form 3-fold coincidences for the non overlapping pixels and forms 2-fold coincidences for the overlap region of 12 pixels.

Each of the Level 1.5 partitions (see Fig. 8) has four kinds of pixels. Most of the pixels participate in normal neighbor logic, where each pixel is the primary pixel in a cell containing seven pixels, all of which are within the same partition of the camera. The outer edge of the camera is a special case, where the cells contain fewer than seven pixels (see Fig. 8). Next, each partition has a border with two other partitions. The border pixels are treated specially. On the edge called the overlap region, the signals from a given region are copied from the region of interest to the logic that processes signals in the neighbor region. (Note that the signal copy process is done on the I/O cards, with the special routing of signals incorporated on the backplane, as described in the previous section) The pixels along the

edge of the given region will have fewer than seven pixels in the cells, but the correction for the loss in efficiency is made up in the signal processing in the neighboring region. On the non-overlap region, the pixels on the edge of a given region receive signals from the neighboring region, and are used to form the 7-pixel cells.

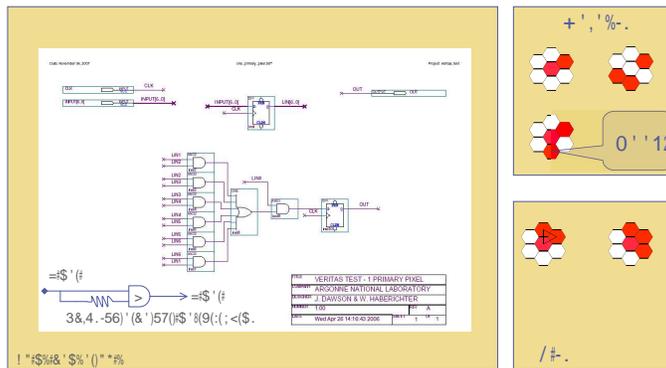


Figure 9: The coincidence logic for determining pixel coincidences and their effect on rejecting and keeping images is outlined.

In general, with the way that the partitioning was implemented, each partition has 180 pixels. Of these, only 12-13 pixels are overlap pixels from a neighboring region. Table 3.1 in Appendix B summarizes the configuration.

The L1.5 Processors have a VME interface, which offers certain control features. The Level 1 signals received by the I/O Cards from the front-end electronics are approximately 2-4 ns wide. No pulse shaping is done on the I/O Cards. Each of the signals coming into a L1.5 Processor is conditioned by a one-shot. The width of all of these one-shots is controlled by the VME write/read 6-bit Input One-Shot Width register (see Appendix C.) This width can be varied from 2.5 nS to 157 ns in 2.5 ns steps, but all of the one-shots widths will be the same in a given L1.5 Processor. Any number of these one-shots can be disabled by writing to one or more of the 12 VME write/read 16-bit Disable Center Pixels registers.

A New Event occurs when any Center Pixel's one-shot and any two, of up to six, neighbors one-shots form a coincidence. The Overlap Pixels are never used as a Center Pixel on this Processor. For diagnostic purposes, a bit in the VME write/read Mode Register can be set so that any one pixel (no coincidence needed) can generate a New Event. The signal processing on the L1.5 Processor uses a 400 MHz clock. A 29-bit Time Stamp counter is constantly being incremented by the clock, and once every second this counter is being reset to zero. Also, a 3-bit counter is counting the number of Time Stamp counter resets. These two counters form the 32-bit Time Stamp data.

All of a L1.5 Processors one-shot outputs, those that are part of the coincidence and those that are not, along with the Time Stamp data are processed using pipelining. Once a New Event occurs, all of the pipelined data is latched along with the one-shot output data on the next two clock time bins after the coincidence. All of this data (212 bits) are then

written into a 256 word (event) FIFO.

When the coincidence within a logic cell is established, the L1.5 Processor stores the pixel number. The pixel number is an 8-bit identifier, from 0 to 179 (the total number of pixels in a given partition minus one.) All hit pixels that satisfy the 3-fold logic criteria are recorded. The L1.5 Processor sends these 8-bit pixel identifiers to the L2 Processor. The actual X-Y locations on the camera are decoded from these identifiers by the L2 Processor. Note that pixel identifiers can be recorded multiple times, perhaps parts of many cells (up to seven.) The L1.5 Processor throws away duplicate identifiers before the data is sent.

After the FIFO becomes not empty, the next/first event is read out and all of the data is latched. The latched data is then sent out to the Level 2 Processor in 2 byte words. The L1.5 Processor appends four other bits with the data: two control bits with each word sent, to identify the data type; an output enable bit; and the output data clock. The decoding of the control bits is shown below:

If there are an odd number of pixels, then n Pixel Numbers would be in Output Bits 7-0 position and all 1s would be in Output Bits 15-8 position in the Last Word. To test the data integrity of data from the Level 1.5 Processor to the Level 2 Processor, an internal Diagnostic RAM Memory can be used. This memory is 180 bits x 2048 words, and the data uses a 200 MHz clock to set the one-shots on the L1.5 Processor. The memory is written/read and controlled from VME. A global VME command can start all three Level 1.5 Processors memory readouts at the same time. See Appendix C. Some of the other features of the L1.5 Processor that can be controlled from VME include: There is a global VME command that clears the 3-bit Number of Time Stamp Counter Resets in all three Level 1.5 Processors at the same time. The Level 1.5 Processors can monitor the condition of the +5 and -5.2 voltages on the I/O Cards with a VME read. A 1 read would mean that voltage is OK.

7.3 L2 design

The Level 2 Processor has three 40-pin input connectors that receive data from the three Level 1.5 Processors. Each connector has 20 LVDS signal pairs (16 data bits, 2 control bits, 1 output enable, and 1 output data clock). While the output enable is true, the data is written into an Input FIFO (18 bits x 1024 words) using the clock that is sent along with the data. When one of the Input FIFOs becomes not empty, the Level 2 Processor waits until at least 3 words have been written to that FIFO. It then reads out the first two words and latches them. These first two words are the 4-byte Time Stamp data with control bits set to '0 1'. If the control bits for these two words are not '0 1', then an error bit is set. Once the timestamp from one FIFO has been read, the Level 2 Processor waits for 3 clock cycles to see if any other Level 1.5 Input FIFOs have received data. A latch is set for each FIFO that has data, indicating that data is available. Those FIFOs that have data available will have their 32-bit timestamps compared. This is accomplished using a programmable value that can be written through VME, the Timestamp Difference Register. Using the lowest timestamp value as a reference, the timestamp values for the other FIFOs with data are evaluated. Only those that are within the specified range are used in the data processing that comes next.

Once the timestamp evaluation has occurred, the L2 Processor begins reading the pixel number data from the selected FIFOs. Each pixel number read sets a bit in one of the 499 'Hit' latches corresponding to that pixel number. The Processor checks that the control bits are either '1 0' (Pixel Number) or '1 1' (Last Pixel Number). If not, then an error bit is set. Also, when a FIFO becomes empty, its control bits must be '1 1' for that last word or an error bit will be set. When all of the data for a given event has been read from the FIFOs, the L2 Processor then latches the 'Hits', the earliest Time Stamp, and any Error Bits. The processor then waits about ≈ 100 nS (this time may have to modified), while the output data algorithms are being computed. The calculated quantities are: $\langle x \rangle$, $\langle y \rangle$, $\langle x^2 \rangle$, $\langle y^2 \rangle$, $\langle xy \rangle$. The calculation of the average X and Y positions is performed using unsigned integer arithmetic. The calculation of the squares and cross-term is done using look-up tables whose values are loaded at power-up from EPROM. The average quantities are 8 bits, while all others are 16 bits. This data is sent to the Level 3 Processor, along with the timestamp, number of hot pixels, and the error bits. The data is saved in the L2 Output FIFO. Once the data has been written to the Output FIFO, then the first event is read out and latched. This latched Output Data is sent, 2 bytes at a time, to a Seralizer/Deserialzer chip which will serialize the data and send it out on a Gigabit Fiber. After sending all of an event's data to the Seralizer/Deserialzer , then if there are more events in the Output FIFO, the next one will be read out, latched and sent out, and so on until it is empty.

With the hit pattern in the FIFO, the calculation of the ϕ , r and the the number of pixels hit (nhit) can be performed in about 100 ns. This time just adds a delay for issueing a camera trigger before it will be send to the L3 for inspection, and has no impact on the deadtime of te system. The FIFO should have a stack length of approximately twice the budgeted delay time ($50 \mu s$ for 1km^2 array) for forming an array trigger so that the complete trigger hit pattern can be captured once an array trigger was formed. The L2 trigger info should be send serially to the optical fiber module that transmits the info at 10 GHz rate.

8 Array Trigger Design

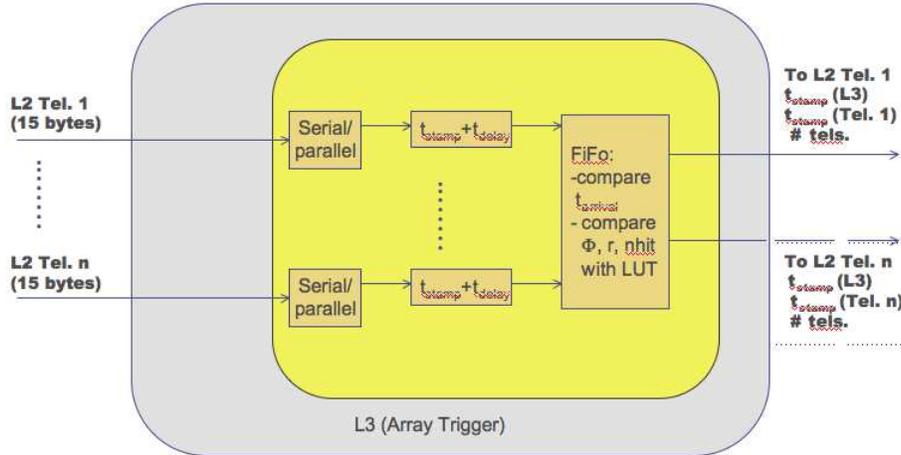


Figure 10: The L3 basic function is shown.

8.1 L3 design

The very basic function of the array trigger is indicated in Fig. 10. After having been adjusted for the proper time delays via adjusting the time stamps the search for time coincidences between different telescopes can start. The coincidence logic has an adjustable gate width (10 ns - 200 ns) so that the L3 reduces the number of accidentals at an early stage before processing based on image information starts. If a time coincidence between N telescopes has occurred, the remaining image information could be read into a FIFO and then processed using a lookup table.

Once the array trigger condition is met, a trigger signal with a time stamp and the individual telescope info should be send back to each telescope for L2 FIFOs to be read out based on a counter or a time stamp originally determined by the individual L2 decisions.

The array trigger design (L3) and the L2-L3 communication are interdependent and we have considered a variety of possible solutions. However, all L3 design schemes are based on using time stamps for matching array trigger events and therefore no timing edges or any time critical information is being exchanged between the L2 and the L3. However, the ability to synchronize the local GPS clocks has to be provided requiring a bi-directional

exchange of data. The challenge is rather to convert and transmit the bit information about the images at the L2 to the L3 so that the camera trigger rates of 1-10 MHz can be achieved.

First we describe the various options that we have explored which include data formats and custom and commercial solutions. We also consider different options for the actual L3 trigger processor unit which is closely tied to the data transmission.

8.2 Solution A: Custom protocol and data push driven L2 - L3 communications:

Once the L2 has produced a trigger, the event information needs to be transferred to the L3 trigger. A possible solution is given by a commercial 16-bit Bus LVDS Serializer/Deserializer (DS92LV16 from National Semiconductor). This chip translates a 16-bit parallel word into a LVDS serial stream with embedded clock information. The translation is the bottleneck and can be done at 80 MHz, which allows 96 bits (4 bytes for time stamp, 5 bytes for calculations and 1 byte for check sum and two bytes TBD) to be translated within 100 ns.

This is adequate for 20 MHz throughput rate which is a factor of two below the maximum specification for the L2 rate. Assuming there is no additional latency, this clearly meets the specs for the L2. The advantage is that the expertise of the implementation already exists for the L2 end, however, no standard solution as to how to read and process the data at the L3 end exists. This design would require another FPGA board design that receives the data at the L3 and processes it.

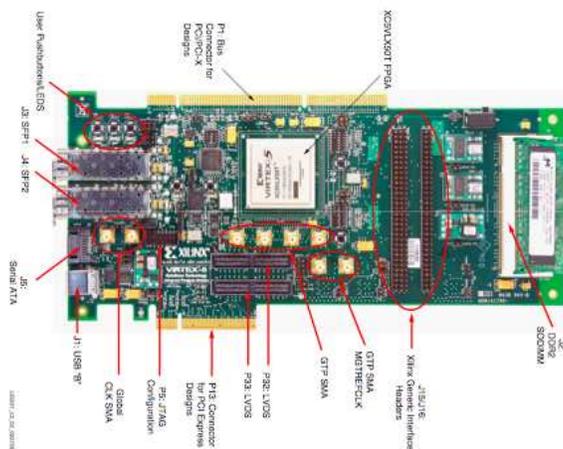


Figure 11: The XILINX development board Virtex-5 LXT ML555 with its connections and inputs/outputs is shown.

The FPGA board that receives the data could be realized for example using the Virtex-5 LXT ML555 FPGA Development Kit for PCI Express (see Fig. 11) which could be used to perform a DMA transfer of the data. This would allow us to get the data from the individual

L2 systems with low latency into the memory of a PC for further processing of the array analysis.

8.3 Solution B: PCI bus protocol and data push or poll driven L2 - L3 communications

An attractive alternative solution for future array trigger systems could be the usage of a standard commercial CPU (Mac G5, etc.) that receives the data via a PCI-bus interface. There are several possible solutions for transmitting processing based the PCI-bus.

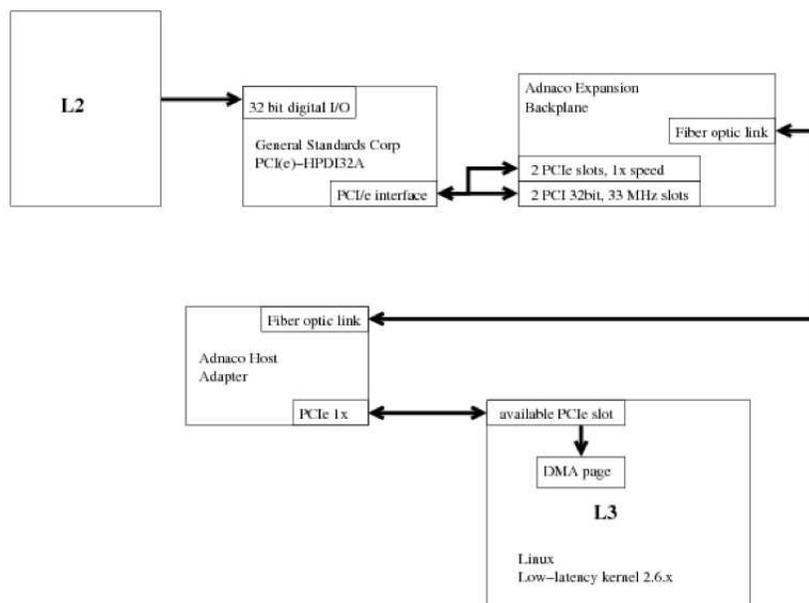


Figure 12: The L2-L3 communication scheme could be based on PCIe for which commercial fiber transmitter cards exist. The data could be transferred from L2 by a DMA transfer (Direct Memory Access) into a PC's memory and allow fast data processing of the L3.

1. An external I/O card receives the L2 data (see Fig. 12). L2 clocks the data in at up to 50 MHz. Data is accumulated for 1 or up to 10 events. Data packages are transferred with direct memory access (DMA) to host computer (L3). The external I/O card comes with a software development kit (SDK). L3 is almost completely independent of L2. Bi-directional communication is slow⁶ and this may be a disadvantage. This scheme uses a **PCIe-HPDI32A** I/O card and can transmit data up to 200 Mbytes/s. The I/O card has a FIFO memory (up to One Mbyte of total FIFO) and provides continuous transmission of data without interrupting the DMA transfers or requiring intervention from the Host CPU.

⁶This is because the I/O card needs to know whether to send or receive data.

Available transceivers are RS485/422 and PECL⁷. The data can be transferred from here to L3 via an **Adnaco-Sirius-R1TK** backplane card that sends the data to the host card at the L3 (**Adnaco-host**). The data can be read and fed into a PCIe slot and is available as the computer's DMA, which is part of its RAM. From here processor interrupts for DMA transfer complete commands are necessary. To read data, the data will be available for the processor to perform the array analysis, should a trigger be issued an interrupt would occur and an L3 trigger be issued and transmitted to the individual telescopes and via their L2 cards to disable those and issue a readout signal to the FADCs.



Figure 13: The PCIe-HPDI32A PCI card is shown.

2. An off-the-shelf PCI card with FPGA **DK-PCIE-2SGX90N** from ALTERA communicates with L2. Communication between L2 and L3 can be bi-directional. This solution needs an FPGA-to-FPGA interface at the L2 end and a PCI-to-FPGA driver development at the ALTERA card. Altera sells a PCI Express development kit (see Fig. 14) Stratix II GX edition that comes with a complete driver development kit.

In this case the L3 development is somewhat independent from L2. In this option, the L2 could potentially provide two options: one would be based on a FPGA-PCI driver that could then use the PCIe option to communicate with L3, the other option would be to have L2 also use the LVDS Serializer/Deserializer (**DS92LV16**) that could also deliver the data to an FPGA at the L3 end, or could deliver the data to a FPGA-PCI card.

⁷TTL and LVDS transceiver versions are also available and use the PMC64-HPDI32ALT but they come only in 64-bit versions



Figure 14: The PCI-EXPRESS-STRATIX-II from ALTERA is shown. This is a development kit and is available.

9 Appendix A: Algorithm

The philosophy of the algorithm is to put the local telescope trigger into a position that it can already make sophisticated trigger decisions based on the image pattern and location. This requires some basic image analysis. To save processing time, it would be most beneficial to process the following calculations in parallel, whenever possible. This is likely going to increase the timing requirements for each individual process and hence it is important to synchronize those. Synchronizing could mean that all processes have a fixed amount of time to come to a decision making it necessary to built in delays for the processes that take the least amount of time.

1. One step for the camera trigger is to calculate the position of the image centroid in the camera from the hit pattern that is received in parallel from the CFDs. It is perhaps useful to express the hit pattern as a vector $\vec{p}(499)$ for further discussion and processing since it enters the FPGA in parallel. For example, if just pixel 1, 2 and 3 have fired, $\vec{p}(499) = (1, 1, 1, 0, \dots, 0)$.

The calculation of the pattern's mean x-position \bar{x} and the y-position \bar{y} can be performed using adders and multipliers effectively forming the dot product of the vector of the x-positions of the individual pixels $\vec{x}(499)$ (supplied in appendix B) and the vector containing the hit pattern \vec{p} . The resulting sum has to be divided by $\vec{p} \cdot \vec{p}$ for normalization. This also provides us with the number of CFDs triggered, hence the pixel number in the image. The vectors \vec{x} and \vec{y} are given in Appendix A.

$$\bar{x} = \frac{\vec{p} \cdot \vec{x}}{\vec{p} \cdot \vec{p}}$$

$$\bar{y} = \frac{\vec{p} \cdot \vec{y}}{\vec{p} \cdot \vec{p}}$$

$$n_{hit} = \text{number of pixels fired: } n_{hit} = \vec{p} \cdot \vec{p}$$

The actual operation could be achieved by loading the contents of the x-coordinate/y-coordinate into an 8-bit stack for each channel and form a sum of all the channels that have a hit using a digital summing operation. Normalization can be achieved by having a separate branch counting the number of hits.

The result from these two operations should be \bar{x} , \bar{y} and n_{hit} . These two operations could be done in parallel.

Besides the mean we also need the variance $\sigma_x^2 = \frac{1}{n-1} \sum (x_i - \bar{x})^2$ which is more efficiently calculated by $\sigma_x^2 = \frac{n}{n-1}(\bar{x}^2 - \bar{x}^2)$. The same should be calculated for the y coordinate ($\sigma_y^2 = \frac{n}{n-1}(\bar{y}^2 - \bar{y}^2)$). Furthermore we would like to get the mixed term $\sigma_{xy} = \frac{n}{n-1}(\bar{xy} - \bar{x}\bar{y})$

2. To make a decision for issuing a local telescope trigger we need two characteristics of the event: number of pixels fired n_{hit} , in the following denoted by j, and the number of neighbor pixels, in the following denoted as m.

Therefore, we need to calculate the number of neighbor pixels in the hit pattern vector. This can be achieved by the following algorithm using a lookup-table that contains the following information:

Each row contains the pixel number i, element 2 to 7 contain the neighbors of pixel i. The algorithm goes as follows (for complete table see Appendix A). First we form a logical AND between the hit pattern vector $\vec{p}(499)$ and column 1. This gives the pixel numbers that have a hit and that should be evaluated for neighbor counts.

The next step is to compare $\vec{p}(499)$ with the neighbor vector $\vec{n}_i(499)$ for each fired pixel in increasing order. The maximum number of steps here is j (given by n_{hit}). Again this is a simple dot product and the result gives the number of neighbors also hit for a particular pixel i . The next steps are going through each fired pixel and compare the neighbor vector with the hit vector $\vec{p}(499) - (0, 0, 1_j, 0, 0, \dots, 0)$, to avoid double counting of neighbors.

By counting the number of matches we get the total number of pixels that have a neighbor $n_{neighbor}$. This algorithm could be fast for small single island images, which are most of the events close to threshold.

Obviously there could be images (hit patterns) that have a large number of n_{hit} and consequently one would count a large number of neighbors. However, once n_{hit} reaches a number between 5 - 10 we are no longer interested in the total amount of neighbors, since the requirement for a low n -fold coincidence is met. This means that we could limit the counting of neighbors to the neighbor coincidence criterion and issue a flag indicating that a camera trigger is present.

3. The centroid positions are most useful in polar coordinates, allowing a straightforward trigger criteria first at the camera level and subsequently for the array trigger level. The following formulas provide the coordinates r and ϕ .

$$r = \sqrt{\bar{x}^2 + \bar{y}^2}$$

$$\phi = \arcsin \frac{\bar{y}}{r}$$

4. Now a local telescope trigger can be issued based on the following criteria:

$$r, n_{hit}, n_{neighbor}$$

The detailed criteria will be determined from simulations that we are currently starting. Here we need a Look Up Table (LUT) that uses for example an algorithm making a trigger decision that has different requirements for different radial distances from the source allowing to maximize the collection area at low energies while maintaining sanity for the trigger rate.

5. Time stamp: it is important that each telescope trigger gets a time stamp attached to its image parameter list. There may be different ways to keep track of the time of the CFD hit pattern causing a local array trigger. One would be to have a constant processing time for each hit pattern. This means that the algorithm has to go through the same number of steps (clock ticks) to make a trigger decision. The time stamp could then be determined by subtracting a constant amount (trigger formation time $t_{trigger}$) from the time stamp recorded when a trigger is issued. This is likely to lead to a slightly inflated trigger formation time $t_{trigger}$. If $t_{trigger}$ is less than about $10\mu s$ this may be acceptable.

6. Each camera trigger should get an event number and event type. Those data should be send together with the image pattern information. We should foresee injected events and special events that can initiate a camera trigger.

7. Each camera trigger should get a calibration input to test the absolute timing precision of the trigger modules from the various cameras.

10 Appendix B: Technical Details

The mapping of the VERITAS pixel numbering scheme onto the I/O cards and the L1.5 is given below.

VME Memory Map for L1.5 Processor:

The Card ID Address (A23-A19) is set by the 5 switches on SW1 (ON = 0). The only Address Modifiers that the card will respond to are:

1. AM = 39 Standard Non-Privileged Data Access
2. AM = 3B Standard Non-Privileged Block Transfer

Address Hex Address (h)

Modifier Offset (A18-A1) Function

39 h00000 WRITE/READ Disable Center Pixels: (1=Disable)

D0 = 19 D1 = 37 D2 = 61 D3 = 91

D4 = 127 D5 = 169 D6 = 217 D7 = 271

D8 = 331 D9 = 397 D10= 463 D11= 2

D12= 8 D13= 20 D14= 38 D15= 62

11 References

- See for instance Rene Ong's Rapporteur Talk at the 29th International Cosmic Ray Conference (Pune) (2005)
- Krennrich, F. and Lamb, R.C. *Experimental Astronomy*, 6, 285-292 (1995a)
- Krennrich, F. and Lamb, R.C. *Proceed. of Towards a Major Atmospheric Cherenkov Detector III*, Padua (1995b)
- see <http://veritas.sao.arizona.edu/>
- see <http://www.mpi-hp.mpg.de/hfm/HESS/HESS.html>
- private communication with A.M. Hillas.
- LeBohec, S., Krennrich, F. & Sleege, arXiv:astro-ph/0501199 v1, (2005).
- Hillas, A.M., in *Proc 19th I.C.R.C. (La Jolla)*, Vol 3, p. 445 (1985).
- see http://gamma3.astro.ucla.edu/future_cherenkov
- Mirzoyan, R. et al., *Nucl. Instr. Meth.* A351, 513 (1994).
- Karle, A., PhD Thesis, Ludwig Maximilians University (Munich) (1994)
- Weekes, T.C., *ApJ*, 342, 379 (1989).