

Conceptual Design of the Digital Telescope (DTEL) ASIC

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1. Introduction

In recent years, advances in the fields of high-energy physics, astronomy, and cosmology have produced results that suggest our understanding of the universe in terms of high-energy physics alone is incomplete. This has given rise to a relatively new field of study called *astro-particle physics*, which incorporates the intersections of high energy physics, cosmic ray physics, cosmological physics, astrophysics and astronomy. For example, astrophysical observations can explore various parameters which, in turn, will motivate searches for the quantum explanation with accelerator experiments. Among the most interesting physics topics of astro-particle physics are the search for dark matter, the understanding of dark energy, quantum theories of gravitation, and the physics of black holes.

A primary area of study in this field is concerned with ground-based observation of gamma rays from astrophysical sources, such as regions of space with a high density of dark matter, gamma ray bursts or high red shift objects. The recent advent of imaging atmospheric Cherenkov telescopes (IACTs) has provided a first look at those sources from the earth's surface. In fact, IACTs provide orders of magnitude more sensitivity than satellite experiments (although with limited fields of view) for measuring sufficiently hard spectra and the angular resolution is typically an order of magnitude better with a ground instrument.

The Earth's Atmosphere is opaque to much of the electromagnetic spectrum. X-rays and gamma-rays are absorbed by the atmosphere and satellites are required for their direct detection. However, the atmosphere of earth can be used as an enormous detector. When a high energy gamma-ray (photon) interacts in Earth's atmosphere, it produces a narrow avalanche of lower-energy electrons, positrons and gamma-rays that head toward the surface. Because most of the electrons in the shower are moving faster than the speed of light in the atmosphere, they emit Cherenkov light, an electromagnetic shock-wave analogous to the sonic boom emitted by a supersonic jet. This light can be detected as a faint blue flash of short duration (tens of nanoseconds) at ground level. Cherenkov gamma ray detectors use tessellated mirrors to image the Cherenkov radiation into a camera composed of an array of photo-multiplier tubes (PMTs). Although Cherenkov light is also produced by cosmic-ray showers (protons or heavier nuclei of extraterrestrial origin), Cherenkov light from gamma-ray showers can be discerned by its comparatively smooth shape, compact angular distribution, and geometric pattern.

Over the past few years ground based gamma-ray astronomy has entered a new era by using arrays of IACTs. These instruments (typically 2-4 telescopes displaced by 50-100m from each other) have improved energy resolution, improved angular resolution and better background discrimination and are able to measure gamma rays in the range of 50 GeV to 50 TeV with a precision of about 15%. They can reconstruct the direction of the gamma ray to better than .1 degree with a field of view of order 3.5 – 5 degrees. Initial results from one of these instruments called HESS has very recently produced images of the galactic center tera-electron-volt sky

locating point sources of very high energy radiation to within 30 arc-seconds. Another instrument called VERITAS will begin making measurements this year.

The ground based gamma-ray astronomy community is now considering new approaches and techniques that will greatly improve the technique. The goal is to achieve even finer angular resolution while lowering the energy threshold, from the current level of 50 – 100 GeV to 10 – 30 GeV. This will result in significantly greater sensitivity in searches for dark matter (neutralino decays) and the ability to probe the universe at earlier times (deeper space is equivalent to earlier time) with the large photon statistics that is the strength of the IACT technique. In addition, by improving the angular resolution, a better identification of sources is obtained, as well as a reduction in the large night sky background.

One leading idea for the next generation of IACTs is to construct a large array of telescopes, each having very fine angular resolution. The approach needed for the new telescopes is to incorporate higher pixelation, which translates into higher resolution. This implies a very high channel count, on the order of 10,000 channels per telescope. The new telescopes will also need high timing resolution, of order 1-2 ns, and a sophisticated high-speed trigger.

Typically, current imaging telescopes use an array of single-anode photo-multiplier tubes. They measure the energy deposition over a wide dynamic range, and have timing resolution on the order of 1-2 nanoseconds. This is achieved by digitizing signal pulse height (integrated current) using an ADC having 12 to 18 bits of dynamic range. Because large dynamic range is often expensive, cost/performance trade-offs usually result in each read-out channel servicing a rather large angular area of the sky. Current telescopes typically use one inch, single anode photo-multiplier tubes, which translates to relatively coarse angular resolution. One aspect of the new generation of telescopes would use an array of multi-channel photo-detectors having very fine pixel structures. A leading candidate is a multi-channel photo-multiplier tube, although avalanche-photo-diode arrays will be considered. Instead of measuring pulse-height, the new approach retains high timing resolution, but instead uses discriminators to measure “hits” on the pixels of the tubes, basically counting signals at the 1-2 photoelectron level. When an event occurs, the telescope will produce high-speed images in time. The events are analyzed by studying the shape of the images, and their progression and movement as a function of time. A significant performance challenge is to trigger on real events, and discard dark noise from thermal emission in the tubes. The tubes will also be exposed to a significant amount of background light from the night sky, which can be a source of noise. Several levels of triggering in the front-end electronics are needed to reduce reading out noise. This also is similar to the technical challenges of a typical high-energy physics experiment.

A consequence of this approach is that with high pixelation comes high channel count. Instrumentation that utilizes pulse-height measurements and extended dynamic range is expensive, even if a custom integrated circuit is used. Current

telescopes have of order 500 channels. In order to achieve the desired angular resolution, of order 10,000 channels are needed for each telescope. The cost of electronics for this number of channels using pulse-height measurement would be prohibitively expensive, as well as present a serious technical challenge to read out the large number of bits associated with high dynamic range at 500 MHz to 1 GHz. Fortunately, the use of small pixels and the analysis techniques envisaged resonates with the use of a simple discriminator on each channel.

Given the high channel count, the high density of detector elements and associated front-end electronics, and the sophisticated nature of the electronics, it is clear that a custom integrated circuit is needed for this implementation. This document is a first pass at the conceptual design of such a chip. The basic architecture has been used in several applications already, including the FSSR for the BTeV experiment, and the DCAL chip for the hadron calorimeter of the Linear Collider. Significant differences and challenges for this chip include the clock speed, 500 MHz or greater, and the intrinsic background noise rate.

2. Overview

A conceptual block diagram of the device under consideration is shown in Figure 2.1. The operation can be divided into several functional blocks, which will be described.

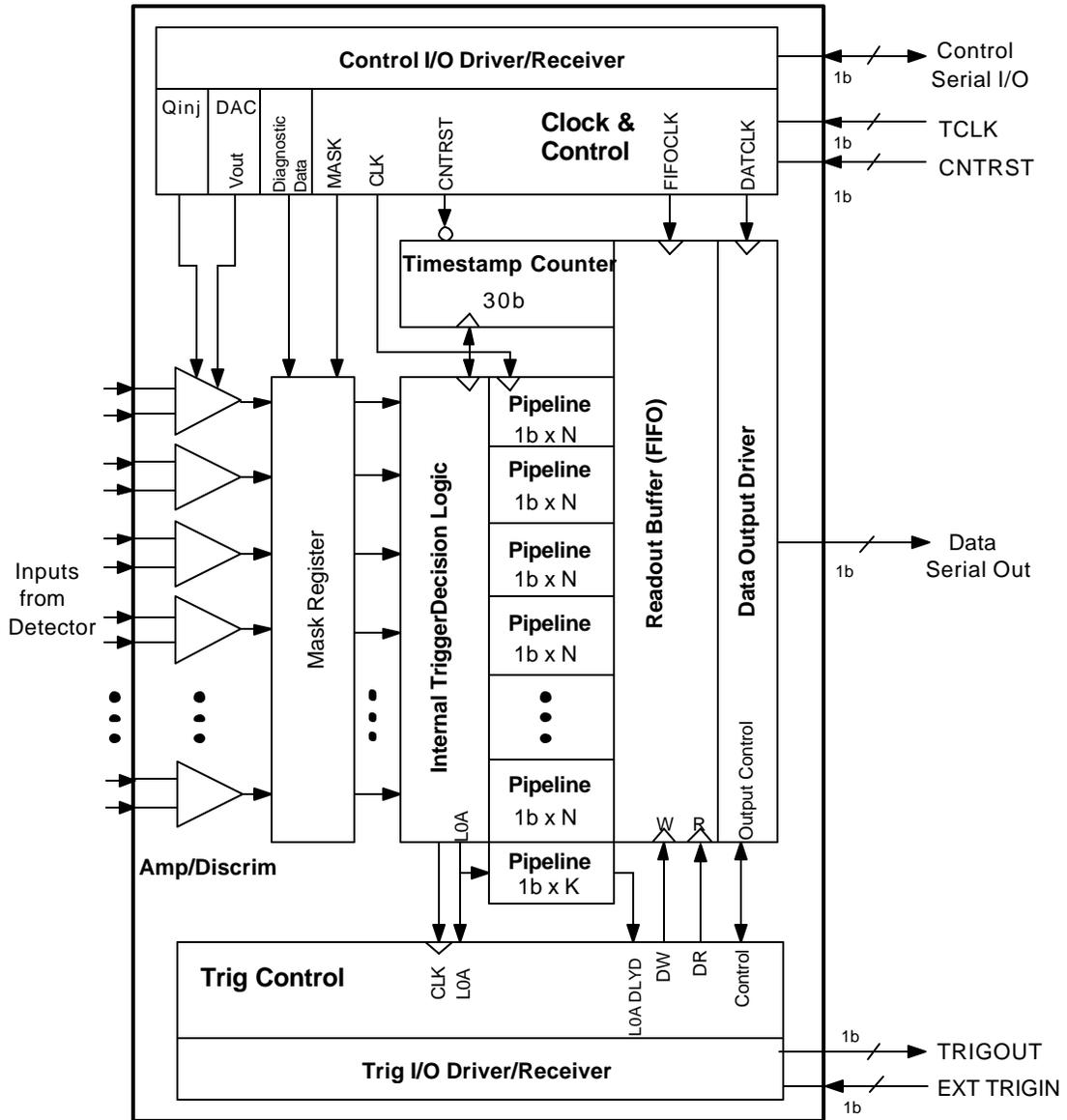


Figure 2.1. Block Diagram of ASIC

2. Overview (Cont.)

Signals from the telescope camera are charge or current pulses. When a signal is received from the camera, it is amplified and shaped. It is then passed to a discriminator, where it is compared to a threshold voltage. If the signal level exceeds the threshold level, then the discriminator would fire. The discriminators are evaluated using a clock provided to the chip from outside. The discriminators must hold the state of the response until the end of the clock cycle (defined to be the rising edge), so that the state of the discriminators can be latched into the circuitry that follows. Care must be exercised so that small pulses that fire a discriminator briefly will cause the discriminator to latch even if the signal level falls below threshold before the end of the clock cycle.

In order to reconstruct hits in the DAQ, the chip shall provide an event ID for each hit. The chip uses the concept of a Timestamp Counter to accomplish this. It is essentially a free-running counter, which is reset periodically (~ once per second.) The counter is advanced by the clock provided to the chip. Since the data is tagged with an event ID at the front end, the constraints on the system for bringing together event fragments in time are greatly reduced. For this application, the frequency of operation for the Timestamp Counter shall be 500 MHz.

Both the Timestamp Counter bits and the discriminator states define event data. They are written into a pipeline, and are advanced through the pipeline by the clock. At the end of the pipeline, a decision must be made whether or not to keep the event data. An accept decision causes the bits to be written into an output buffer, which is configured as a FIFO. From there, circuitry in the chip is activated that reads the event data from the output buffer, and sends it out of the chip.

The chip would have two levels of triggering. Prior to being shifted into the pipeline, the discriminator states are evaluated by logic called the Level 0 Trigger. This logic looks for a multiplicity of hits within a certain time window. Only if this is satisfied would the discriminator states be written into the pipeline. When this condition is satisfied, the chip also makes the signal available to the outside, to be part of the next level of triggering, called the Level 1 Trigger. This trigger exists outside of the DTEL chip, and uses information from several chips, and possibly from other sources, to decide if a particular event shall be read out. The Level 1 Trigger decision must be presented to the DTEL chip (actually all DTEL chips) by the time the data emerges from the pipeline.

The data output is envisaged to use a serial communication protocol. It is a dedicated communication path, and uses a "data push" configuration. It is not necessary for this link to be bi-directional. The format of the output data transmission is described below. The link shall operate at the frequency of the Timestamp Counter, or 500 Mb/Sec.

2. Overview (Cont.)

The chip requires three timing signals to function. The most important is the clock. There is only one clock for all of the functions of the chip, and everything operates synchronously. Another timing signal needed is Counter Reset. This must be a precision signal (to within one clock cycle), as it is used to synchronize timing of all chips in the system. The third timing signal is be used to inject charge into the front-end amplifiers at a precise time.

Control functions of the chip are handled by a dedicated interface called Slow Controls. It also uses a serial communication protocol, and is bi-directional. This communication path has several functions. The chip needs an on-board DAC to generate the threshold voltage for the discriminators. Another important control feature is the ability to mask off bad channels. This is needed to prevent noisy channels from co-opting the readout bandwidth. This could be incorporated by using a simple AND gate with the output of each discriminator. The masking would be accomplished by loading a "Mask Register" through the control link. Another control function is the control of charge injection. The ability to inject charge is useful for testing the basic signal processing circuitry. By providing the capability of injecting charge at a precise time over many parts of the system, the synchronization of the chip counters could be tested. If the charge injection circuitry were further enhanced to incorporate a DAC, it would be possible to study the sensitivity of the discriminators as a function of threshold voltage setting versus value of the charge injected.

3. Specifications

3.1 General

- 3.1.1 The intended frequency of operation for the chip, including timing, pipeline operation, and time frame formation for the serial drivers, shall be a minimum of 500 MHz. This is defined as the ***Fundamental Frequency of Operation***. In general, it is expected that the chip be capable of operation up to, or in excess of, 600 MHz without failure or error. See Section 3.10 for timing specifications.
- 3.1.2 The digital functions of the chip are intended to operate synchronously with respect to the clock.
- 3.1.3 This specification describes the design of a mixed analog/digital chip. In certain modes of operation, low-noise analog design techniques are required. The semiconductor fabrication technology and specific design and implementation details are left to the chip designer's discretion.
- 3.1.4 The chip shall service 64 detector channels.

3. Specifications (Cont.)

3.2 Amplifier/Discriminator Section

3.2.1 The Amplifier/Discriminator Section performs the analog signal processing in the chip. The outputs are digital signals.

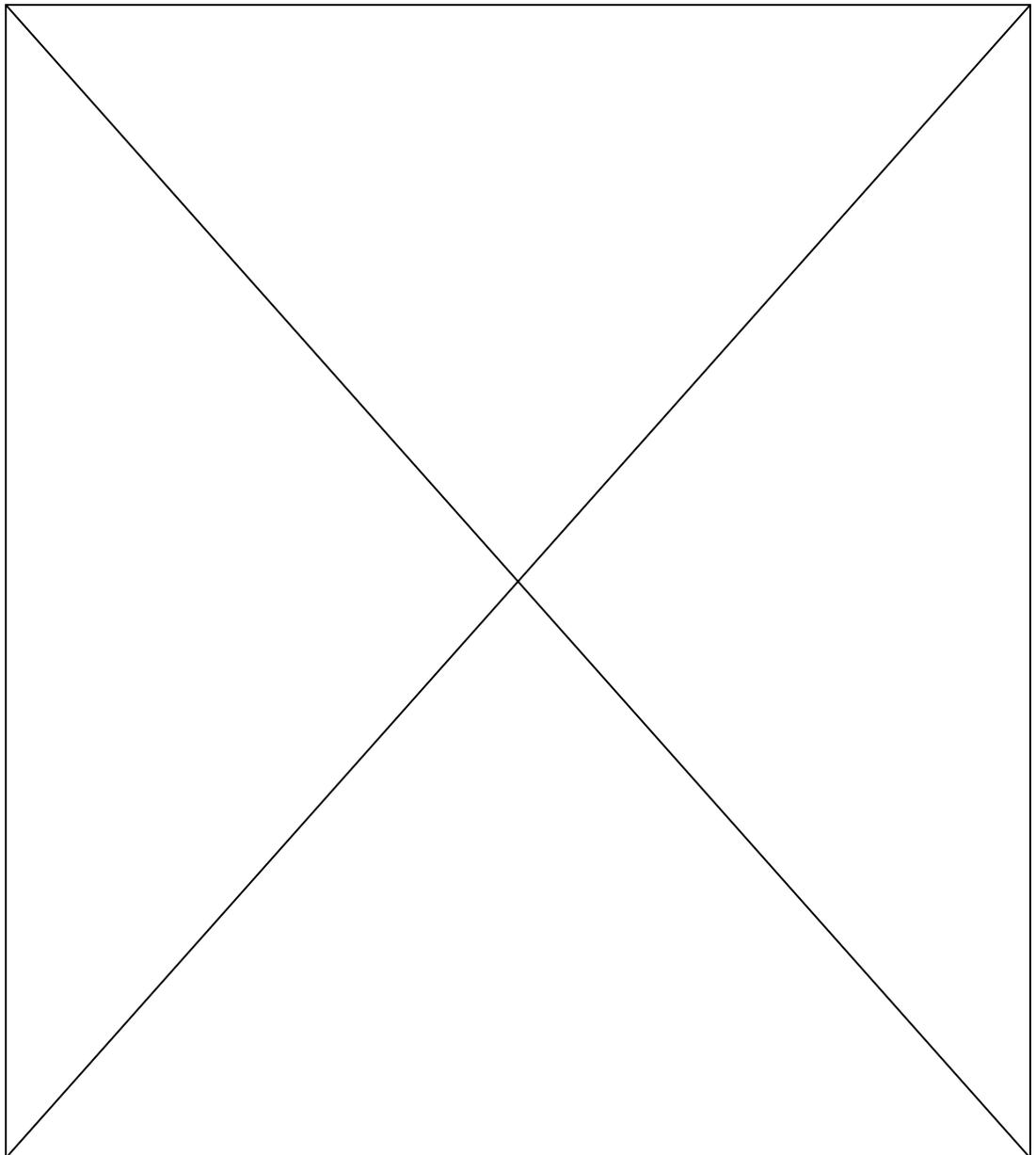


Figure 3.2.1. Amplifier/Discriminator Section

3. Specifications (Cont.)

3.2 Amplifier/Discriminator Section (Cont.)

3.2.2 The Amplifier/Discriminator Section can be divided into two functional blocks, as shown in Figure 3.2.2.

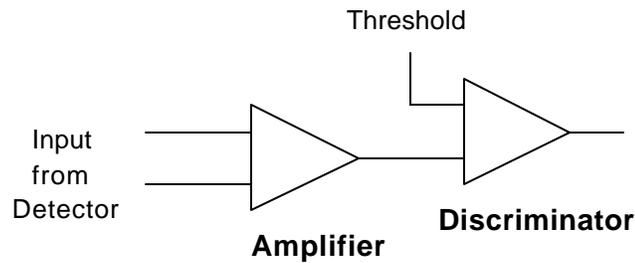


Figure 3.2.2. Amplifier/Discriminator Block Diagram

3.2.2.1 The primary function of the amplifier is to receive and amplify charge pulses from the detector, and produce an output voltage that is proportional to the signal received. The amplifier may also provide shaping for the output voltage signals.

3.2.2.2 The primary function of the discriminator is to receive a voltage from the amplifier, and compare it to a threshold voltage provided on-board the chip. If the amplifier voltage is greater than or equal to the threshold voltage, then the output of the discriminator shall be asserted to the logic 1 state. Otherwise, the output of the discriminator shall be asserted to the logic 0 state, which is also defined to be the "Rest State." Note that the discrimination process acts on the total charge received from the detector.

3. Specifications (Cont.)

3.2 Amplifier/Discriminator Section (Cont.)

3.2.3 The Amplifier Section has the following properties:

3.2.3.1 The front-end amplifier must be capable of receiving, amplifying, and processing signals from the detectors. The detector signals are current pulses in nature (i.e. high source impedance at DC.) The amplifier must be capable of processing current pulses that are negative in the conventional sense (electrons are sourced from the detector).

3.2.3.2 The output of the amplifier is a voltage, which is proportional to the magnitude of charge signal received (dQ). The output voltage is passed to the discriminator section, to be compared to a threshold voltage.

3.2.3.3 The smallest signal of interest from the detector corresponds to 5 fC of total charge. (This is one photo-electron from the photo-multiplier, with a gain of $1E5$, on the lowest gain pixel having 1/3 the response of "normal" pixels.)

3.2.3.4 The largest signal of interest from the detector corresponds to 2 pC of total charge.

3.2.3.5 It is necessary to record hits from the detector promptly. Consequently, the rise-time of the amplifier is important. The charge signals have rise times of ~ 1 nS. The closed-loop, -3 db bandwidth of the amplifier shall be such that the rise-time of the amplifier is less than or equal to 50% of the period of the Fundamental Clock Frequency.

3.2.3.6 The maximum rate at which a channel will receive signals from the detector is on the order of 1 MHz. Shaping and recovery times should be designed to prevent baseline shifts and pile-up. The amplifier should be capable of recovering back to baseline from a full-scale input signal within 100 nanoseconds

3. Specifications (Cont.)

3.2 Amplifier/Discriminator Section (Cont.)

3.2.3 The Amplifier Section has the following properties (cont.):

3.2.3.7 It is NOT acceptable to use AC-coupling between the output of the amplifier and the discriminator. Due to the expected rates, this system shall be DC-coupled throughout the analog signal-processing chain.

3.2.3.8 It is acceptable for the input voltage of the amplifier to have a non-zero bias within one or two volts. The detector performance will not be affected at these levels.

3.2.3.9 It is necessary for each channel to have a specific signal return connection to the detector that corresponds to the signal input from the detector. The amplifier may be configured to have a single-ended input with respect to signal return to the detector. In this case, it is necessary for the amplifier to have a reference (analog ground) to the signal return to the detector. It is not necessary for the amplifier itself to have full differential input capability with common mode rejection. See Fig. 3.2.3. It is acceptable to gang the returns of several amplifiers together, up to a maximum of four amplifier returns per pin.

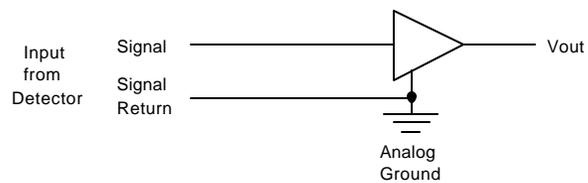


Figure 3.2.3. Single-Ended Amplifier with Signal Return

3. Specifications (Cont.)

3.2 Amplifier/Discriminator Section (Cont.)

3.2.3 The Amplifier Section has the following properties (cont.):

- 3.2.3.9 The wide-band input impedance of the amplifier shall be 50 ohms +/- 5%, with of a phase angle approximately 0, over the frequency range of ~100 Hz through the closed-loop bandwidth of the amplifier. The impedance may have non-zero reactive components below 100 Hz, and above the closed-loop bandwidth of the amplifier.
- 3.2.3.10 The intrinsic noise level of the amplifier must be less than 30% of the smallest signal level to be processed.
- 3.2.3.11 The amplifier must be designed so that digital activity in the chip is not picked up or amplified, at the minimum operational threshold levels (see Section 3.2.4.)
- 3.2.3.12 It is desirable for the amplifier to have a power supply rejection ratio in excess of -60 db up to the closed-loop -3 db bandwidth of the amplifier.
- 3.2.3.13 It is desirable for neighboring channels on the chip to reject cross talk to better than 40 db.
- 3.2.3.14 It is not desirable to use a sample-and-hold to sample the output voltage of the amplifier.

3. Specifications (Cont.)

3.2 Amplifier/Discriminator Section (Cont.)

- 3.2.4 The Discriminator Section has the following properties:
 - 3.2.4.1 Each channel shall have a discriminator, capable of responding to signals above a threshold voltage.
 - 3.2.4.2 The Threshold Voltage shall be generated from an on-board DAC called the Threshold DAC, and shall be common to all channels. See Section 3.11.
 - 3.2.4.3 The Discriminator shall be capable of discriminating on the smallest signals as specified in Section 3.2.3.3 with 50% efficiency. It is not necessary for the Threshold Voltage range to be so large as to prevent the Discriminator from firing on the largest signals as specified in Section 3.2.3.4. See Section 3.11 for a discussion of dynamic range and resolution of the Threshold DAC.
 - 3.2.4.4 The states of the discriminators shall be evaluated and stored on the rising edge of the Fundamental Clock Frequency.
 - 3.2.4.5 When an input signal meets the threshold requirements, it shall fire the discriminator on the clock cycle that follows. (This addresses the case where small, fast signals from the detector that have duration less than the period of the Fundamental Clock Frequency but otherwise meet the threshold requirements will fire the discriminator. This may be accomplished in different ways, including the adjustment of shaping times, or the use of edge-fired flip-flops on the output of the discriminator.)
 - 3.2.4.6 When an input signal meets the threshold requirements, it shall fire the discriminator once, and only once. (This addresses the case where shaping time constants are such that the amplifier recovery is slower than the Fundamental Clock Frequency.) A measurement of time-over-threshold is neither required nor desired.

3. Specifications (Cont.)

3.2 Amplifier/Discriminator Section (Cont.)

3.2.4 The Discriminator Section has the following properties (Cont.):

3.2.4.7 When an input signal meets the threshold requirements and occurs at or near the clock edge that would record the hit, it must be arranged so that the hit is not missed. If necessary, it is acceptable for the hit to be asserted in two adjacent clock cycles. It may be necessary to arrange the logic to use multi-phasing of the clock to accomplish recording and clearing functions.

3.2.4.8 The channel-to-channel matching of the input offset voltages of the discriminator shall be better than 2 equivalent DAC counts.

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3. Specifications (Cont.)

3.3 Level 0 Trigger Decision Formation

3.3.1 The output states of the discriminators shall be used as inputs to a logic block inside the chip to form a signal called the ***Level 0 Trigger Accept Decision, or L0A***. This signal shall be used both internally and external to the chip as described below, as part of the trigger decision process. See Fig. 3.3.1. Note that the method by which the chip is actually forced to record an event for read-out is described in Section 3.6.

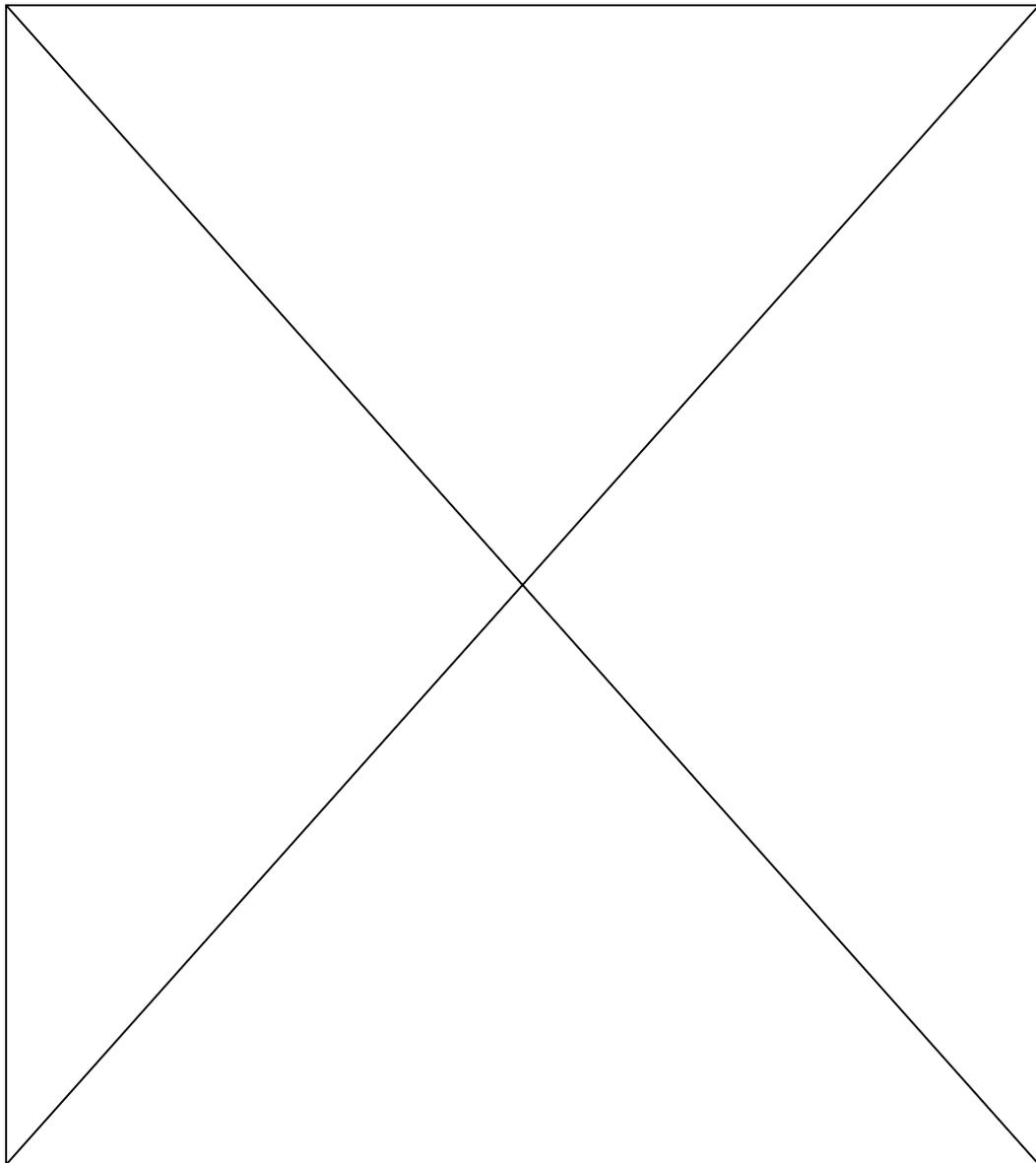


Figure 3.3.1. Formation of the L0A Trigger Decision

3. Specifications (Cont.)

3.3 Level 0 Trigger Decision Formation (Cont.)

- 3.3.2 The L0A signal is formed from the comparator states. L0A is asserted to the logic 1 state when one or more discriminators have a positive state in a certain time window.
- 3.3.3 The chip shall have two modes for executing a L0 decision as described below. The particular mode, called L0SEL, is set through Slow Controls (see Section 3.9.)
 - 3.3.3.1 For L0SEL = 0, the chip shall assert L0A whenever any single discriminator has a positive state in a certain time window. This shall be the default state.
 - 3.3.3.2 For L0SEL = 1, the chip shall assert L0A whenever two or more discriminators have a positive state in a certain time window.
- 3.3.4 The chip shall have the capability to define one of two time windows for forming a L0 decision. The particular selection, defined as LOWIN, is set through Slow Controls (see Section 3.9.)
 - 3.3.4.1 For LOWIN = 0, the time window for evaluating the discriminator states shall be 1 clock cycle. This shall be the default state.
 - 3.3.4.2 For LOWIN = 1, the time window for evaluating the discriminator states shall be 8 clock cycles.
- 3.3.5 The signal L0A shall be formed on the rising edge of the clock. The states of the discriminators are evaluated at that time (see Section 3.2), and the state of the L0A is determined accordingly.
- 3.3.6 A new L0 trigger decision shall be made on each clock cycle. The circuitry must be capable of operation well in excess of the Fundamental Clock Frequency, specified in Section 3.1.
- 3.3.7 It is acceptable for the processing time in the formation of the signal L0A to cause one or more clock cycles of delay. This delay may be in series or in parallel with the pipeline delay, as specified in Section 3.4, at the chip designer's discretion.

3. Specifications (Cont.)

3.3 Level 0 Trigger Decision Formation (Cont.)

- 3.3.8 The signal L0A shall be used to create an output signal from the chip, called ***Trigger Out, or TRIGOUT***. When L0A is asserted as described above, TRIGOUT shall have duration equal to half of a clock period. (The rising edge of TRIGOUT shall be used on the receiving end to process triggers.)
- 3.3.9 The chip shall be capable of driving the output signal TRIGOUT out of the chip. It is desirable to use a differential, balanced, current-drive technique. It is desirable that the output driver be capable of driving a terminated transmission line. The impedance of the transmission line is left to the chip designer's discretion. The driver must adhere to a standard, chosen at the chip designer's discretion, and interface on the receiving end to a commercially available chip set. Note that the maximum TRIGOUT rate is equal to the Fundamental Clock Frequency.

3. Specifications (Cont.)

3.4 Pipeline Section

- 3.4.1 The chip shall have a pipeline for storing the discriminator states and the Timestamp Counter bits. This is used to provide time delay for the case where the chip read out is triggered from an external trigger (Level 1 Trigger.) (See Section 3.5 for a description of the Timestamp Counter.)

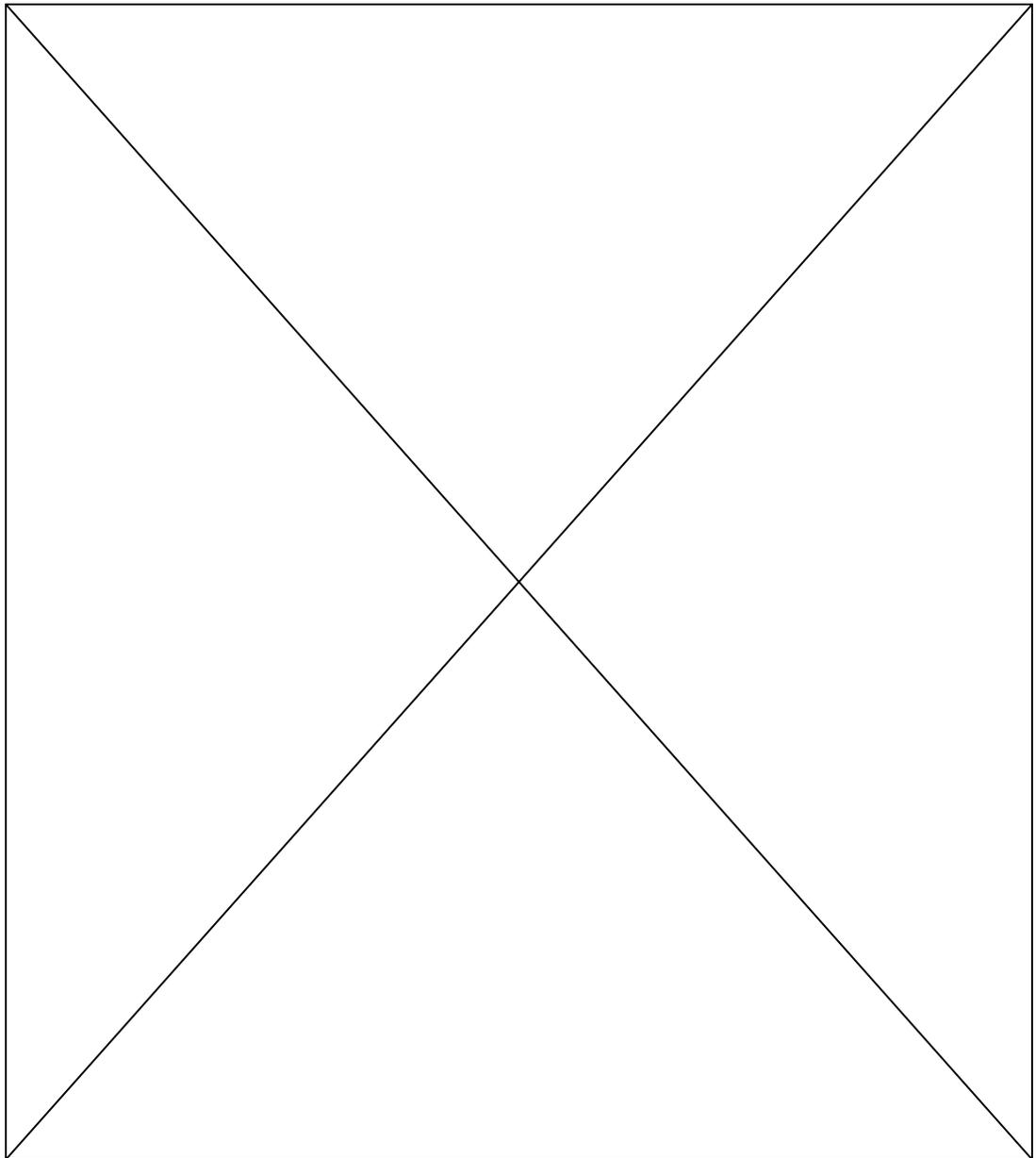


Figure 3.4.1. Configuration of the Pipeline Section

3. Specifications (Cont.)

3.4 Pipeline Section (Cont.)

- 3.4.2 Data written to the first stage of the pipeline shall be advanced to the next stages synchronously with the clock, using shift register techniques.
- 3.4.3 Data shall be advanced to subsequent pipeline sections on the rising edge of the clock.
- 3.4.4 When data is advanced to the end of the pipeline, it shall either be advanced to the next section of circuitry (the Readout Buffer), or not, depending on the result of the L1 trigger decision on that data. See Section 3.7.
- 3.4.5 The pipeline section shall be configured so that there are 512 clock cycles of delay. (At a 500 MHz clock rate, this corresponds to 1024 nanoseconds.)
- 3.4.6 The pipeline section must be capable of operation up to two times of the Fundamental Clock Frequency (see Section 3.1.)

3. Specifications (Cont.)

3.5 **Timestamp Section**

- 3.5.1 The chip shall have a 30-bit counter called the ***Timestamp Counter***, which counts clock cycles from a reference time. This will be used to correlate triggered events in time across the entire read-out system.

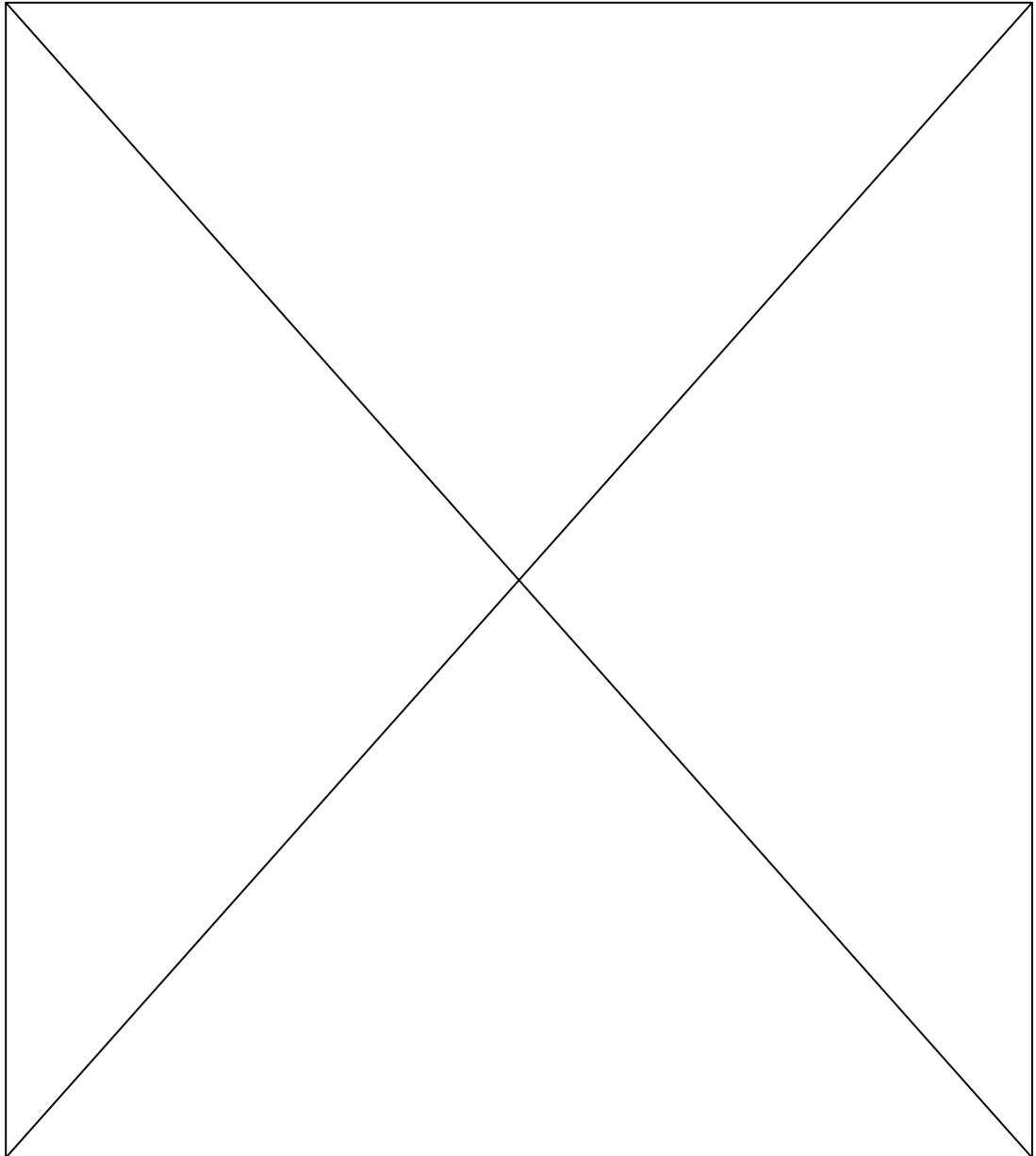


Figure 3.5.1. Timestamp Circuitry

3. Specifications (Cont.)

3.5 **Timestamp Section (Cont.)**

- 3.5.2 The Timestamp Counter shall be configured to advance on the rising edge of the clock (up-counter.) The ability to count down is neither required nor desired.
- 3.5.3 The Timestamp Counter must be capable of operation well in excess of the Fundamental Clock Frequency (see Section 3.1.)
- 3.5.4 The Timestamp Counter shall have a reset called **Counter Reset, or CNTRST**, provided from outside the chip. The reset signal shall be arranged as a synchronous clear with respect to the rising edge of the clock. The counter reset shall be provided as one of the functions of the control circuitry (see Section 3.9.)
- 3.5.5 The Timestamp Counter shall be configured to overflow gracefully, advancing from a full-scale count to 0 without glitch or error.
- 3.5.6 The output bits of the Timestamp Counter shall be written into the Readout Buffer when a Trigger Accept occurs (see Section 3.7), becoming part of the event data.

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3. Specifications (Cont.)

3.6 **Triggering Data for Readout - Trigger Control**

3.6.1 The discriminator states and the timestamp bits are clocked continuously through the pipeline section. An explicit state, the ***Level 1 Trigger Accept, or L1A***, is to be asserted in order to capture data from a particular period in time, to make the data available to be read out of the chip.

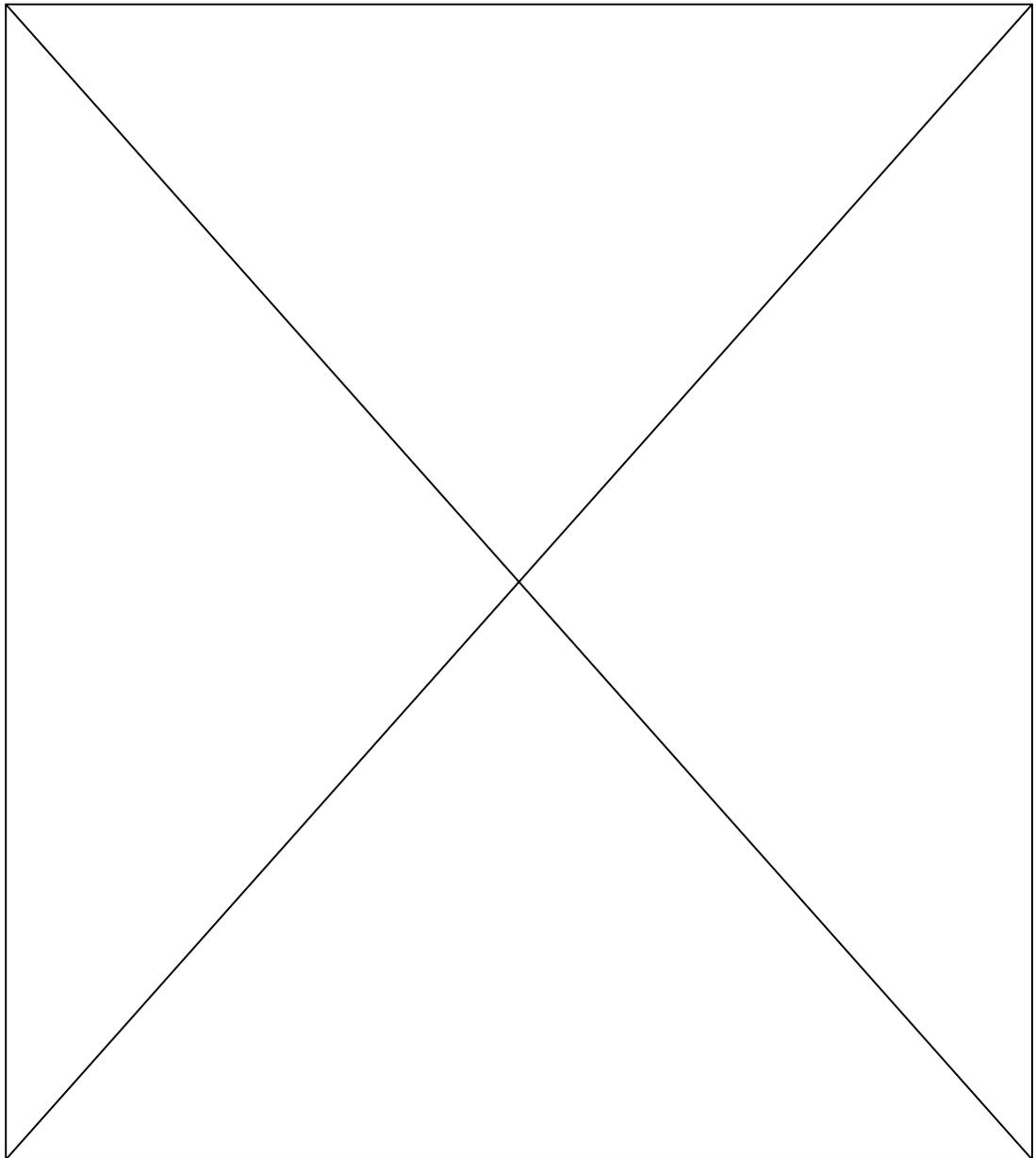


Figure 3.6.1. Triggering Data for Read Out

3. Specifications (Cont.)

3.6 Triggering Data for Readout - Trigger Control (Cont.)

- 3.6.2 The chip shall have two modes for determining how a L1A may be asserted. The particular mode, called L1SEL, is set through Slow Controls (see Section 3.9.)
 - 3.6.2.1 For L1SEL = 0, the chip shall use the internal trigger decision signal L0A (see Section 3.3.) In this case, the assertion of L0A shall cause data to be written from the output of the Pipeline Section into the Readout Buffer (see Section 3.7.) The timing must be arranged so that this action is delayed appropriately, to capture the event of interest as it emerges from the output of the pipeline.
 - 3.6.2.2 For L1SEL = 1, data from the output of the Pipeline Section shall be written into the Readout Buffer when an External Trigger Signal is received by the chip.
- 3.6.3 In both modes, data from the pipeline shall be written to the Readout Buffer synchronously with the clock, synchronized with the rising edge of the clock.
- 3.6.4 Data is acquired from the output of the Pipeline (see Section 3.4) and stored in the Readout Buffer (see Section 3.7) through the assertion of a signal **called Data Write, or DW**. This must be a prompt signal arising from the Trigger Accept state, arranged to capture the event of interest associated with a particular trigger.
- 3.6.5 It is desirable for External TRIGIN to be LVDS-compatible.

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3.7 Readout Buffer

3.7.1 ***Event data*** is defined as the state of all discriminators and the value of the Timestamp Counter at the end of a given clock cycle.

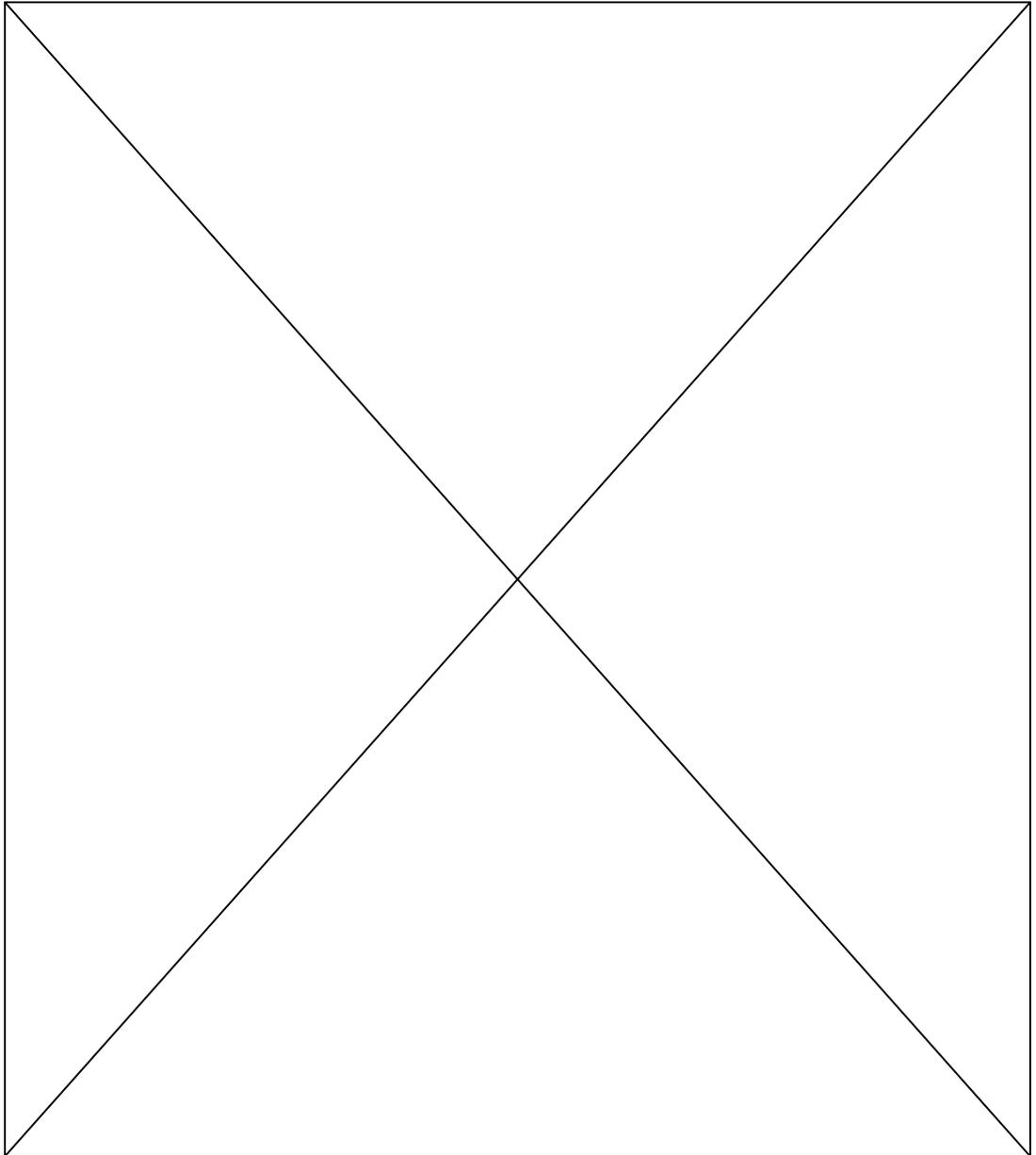


Figure 3.7.1. Readout Buffer Circuitry

3. Specifications (Cont.)

3.7 Readout Buffer (Cont.)

- 3.7.2 Event data shall be written into the Readout Buffer in response to the formation of a L1A Trigger Accept state (see Section 3.6.)
- 3.7.3 The Readout Buffer shall be capable of storing 16 events. The transmission of events out of the chip shall occur as a “first in, first out” (FIFO) process.
- 3.7.4 Once event data is written into the Readout Buffer, the transmission of data out of the chip shall be automatic, i.e. not dependent on external processes, communication, or intervention. See Section 3.8.

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3. Specifications (Cont.)

3.8 Data Output Driver

- 3.8.1 When one or more events are stored in the Readout Buffer, the chip shall execute operations to transfer event data to the Output Driver for transmission out of the chip, one event at a time.

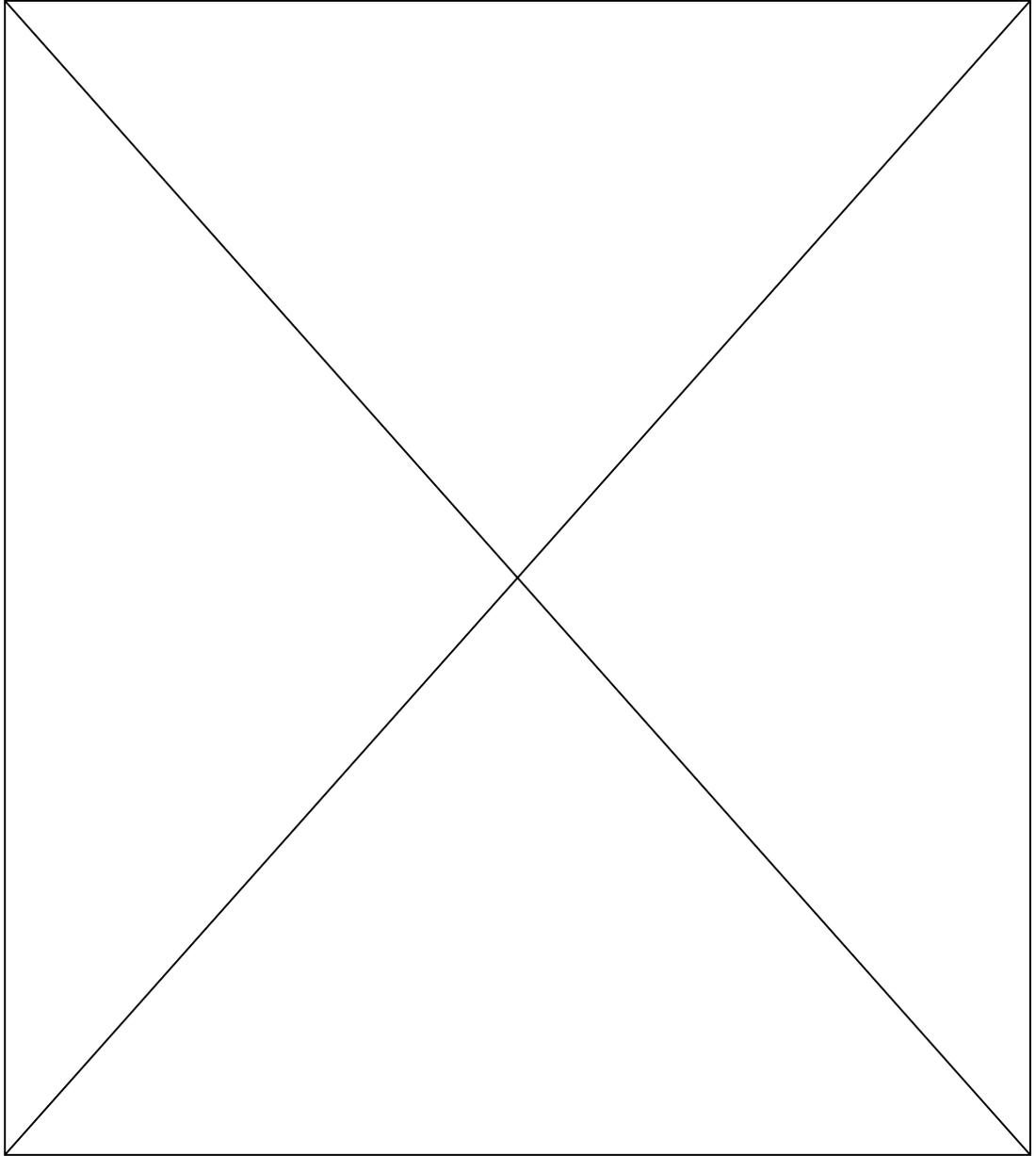


Figure 3.8.1. Output Driver Circuitry

3. Specifications (Cont.)

3.8 Data Output Driver (Cont.)

- 3.8.2 On-board control circuitry shall monitor the state of the FIFO in the Readout Buffer. If there is an event pending in the Readout Buffer, this control circuitry shall arrange to transfer data to the Output Driver when the Output Driver circuitry is in an idle state.
- 3.8.3 The data stored in the Readout Buffer is written to the Output Driver through the assertion of a signal called Data Read, or DR. Once data is transferred, it shall be cleared from the Readout Buffer, making memory space in the Readout Buffer available for a new event.
- 3.8.4 Data shall be transmitted out of the chip using a serial transmission format. This shall be a dedicated communication path, defined as the **Data Output**, and shall be independent and separate from chip control I/O (see Section 3.9.)
- 3.8.5 The chip must transfer an event out of the chip within 250 nanoseconds, to meet event rate requirements. This assumes that the receiver is capable of receiving data without any limitations from flow control.
- 3.8.6 The format of the serial transmission scheme shall be specified.
- 3.8.7 The data shall be self-clocking at the receiver, consistent with standard serial-transmission techniques.
- 3.8.8 The timing for the serial transmission shall be derived from the clock provided to the chip, operating at the Fundamental Clock Frequency. See Section 3.10.
- 3.8.9 The use of flow control or a handshake between the driver and receiver is not required. The readout of data from the chip shall use the concept of "data push," where data is not requested by the receiver but instead pushed out of the chip as it is acquired.

3. Specifications (Cont.)

3.8 Data Output Driver (Cont.)

- 3.8.10 The format of the data shall have a header that can uniquely be detected at the receiver, and identified as the beginning of the transmission of a new event.
- 3.8.11 The use of a trailer is not required, since the format of the data always has the same number of bits.
- 3.8.12 The hardware implementation of the serial transmission shall be at the chip designer's discretion. The driver must adhere to a standard, and interface on the receiving end to a commercially available chip set.

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3. Specifications (Cont.)

3.9 Control Section

- 3.9.1 Control of the chip shall be realized using a serial communication protocol. This shall be a dedicated communication path, defined as **Slow Controls**, and be independent of and separate from the Data Output (see Section 3.8.)

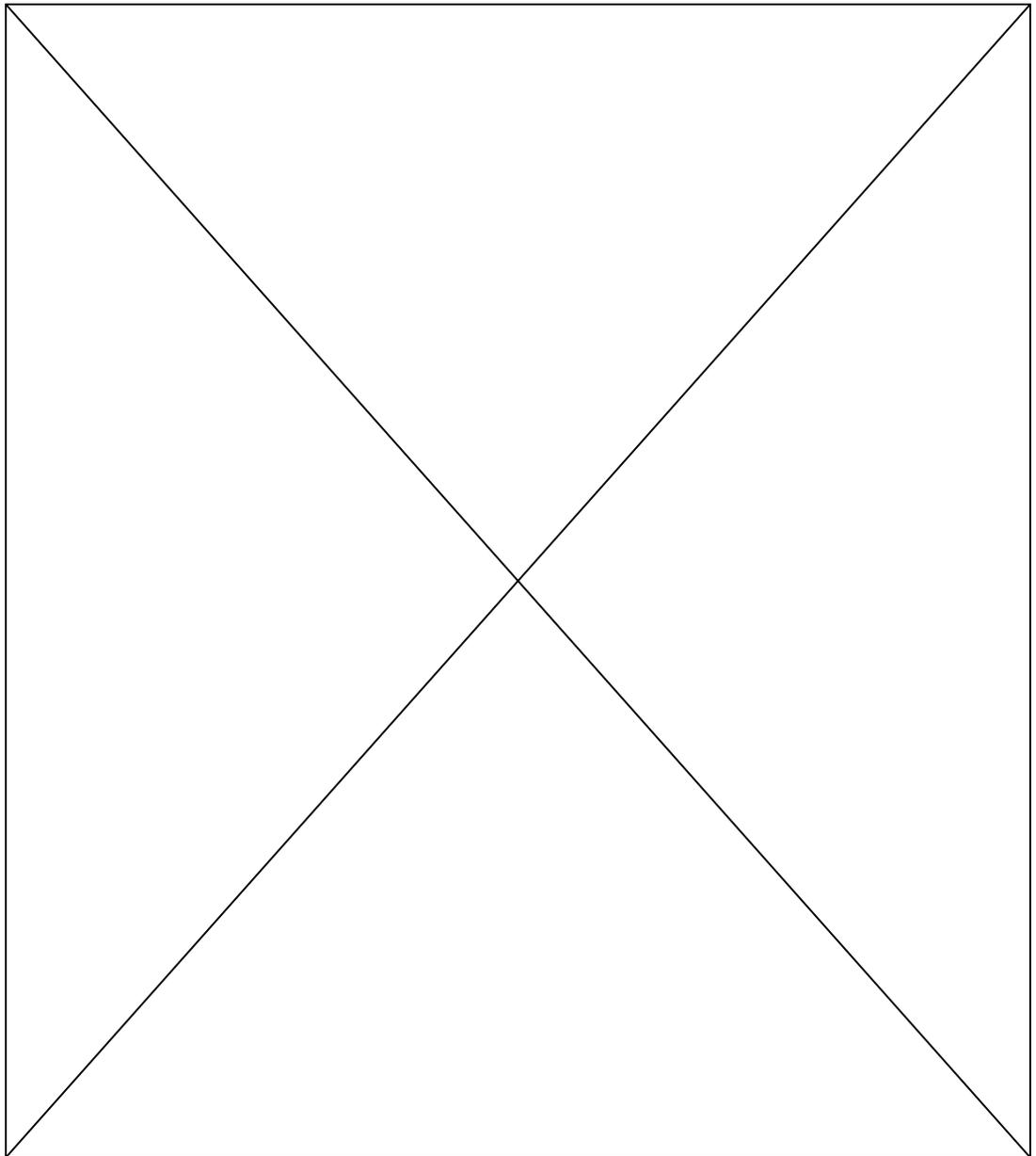


Figure 3.9.1. Output Driver Circuitry

3. Specifications (Cont.)

3.9 Control Section (Cont.)

- 3.9.2 The functions of the Slow Controls are not time-critical, and are related to writing or reading static control words to or from registers on the chip.
- 3.9.3 Control of the chip shall be realized with the use of registers, which are accessed via the Slow Controls :
 - 3.9.3.1 There shall be a **Control Register**, which shall control various modes of operation in the chip. These include LOSEL (see Section 3.3), LOWIN (see Section 3.3), and L1SEL (see Section 3.6).
 - 3.9.3.1 There shall be a **Threshold Register**, which shall control an on-board DAC for setting the threshold voltage for the discriminators. See Section 3.11.
 - 3.9.3.2 A **Mask Register** is needed, which is capable of turning off input channel discriminators at the front end. N bits are required, one for each discriminator channel.
 - 3.9.3.3 It is desirable to have a **QINJ Register**, which shall control the operation of an on-board charge injection circuit. See Section 3.12.
 - 3.9.3.4 It is desirable, but not required, to have a **Diagnostic Data Register**, capable of sending diagnostic data out of the chip through the data output driver. If implemented, the configuration should include a way to trigger such an event.
- 3.9.4 The Slow Controls shall be bi-directional, providing both read and write capability to all registers implemented. The chip should be regarded as a slave with respect to the Slow Controls, where control of the read/write states is assumed to reside outside the chip.
- 3.9.5 The format of the serial transmission scheme shall be specified.

3. Specifications (Cont.)

3.9 Control Section (Cont.)

- 3.9.6 The data shall be self-clocking at the receiver, consistent with standard serial-transmission techniques.
- 3.9.7 The timing for the serial transmission shall be self-derived from the Slow Controls transceiver. It is desirable for this clock to be synchronous with the Fundamental Clock Frequency, where the framing of data bits sends an integer number of bits in one clock cycle. See Section 3.10.
- 3.9.8 The use of flow control or a handshake between the driver and receiver is desirable.
- 3.9.9 The format of the data shall include both address and data. The format should have a header that can uniquely be detected at the receiver, and identified as the beginning of the transmission of new data.
- 3.9.10 The use of a trailer is not required, if the format of the data always has the same number of bits.
- 3.9.11 The hardware implementation of the serial transmission is at the chip designer's discretion. The transceiver must adhere to a standard, and interface on the receiving end to a commercially available chip set.

3. Specifications (Cont.)

3.10 Clock Specifications

- 3.10.1 The chip shall have one clock signal delivered to it as an input signals, called **TCLK**, operating at the Fundamental Frequency of Operation, with a 50% duty cycle.
- 3.10.2 The chip shall use TCLK to produce the Serial Data Output Clock, which shall be equal to the Fundamental Frequency of Operation. This shall be used by the output driver circuitry in the Data Output to drive data out of the chip.
- 3.10.3 The chip shall use TCLK as the clock for the Timestamp Counter, as well as the clock for other synchronous activity in the chip.
- 3.10.4 The digital functions of the chip operate synchronously, with state changes occurring on the rising edge of the internal clock.
- 3.10.5 The rise and fall times of the internal clock for the Timestamp Counter shall be less than 5% of the Fundamental Clock Frequency.
- 3.10.6 The jitter of the internal clock for the Timestamp Counter shall be less than 2% of the Fundamental Clock Frequency.
- 3.10.7 The jitter of the Serial Data Output Clock shall be less than 2% of the Fundamental Clock Frequency.
- 3.10.8 The temperature stability of the phase of the internal clocks for both the Timestamp Counter and the Serial Data Output Clock shall not be worse than 0.2 nSec/Degree C.
- 3.10.9 Chip-to-chip variations of the phase of the internal clock for the Timestamp Counter, assuming identical clock source circuitry and transmission lengths, shall be better than 5% of the Fundamental Clock Frequency.

3. Specifications (Cont.)

3.10 Clock Specifications (Cont.)

3.10.10 It may be desirable to implement a Phase-Lock Loop (PLL) in the chip, in order to meet clock performance specifications. This is left to chip designer's discretion.

3.10.11 The other time-critical functions are as follows:

3.10.11.1 Counter Reset for the Timestamp Counter shall be provided to the chip. This needs to be a precision signal, capable of being synchronized across the entire system on a given clock cycle. The system must have the capability to send a Counter Reset on any given clock cycle. It is acceptable to implement this signal either as a dedicated signal pair provided to the chip, or as part of the Slow Controls. The protocol may have one or more clock cycles of delay from the time that the Counter Reset command is received to when it is actually asserted at the Timestamp Counter. However, any such delay must be a constant, and uniform from chip to chip.

3.10.11.2 It is desirable to implement a global Charge Injection Command (see section 3.12.) If implemented, it is desirable for it to be a precision signal, synchronized across the entire system on a given clock cycle. It is acceptable to implement this signal either as a dedicated signal pair provided to the chip, or as part of the Slow Controls. The protocol may have one or more clock cycles of delay from the time that the Charge Inject Command is received to when charge injection actually occurs. However, any such delay must be a constant, and uniform from chip to chip.

3. Specifications (Cont.)

3.11 Threshold DAC

- 3.11.1 The least count resolution of the Threshold DAC must correspond to a minimum of 10% of the smallest signal size, reflected in the equivalent output voltage of the DAC.
- 3.11.2 It is desirable for the range of the Threshold DAC to be capable of discriminating on signals approximately 50 times larger than the smallest signal size, reflected in the equivalent output voltage of the DAC.
- 3.11.3 For this application, the requirements for differential and integral nonlinearity of the DAC output voltage as a function of digital code are not critical. The DAC voltage should be monotonic, over the range, with no missing codes.
- 3.11.4 The requirements of 3.11.1 through 3.11.3 imply approximately 7 bits of dynamic range.
- 3.11.5 The voltage levels of the DAC are left to the chip designer's discretion, to meet the other performance specifications.
- 3.11.6 It is desirable for the DAC to have an on-board reference. If implemented, the noise and stability of the reference, and the DAC itself, must be such that DAC voltage stability and noise are less than one DAC count in equivalent voltage. The alternative is to provide the reference voltage to the chip from an external source using an I/O pin.
- 3.11.7 It is requested that both the DAC voltage and the reference voltage be brought out of the chip as test points.

3. Specifications (Cont.)

3.12 Charge Injection

- 3.12.1 It is desirable for the chip to have the capability to inject charge into the front-end amplifier.
- 3.12.2 At a minimum, capability should exist to inject charge at one known, stable value. If implemented this way, a value should be chosen to function above minimum threshold settings.
- 3.12.3 It is desirable, but not required, to have the capability to inject charge over a range of value. This would facilitate the mapping and calibration of the discriminator as a function of the threshold voltage. This might be implemented using a DAC to set a voltage on a capacitive discharge circuit.
- 3.12.4 A means should be provided to fire the charge injection circuit. It is desirable for this to be provided as a timing signal, defined as the **Charge Inject Command**, to facilitate the firing of two or more chips simultaneously across the system. (This is desirable to test the timing of Timestamp Counter.) If implemented this way, the Charge Inject Command should be incorporated through Slow Controls, and be treated in a similar way as Counter Reset (see Section 3.9.)

3. Specifications (Cont.)

3.13 Power and Packaging

- 3.13.1 The power supply levels are left to the chip designer's discretion. It is desirable for the chip to use a minimum number of external supplies, and to be common voltages.
- 3.13.2 It is desirable for the chip to have a large range of insensitivity to power supply variation, so that local, external regulation is not required.
- 3.13.3 It is desirable for the power dissipation of the chip to be ~2-3 mW per channel, averaged over the entire chip, when operated at the Fundamental Clock Frequency. Power dissipation should not exceed 5 mW per channel, averaged over the entire chip.
- 3.13.4 The device should be packaged such that it can be assembled onto a printed circuit board using "conventional" techniques, such as SMT assembly or BGA technology.
- 3.13.5 The height of the packaged chip from the assembly surface is not critical.

4. Bibliography