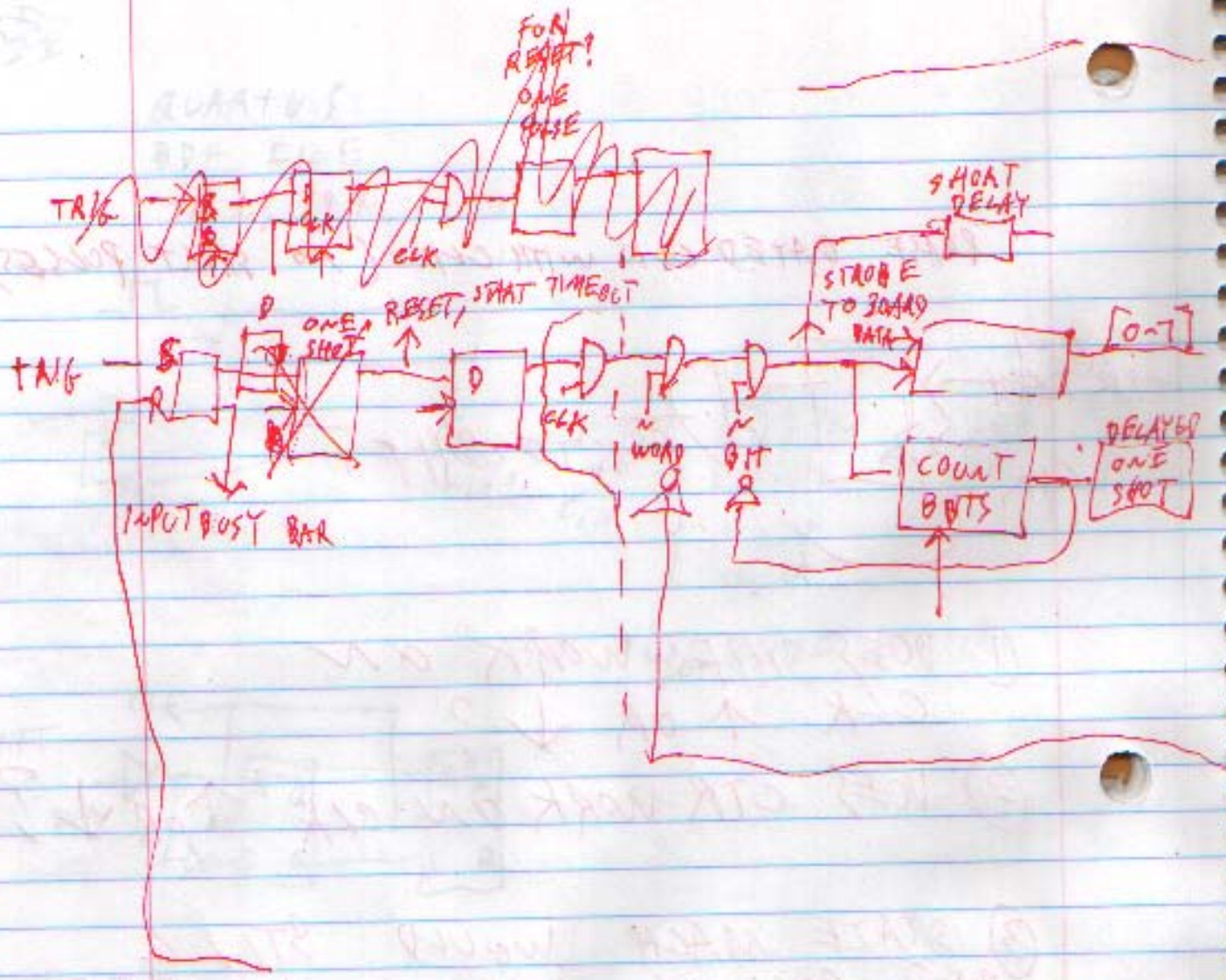
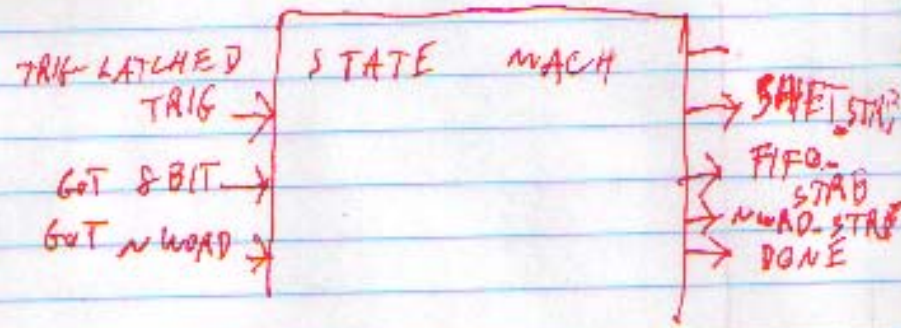
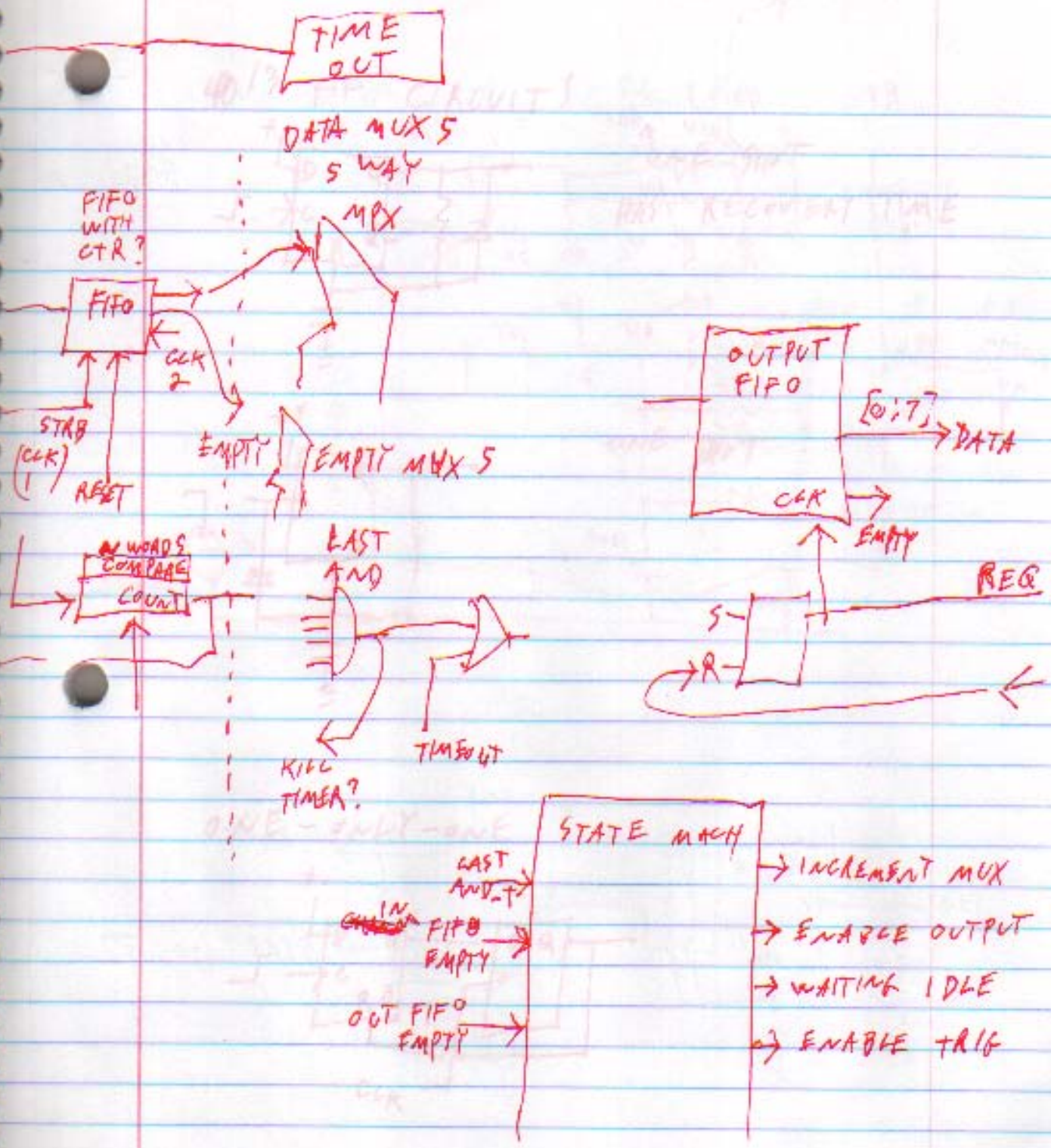


MOVE DOTTED LINE LEFT
SO EITHER STATE MACH
OR DISCRETE LOGIC
CAN BE USED

WHERE IS RESET?



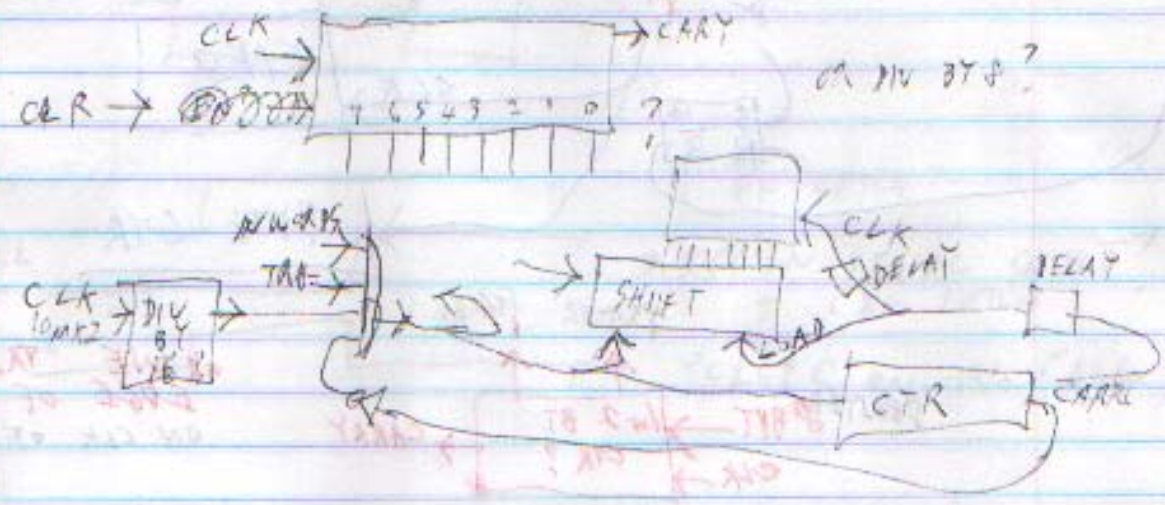


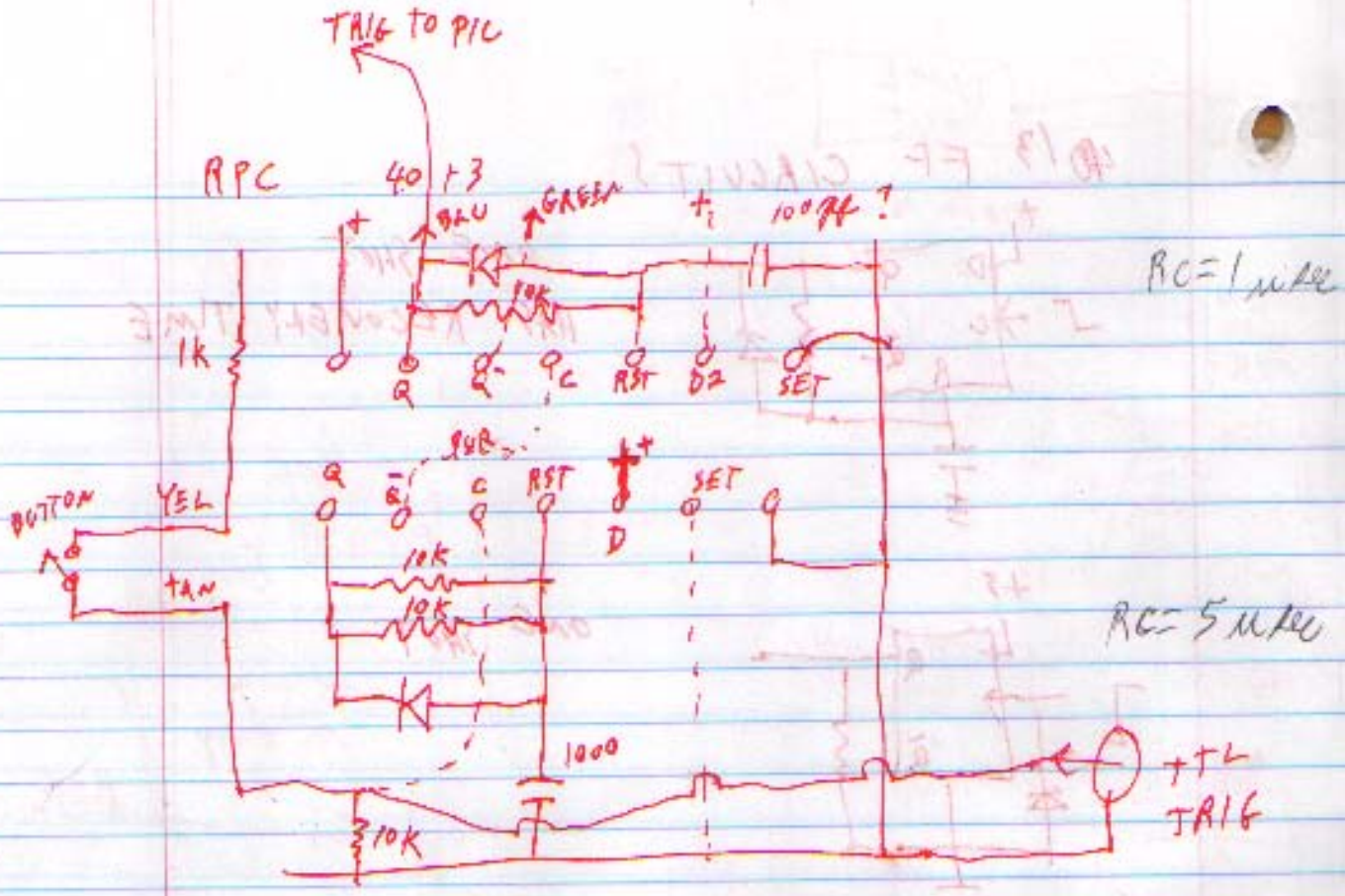
~~EITHER COUNT N_1 N_2 WORDS INTO MUX~~
OR HAVE COUNTER ON EACH FIFO GO TO Ø

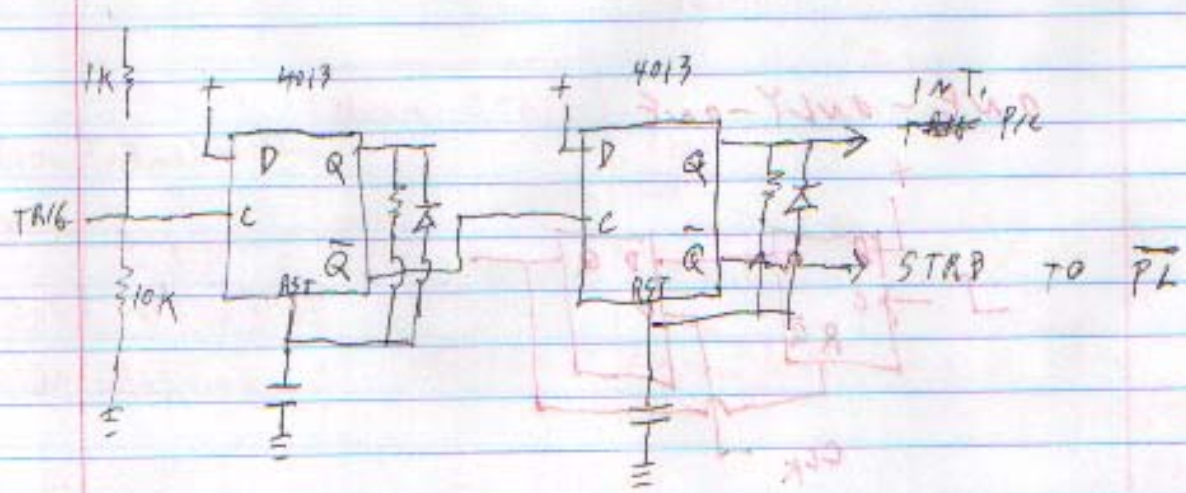
FILE
NEW
BLOCK DIAGRAM / SCHEMATIC

R CLICK IN WINDOW
EDIT INSERT SYMBOL

COUNTER
DECODED UP TO 16
ALSO HAS EQ N OUTPUT (ONLY FOR > 16 ?)

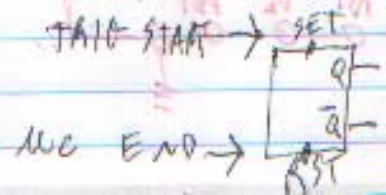






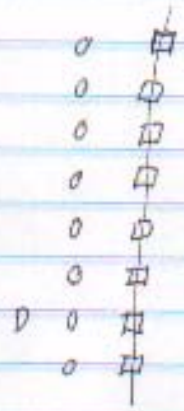
LOOK AT MC CODE

SEE IF A PIN IS FREE FOR BUSY RST

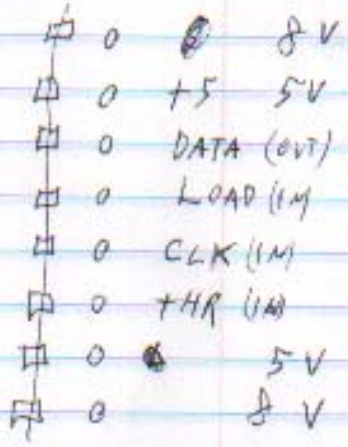


CONNECTOR ON 256 BD

COMPONENT
(BACK OF CONN)



CONNECTOR
SIDE



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HOROWITZ AND HILL

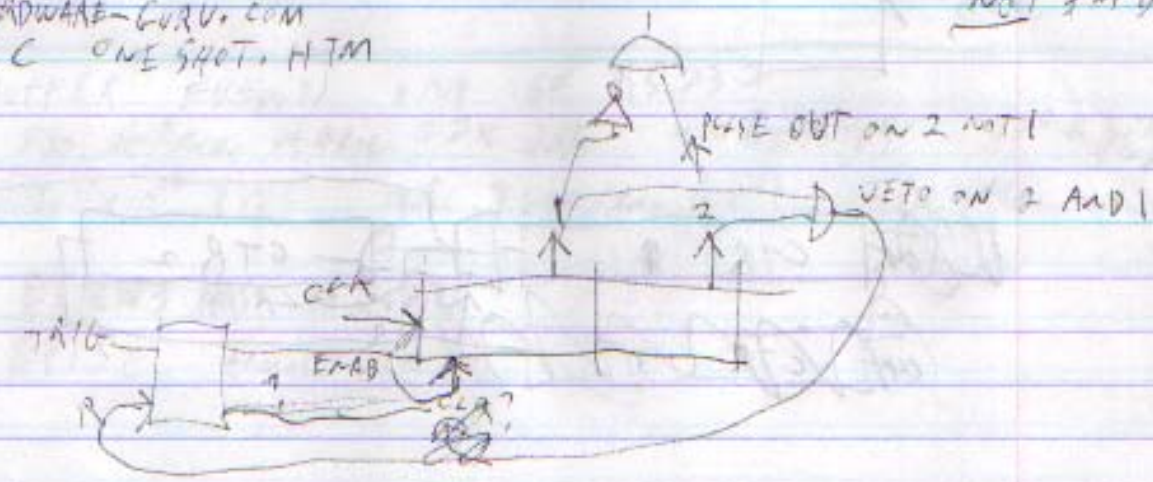
DUGBEAT. ABEBOOKS.COM
25.47 + 6.50 SHIP
79

PATENT 6710622 ?
~~4644547~~

N BIT CTR CLOCKE ALL TIME

ENABLE OR CLEAR
OR BOTH ?
CONTINUOUS CLR
WOULD = NOT ENABLE

HARDWARE-GURU.COM
5C ONESHOT.HTM



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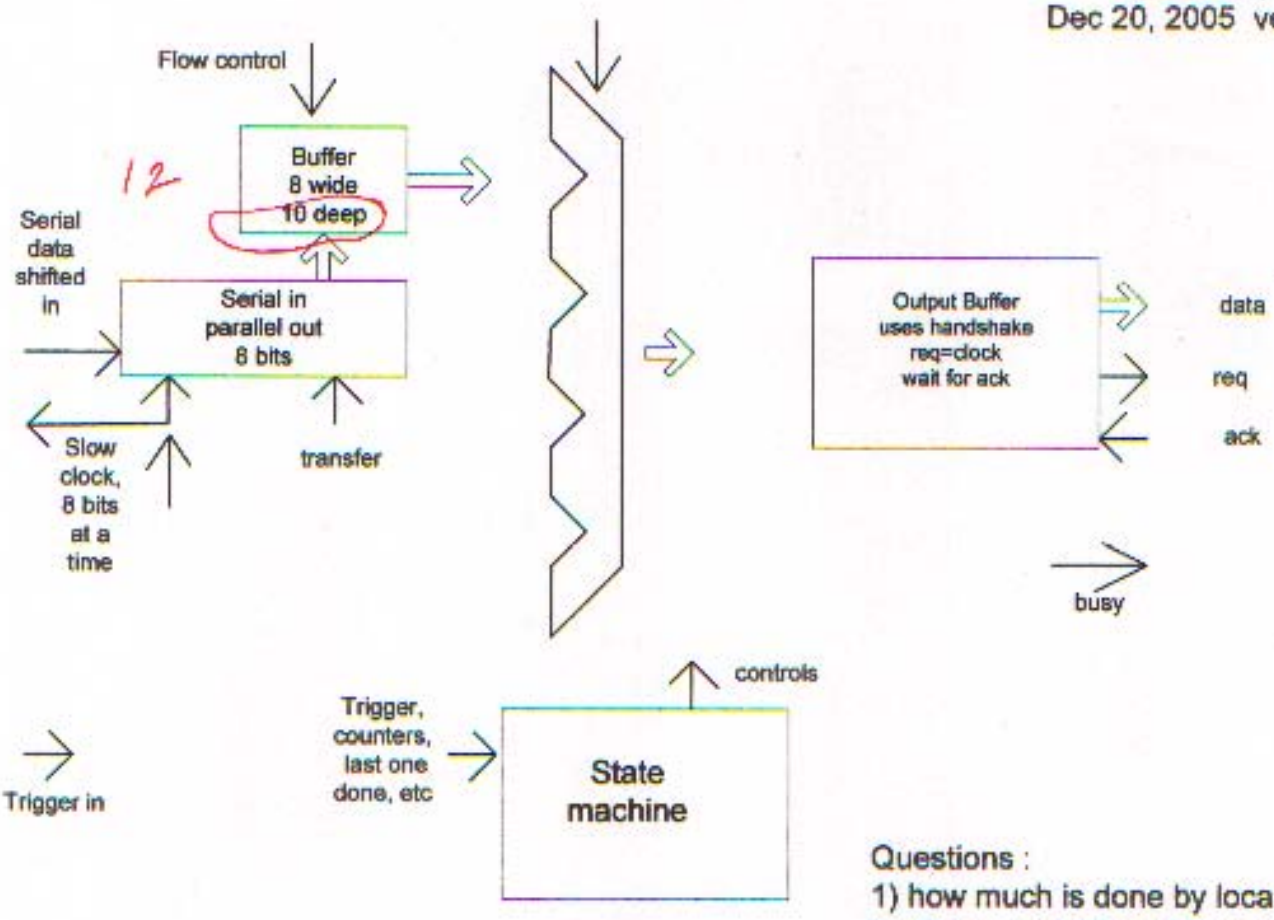
AUTHORIZATION # 100-107-629
PASSWORD HAWK # MXSS

5 channel shift register readin system
to implement in smallest ~~Stratix~~
~~(EP1S10)~~
Dec 20, 2005 version

One of 5 input channels



Features:
1) trigger input
2) busy output
3) handshake mode output buffer
(8 bit wide, req=data clock, wait for ack
4) different number of bytes in each of five serial input channels (eg 4, 8, 9)
(start mpx after longest one done)
5) 5 way mpx to send input buffers to output buffer.
6) Serial shiftin at 1/2 MHZ , sending clock out and reading bit in after delay
7) output at roughly 2 MHz using handshake

Questions :
1) how much is done by local hardware control, and how much by a state machine?
eg,
a) stopping shifitin clock after 8 bits, transferring parallel 8 bits to buffer, starting serial input for another 8 bits, counting number of bytes to quit
b) after longest input is done, start mpx all 5 chan data to output buffer at high clock rate to minimize dead time
c) when all input buf have been transferred to output buf, start handshake, and control transfers with handshake to keep rate at roughly 2 MHz (maybe release input busy signal during this ?)