

American Linear Collider
Physics Group

**Conceptual Design
of the
Amplifier/Discriminator/Timestamp (ADT) ASIC**

Gary Drake, José Repond, Dave Underwood, Lei Xia
Argonne National Laboratory

Charlie Nelson
Fermilab

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Contents

1. Introduction	p. 3
2. Overview	p. 5
3. Specifications	p. 9
3.1 General	p. 9
3.2 Amplifier/Discriminator Section	p. 10
3.3 Internal Trigger Decision Formation	p. 19
3.4 Pipeline	p. 21
3.5 Timestamp Section	p. 23
3.6 Triggering Data for Readout – Trig Control	p. 25
3.7 Readout Buffer	p. 27
3.8 Data Output Driver	p. 29
3.9 Control Section	p. 32
3.10 Clock Specifications	p. 36
3.11 Threshold DAC	p. 37
3.12 Charge Injection	p. 38
3.13 Power and Packaging	p. 39
4. Bibliography	p. 40

1. Introduction

A new approach is emerging in the instrumentation of detectors for calorimetry. Traditionally, calorimeters have been designed to measure the energy deposition over a wide dynamic range. This is often done by digitizing signal pulse height (integrated current) using an ADC having 12 to 18 bits of dynamic range. Because large dynamic range is often expensive, cost/performance trade-offs usually result in each read-out channel servicing a rather large part of the fiducial volume of the detector, often including many sampling layers in transverse depth.

For the Linear Collider, it is important to be able to measure jets with excellent energy resolution. Significant improvement in jet energy resolution over what has been obtained with previous detectors can be achieved by applying a technique known as *Particle Flow Algorithms*. By utilizing the information from both the tracking systems and the calorimeter, these algorithms rely on the correct assignment of the energy deposits in the calorimeter to the different components of a jet, i.e. due to charged or neutral particles. The Particle Flow Algorithms work best when the detector components are specifically optimized for this technique. A requirement is that the calorimeter have extremely fine segmentation, on the order of one square centimeter, both laterally and layer-by-layer longitudinally. This fine segmentation results in a large number of electronic readout channels, and renders a high-resolution measurement for each channel impractical. This leads to the consideration of a simple digital readout, where the dynamic range of a single channel is reduced to a small number of bits. In fact, Monte Carlo simulations have shown that it is possible to preserve the energy resolution of single hadronic particles using a simple discriminator with only one threshold – a 1-bit ADC! In essence, this approach trades wide dynamic range on a small number of channels, for low dynamic range on a large number of channels.

This document describes the conceptual design of a new custom application-specific integrated circuit (ASIC) that might service several different kinds of detectors designed specifically to use particle flow algorithms. At the present time, several new detectors are being considered that would use this technique, and there is interest in using the custom chip described. These include:

A. Resistive Plate Chambers (RPCs) for the Hadron Calorimeter of the Linear Collider

This detector would use 1 cm x 1 cm pads to read out RPCs made from glass. The RPCs would be operated in avalanche mode (as opposed to streamer mode), where the smallest signal to measure is approximately 100 fC. The pads are arranged in a square array. A convenient grouping of channels would be 8 by 8 pads, or 64 channels per chip. The chips would reside directly on the RPCs. (See [1-10] for a description of RPC detectors.)

B. Gas Electron Multipliers (GEMs) for the Hadron Calorimeter of the Linear Collider

The read-out configuration of this detector would be similar to that of the RPCs described above. It would also use 1 cm x 1 cm pads for read-out. The smallest signal to measure is approximately 5 fC. Like the RPCs, a convenient grouping of channels would be 8 by 8 pads, or 64 channels per chip. The chips would reside directly on the read-out pads. (See [11-19] for a description of GEM detectors.)

C. Resistive Plate Chambers (RPCs) for the NUMI Off-Axis Detector

This detector would use 2 cm x ~20 m strips to read out RPCs made from glass. The RPCs for this detector would be operated in streamer mode, where the signals are relative large, on the order of 1-2 pC. The sampling layers would be arranged in alternating "X" and "Y" configurations. The chips would reside on the outer edge of the detector. Because the strips are relatively long, the chip would need to terminate the transmission line formed by the strips to prevent reflections. It is also desirable for the chip to receive the signals differentially to reduce noise pick-up.

D. Scintillator for the Hadron Calorimeter of the Linear Collider

This detector would use ~10cm² scintillator tiles with an inlaid wavelength shifting fibers. The newly developed Silicon-Photomultipliers have been proposed as the readout device. These devices will be located close to the tiles, thus avoiding the need to transport the light over long distances using clear fibers. The signals from these devices are similar in shape and magnitude to that obtained from RPCs in avalanche mode. (The requirements on the instrumentation for this detector shall be assumed to be the same as that for RPCs in avalanche mode is the description that follows.)

The three applications described above have several important differences. It is envisaged that the differences might be accommodated using circuitry that can be configured at the front end of the chip. A proposed method is described in the description that follows.

2. Overview

A conceptual block diagram of the device under consideration is shown in Figure 2.1. The operation can be divided into several functional blocks, which will be described.

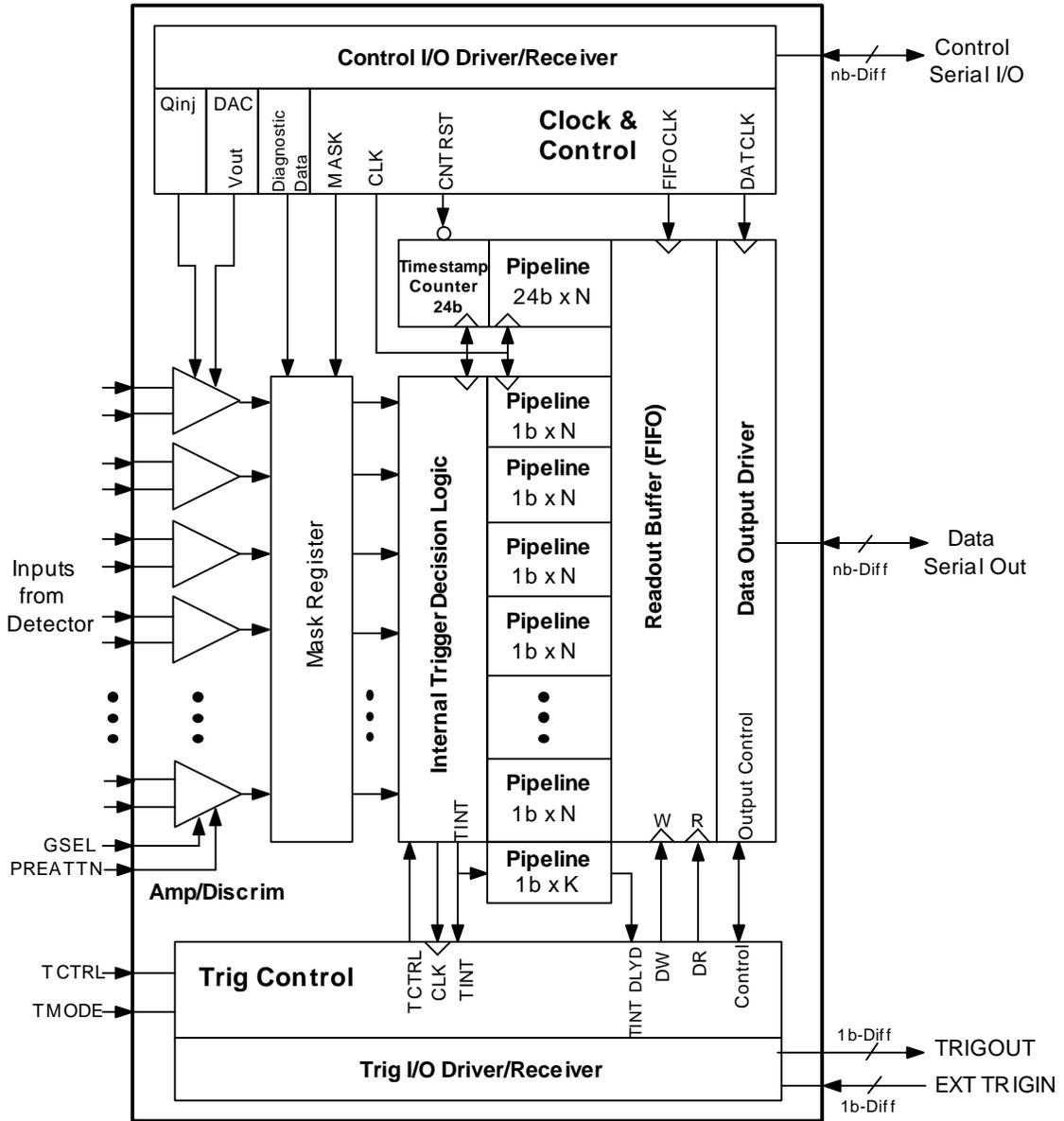


Figure 2.1. Block Diagram of ASIC

2. Overview (Cont.)

Signals from the detector are charge or current pulses. When a signal is received from the detector, it is amplified and shaped. It is then passed to a discriminator, where it is compared to a threshold voltage. If the signal level exceeds the threshold level, then the discriminator would fire. The discriminators are evaluated using a clock provided to the chip from outside. The discriminators must hold the state of the response until the end of the clock cycle (defined to be the rising edge), so that the state of the discriminators can be latched into the circuitry that follows. Care must be exercised so that small pulses that fire a discriminator briefly will cause the discriminator to latch even if the signal level falls below threshold before the end of the clock cycle.

In order to reconstruct hits in the DAQ, the chip shall provide an event ID for each hit. The chip uses the concept of a Timestamp Counter to accomplish this. It is essentially a free-running counter, which is reset periodically (~ once per second.) The counter is advanced by the clock provided to the chip. Since the data is tagged with an event ID at the front end, the constraints on the system for bringing together event fragments in time are greatly reduced.

Both the Timestamp Counter bits and the discriminator states define event data. They are written into a pipeline, and are advanced through the pipeline by the clock. At the end of the pipeline, a decision must be made whether or not to keep the event data. This decision, called the Trigger Accept, causes the bits to be written into an output buffer, which is configured as a FIFO. From there, circuitry in the chip is activated that reads the event data from the output buffer, and sends it out of the chip.

The chip would have two ways to capture event data. The first way uses an external trigger, provided from outside the chip. The second uses on-board circuitry to make a trigger decision internally. The circuitry would evaluate the states of the discriminators, and arrange for a Trigger Accept to capture the data associated with the trigger decision as the data emerges from the end of the pipeline. The chip also uses the internal trigger to send a trigger signal out of the chip, for use by an external trigger system. The trigger output and external trigger input would be configured as individual output lines.

The data output is envisaged to use a serial communication protocol. It is a dedicated link, and uses a "data push" configuration. It is not necessary for this link to be bi-directional. It is desirable to have the capability for flow control, in case the receiver becomes busy. Other details, such as format, error correction or detection, start and stop bits, framing, headers, etc. are described.

2. Overview (Cont.)

Control functions of the chip are handled by a dedicated interface called the Control Communication Link. It also uses a serial communication protocol, although it may utilize several signal lines. This link has several functions. The most important is the clock. The link is envisaged to provide the basic clock frequency, and interleave bi-directional data along with it. Besides the clock, there are two other timing signals that must be incorporated into the communication protocol: Counter Reset must be a precision signal (to within one clock cycle), as it is used to synchronize timing of all chips in the system. The other timing signal would be used to inject charge into the front end amplifiers. This protocol, where data is interleaved with a fundamental clock frequency, might be similar to that used by commercial devices, such as the HOTLINK chip set.

The control section of the chip must also provide several other functions. The chip needs an on-board DAC to generate the threshold voltage for the discriminators. It is thought that a 6-bit DAC would provide adequate sensitivity for the range of signals that the chip would process. It is desirable for the chip to incorporate an on-board voltage reference, although concerns about stability and accuracy may make it necessary to have it be off chip.

An important control feature is the ability to mask off bad channels. This is needed to prevent noisy channels from co-opting the readout bandwidth. This could be incorporated by using a simple AND gate with the output of each discriminator. The masking would be accomplished by loading a "Mask Register" through the control link.

Another control function is the control of charge injection. The ability to inject charge is useful for testing the basic signal processing circuitry. By providing the capability of injecting charge at a precise time over many parts of the system, the synchronization of the chip counters could be tested. If the charge injection circuitry were further enhanced to incorporate a DAC, it would be possible to study the sensitivity of the discriminators as a function of threshold voltage setting versus value of the charge injected. Clearly the latter features represent a more complex design, and are open for discussion.

Lastly, a feature that is desirable but not required is the ability to send diagnostic data through the chip. This could also be accomplished by loading a register, and diverting the diagnostic data through the signal-processing path.

2. Overview (Cont.)

To summarize, the chip described has many functional blocks, but most of them are relatively straight-forward to implement. There are three primary challenges in this design:

1. The chip is a mixed analog/digital design, containing charge-processing circuitry with moderately-high gain. It is important to prevent digital noise from being picked up by the sensitive analog circuitry. On the plus side, the major portion of the chip contains digital circuitry that is relatively straight-forward in function and complexity. The analog circuitry represents a relatively small portion of the design, and can be constrained to a small portion of the floor plan. The low dynamic range (a 1-bit ADC) also helps to ease the design challenge.
2. The performance of the chip relies on the use of a minimum number of digital I/O signal lines, where the use of serial communication protocols is desired. Serial communication is more difficult than parallel communication, especially where handshakes or flow control are implemented. Bi-directional protocols also represent a design challenge. It is desirable to incorporate a robust, reliable communication protocol, but the design must weigh and balance the overhead in complexity. The scheme to interleave clock and control information may represent a design challenge, but several good examples exist in the current technology, which might be used as guidance.
3. The approach to this type of detector and the associated instrumentation trades large dynamic range for a large number of channels with low dynamic range. It is desirable to incorporate as many channels as possible in the chip design. The preferred number is 64 channels, with 32 channels as a second choice. There may be aspects of the design or fabrication that suggest an optimum number, perhaps different from the above. With the goal of having as large a number of channels as possible, the realization is left to the chip designer's discretion.

The chip has many features, some of which are required, while others are optional or desirable. It is clear that the realization of this design must be a collaborative effort. Input and feedback from the chip designers are necessary and important. It is expected that this specification will be iterated upon as necessary to achieve a design that is well-engineered, and meets the performance goals of the experiments.

3. Specifications

3.1 General

- 3.1.1 The intended frequency of operation for the chip, including timing, pipeline operation, and time frame formation for the serial drivers, shall be 10 MHz. This is defined as the ***Fundamental Frequency of Operation***. In general, it is expected that the chip be capable of operation up to, or in excess of, 40 MHz without failure or error. See Section 3.10 for timing specifications.
- 3.1.2 The digital functions of the chip are intended to operate synchronously with respect to the clock.
- 3.1.3 This specification describes the design of a mixed analog/digital chip. In certain modes of operation, low-noise analog design techniques are required. The semiconductor fabrication technology and specific design and implementation details are left to the chip designer's discretion.
- 3.1.4 The chip shall service a minimum of 32 detector channels. If possible, it is desirable to implement 64 channels per chip.

3. Specifications (Cont.)

3.2 Amplifier/Discriminator Section

3.2.1 The Amplifier/Discriminator Section performs the analog signal processing in the chip. The outputs are digital signals.

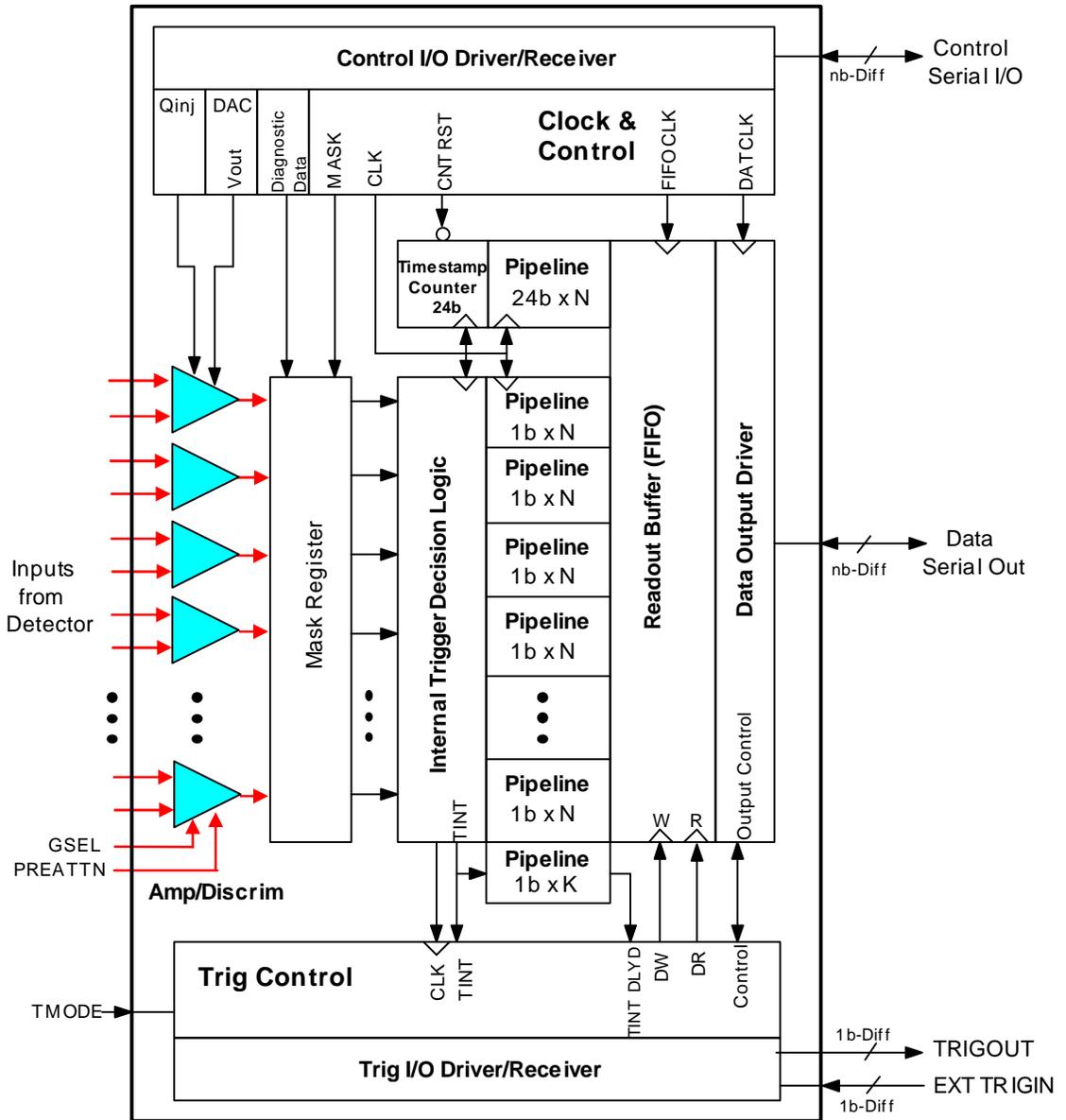


Figure 3.2.1. Amplifier/Discriminator Section

3. Specifications (Cont.)

3.2 Amplifier/Discriminator Section (Cont.)

3.2.2 The Amplifier/Discriminator Section can be divided into three functional blocks, as shown in Figure 3.2.2.

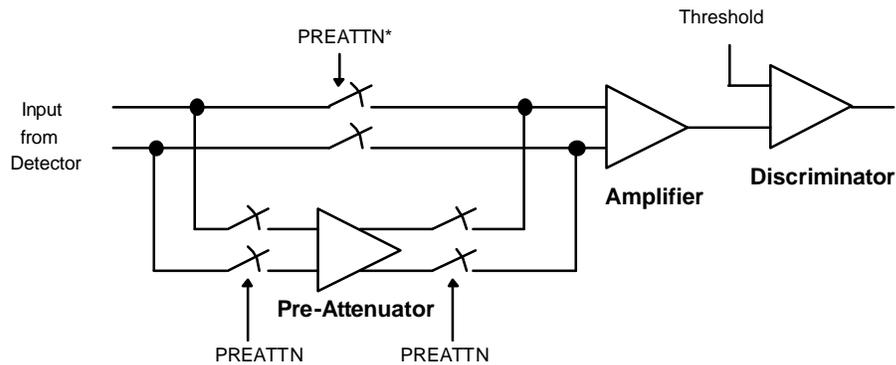


Figure 3.2.2. Amplifier/Discriminator Block Diagram

3.2.2.1 The primary function of the amplifier is to receive and amplify charge pulses from the detector, and produce an output voltage that is proportional to the total charge received. The amplifier may also provide shaping for the output voltage signals. It is intended to use the amplifier directly with RPC avalanche and GEM signals (see Section 1.)

3.2.2.2 The primary function of the discriminator is to receive a voltage from the amplifier, and compare it to a threshold voltage provided on-board the chip. If the amplifier voltage is greater than or equal to the threshold voltage, then the output of the discriminator shall be asserted to the logic 1 state. Otherwise, the output of the discriminator shall be asserted to the logic 0 state, which is also defined to be the "Rest State." Note that the discrimination process acts on the total charge received from the detector.

3.2.2.3 The primary function of the Pre-Attenuator is to provide the capability to attenuate the input signal, for the case where the signals are from streamers in RPCs (see Section 1.) It has the feature that it can be switched in or out of the signal path. The Pre-Attenuator has other properties for working with RPC streamer signals, as described in Section 3.2.5.

3. Specifications (Cont.)

3.2 Amplifier/Discriminator Section (Cont.)

3.2.3 The Amplifier Section has the following properties:

3.2.3.1 The front-end amplifier must be capable of receiving, amplifying, and processing signals from the detectors. The signals are current pulses in nature (i.e. high source impedance at DC.) The amplifier must be capable of processing current pulses that are negative in the conventional sense (electrons are sourced from the detector).

3.2.3.2 The output of the amplifier is a voltage, which is proportional to the total charge received in a pulse from the detector. The output voltage is passed to the discriminator section, to be compared to a threshold voltage.

3.2.3.3 It is necessary to record hits from the detector promptly. Consequently, the rise-time of the amplifier is important. The closed-loop, -3 db bandwidth of the amplifier shall be such that the rise-time of the amplifier is less than or equal to 10% of the period of the Fundamental Clock Frequency, or 10 nS, whichever is greater.

3.2.3.4 The maximum rate at which a channel will receive signals from the detector is on the order of 1 KHz. Shaping and recovery times should be designed to avoid pile-up or baseline shifts.

3.2.3.5 It is acceptable for the input voltage of the amplifier to have a non-zero bias within one or two volts, provided that it is compatible with the Pre-Attenuator circuit (see Section 3.2.4.) The detector performance will not be affected at these levels.

3.2.3.6 It is acceptable to use AC-coupling between the output of the amplifier and the discriminator, in order to reduce sensitivity to baseline shifts or channel-to-channel variations in output voltages. This is contingent on meeting recovery criteria (see Section 3.2.3.4), and for the relaxation transients to not affect the performance of the discriminator.

3. Specifications (Cont.)

3.2 Amplifier/Discriminator Section (Cont.)

3.2.3 The Amplifier Section has the following properties (cont.):

3.2.3.7 It is necessary for each channel to have a specific signal return connection to the detector that corresponds to the signal input from the detector. The amplifier may be configured to have a single-ended input with respect to signal return to the detector. In this case, it is necessary for the amplifier to have a reference (analog ground) to the signal return to the detector. It is not necessary for the amplifier itself to have full differential input capability with common mode rejection. See Fig. 3.2.3.

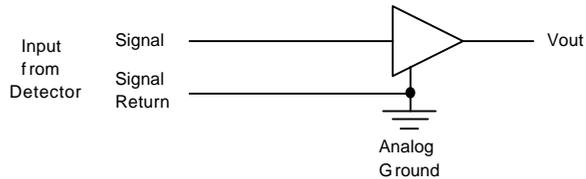


Figure 3.2.3. Single-Ended Amplifier with Signal Return

3.2.3.8 The front-end amplifier must have the capability to operate at two different gains, as indicated in Table 3.2.1. It is desirable to have the capability to select the gain of the amplifier by biasing external pins on the chip, defined as **GSEL, or Gain Select**. It is neither required nor desirable for gain selection to be programmable through the Control Communication Link (see Section 3.9.) The operational gains should be chosen by the chip designer to optimize the discriminator performance. GSEL shall default to logic 0 when open-circuited.

Detector	GSEL Logic	Smallest Signal	@Pulse Width	Avg. FS Signal	Source Capacitance
RPC (Avalanche)	0	50 fC	4 nS	15 pC	100 pF
GEM	1	5 fC	2 nS	100 fC	100 pF

Table 3.2.1. Detector Parameters for Gain Select

3. Specifications (Cont.)

3.2 Amplifier/Discriminator Section (Cont.)

- 3.2.3 The Amplifier Section has the following properties (cont.):
- 3.2.3.9 The amplifier must be capable of recovering back to baseline from the average full-scale signals shown in Table 3.2.1 within 1 mSec.
 - 3.2.3.10 The wide-band input impedance of the amplifier shall be 110 ohms +/- 5%, with of a phase angle approximately 0, over the frequency range of ~100 Hz through the closed-loop bandwidth of the amplifier. The impedance may have non-zero reactive components below 100 Hz, and above the closed-loop bandwidth of the amplifier.
 - 3.2.3.11 The intrinsic noise level of the amplifier must be less than 30% of the smallest signal level to be processed, as given in Table 1.
 - 3.2.3.12 The amplifier must be designed so that digital activity in the chip is not picked up or amplified, at the minimum operational threshold levels (see Section 3.2.4.)
 - 3.2.3.13 It is desirable for the amplifier to have a power supply rejection ratio in excess of -60 db up to the closed-loop -3 db bandwidth of the amplifier.
 - 3.2.3.14 It is desirable for neighboring channels on the chip to reject cross talk to better than 40 db.
 - 3.2.3.15 It is not desirable to use a sample-and-hold to sample the output voltage of the amplifier.
 - 3.2.3.16 Protection circuitry is required on the signal inputs to protect against instantaneous discharges from the detectors. (RPCs can have spontaneous discharges. As an upper estimate, assume that the 8KV detector bias charges ~10 pF of detector capacitance. The total energy of the discharge would be 320 micro-joules, but might be delivered in a few nanoseconds.)

3. Specifications (Cont.)

3.2 Amplifier/Discriminator Section (Cont.)

- 3.2.4 The Discriminator Section has the following properties:
- 3.2.4.1 Each channel shall have a discriminator, capable of responding to signals above a threshold voltage.
 - 3.2.4.2 The Threshold Voltage shall be generated from an on-board DAC called the Threshold DAC, and shall be common to all channels. See Section 3.11.
 - 3.2.4.3 The Discriminator shall be capable of discriminating on the smallest signals shown in Table 3.2.1 with 50% efficiency. It is not necessary for the Threshold Voltage range to be so large as to prevent the Discriminator from firing on the largest signals shown in Table 3.2.1. See Section 3.11 for a discussion of dynamic range and resolution of the Threshold DAC.
 - 3.2.4.4 The states of the discriminators shall be evaluated and stored on the rising edge of the Fundamental Clock Frequency.
 - 3.2.4.5 When an input signal meets the threshold requirements, it shall fire the discriminator on the clock cycle that follows. (This addresses the case where small, fast signals from the detector that have duration less than the period of the Fundamental Clock Frequency but otherwise meet the threshold requirements will fire the discriminator. This may be accomplished in different ways, including the adjustment of shaping times, or the use of edge-fired flip-flops on the output of the discriminator.)
 - 3.2.4.6 When an input signal meets the threshold requirements, it shall fire the discriminator once, and only once. (This addresses the case where shaping time constants are such that the amplifier recovery is slower than the Fundamental Clock Frequency.) A measurement of time-over-threshold is neither required nor desired.

3. Specifications (Cont.)

3.2 Amplifier/Discriminator Section (Cont.)

3.2.4 The Discriminator Section has the following properties (Cont.):

3.2.4.7 When an input signal meets the threshold requirements and occurs at or near the clock edge that would record the hit, it must be arranged so that the hit is not missed. If necessary, it is acceptable for the hit to be asserted in two adjacent clock cycles. It may be necessary to arrange the logic to use multi-phasing of the clock to accomplish recording and clearing functions.

3.2.4.8 The channel-to-channel matching of the input offset voltages of the discriminator shall be better than 2 equivalent DAC counts.

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3. Specifications (Cont.)

3.2 Amplifier/Discriminator Section (Cont.)

3.2.4 The Discriminator Section has the following properties (Cont.):

3.2.4.9 Comparators can oscillate under certain biasing conditions of the inputs. It is acceptable for such conditions to exist in the Discriminator, provided the oscillations occur only if the following conditions are met:

3.2.4.9.1 The oscillations can occur **ONLY** in a limited range of Threshold DAC values. Define the range of DAC values under which the Discriminator oscillates as the ***Oscillation Band***.

3.2.4.9.2 The Oscillation Band must occur only near the very low end of the DAC range. Further, it must be such that the nominal DAC voltage needed to discriminate on the smallest signals (as specified in Section 3.2.4.3) is at least three times the width of the Oscillation Band **AWAY** from the Oscillation Band. The headroom between the upper edge of the Oscillation Band and the threshold setting to discriminate on the smallest signals is defined as the ***Headroom Band***.

3.2.4.9.3 The Oscillation Band must be stable and reproducible to within +/- 1 DAC count.

3.2.4.9.4 The channel-to-channel matching of the Oscillation Band edges must be less than 30% of the width of the Oscillation Band, or 10% of the Headroom Band, whichever is greater.

3. Specifications (Cont.)

3.2 Amplifier/Discriminator Section (Cont.)

3.2.5 The Pre-Attenuator Section has the following properties:

3.2.5.1 The Pre-Attenuator Section is required for the case where the detector is operated in a saturated (streamer) mode, producing large pulses. The Pre-Attenuator must attenuate the signal by a factor of 10 before passing it on to the Amplifier Section. See Table 3.2.2.

Detector	Smallest Signal	@Pulse Width	Largest Signal	Source Capacitance
RPC Streamer	500 fC	50 nS	10 pC	(Trans. Line) Zo = 110 ohms

Table 3.2.2. Detector Parameters for Pre-Attenuator

3.2.5.2 The Pre-Attenuator Section shall be configured so that it can be switched into the signal path by setting a bias level on external pins of the chip, defined as **PREATTN**. It is neither required nor desirable for Pre-Attenuator selection to be programmable through the Control Communication Link (see Section 3.9.) Asserting PREATTN to logic 1 shall switch the Pre-Attenuator circuit into the signal path, while logic 0 switches it out. PREATTN shall default to logic 0 when open-circuited.

3.2.5.3 The Pre-Attenuator shall have a differential input, where it is assumed that the signal path from the detector and signal return path to the detector are balanced.

3.2.5.4 The Pre-Attenuator shall provide common-mode rejection of 40 db (minimum) up through the bandwidth of the Amplifier.

3.2.5.5 The input impedance of the Pre-Attenuator shall be purely resistive, with a value of 110 ohms, +/- 5%.

3.2.5.6 The output impedance of the Pre-Attenuator must be compatible with the Amplifier so that the attenuated signals are discriminated reliably and efficiently.

3. Specifications (Cont.)

3.3 Internal Trigger Decision Formation

3.3.1 The output states of the discriminators shall be used as inputs to a logic block to form a signal called the **Internal Trigger Decision, or TINT**. This signal shall be used both internally and external to the chip as described below, as part of the trigger decision process. See Fig. 3.3.1. Note that the method by which the chip is actually forced to record an event for read-out is described in Section 3.6.

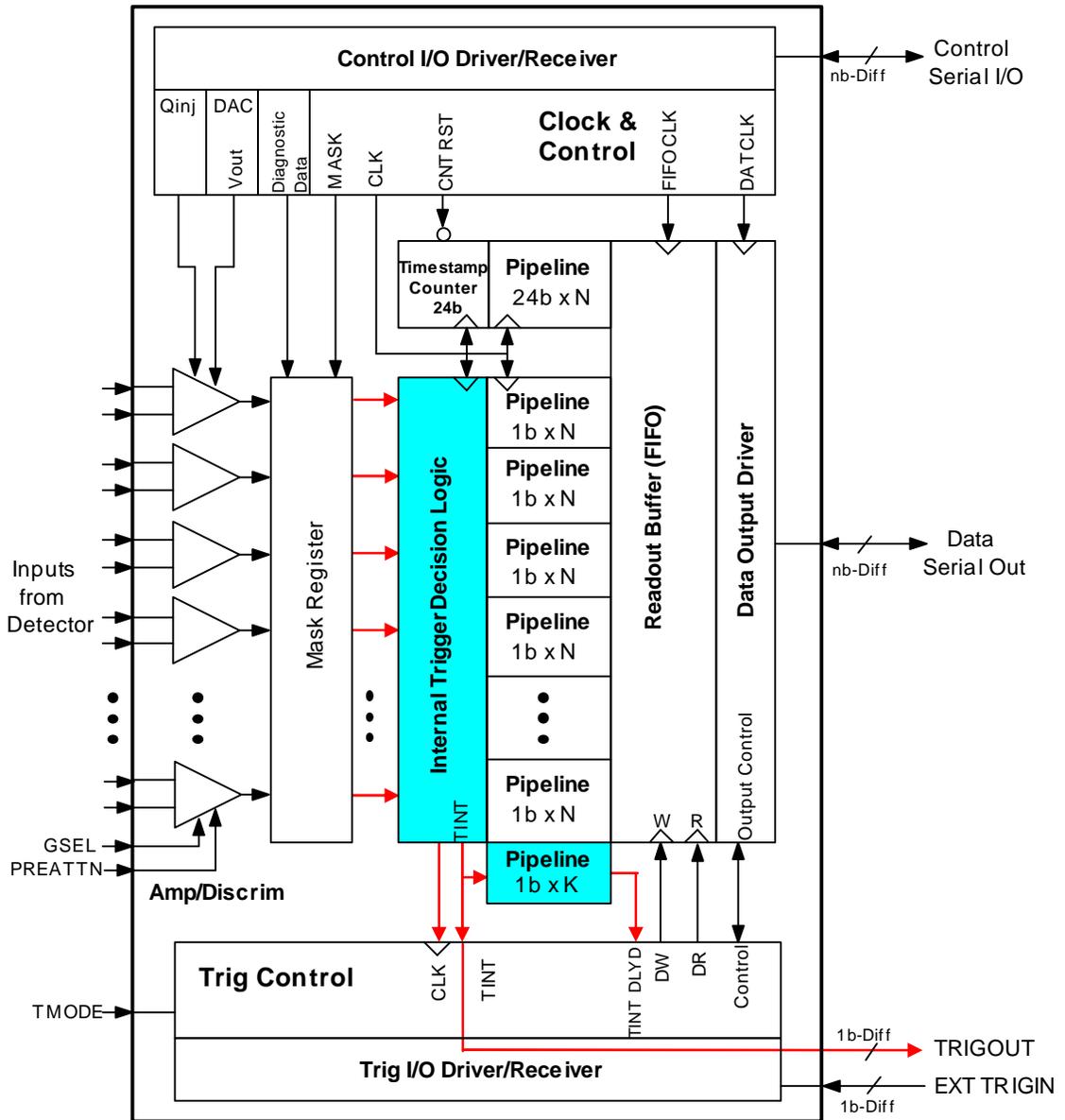


Figure 3.3.1. Formation of the Internal Trigger Decision

3. Specifications (Cont.)

3.3 Internal Trigger Decision Formation (Cont.)

- 3.3.2 The signal TINT is formed from the comparator states. TINT is asserted to the logic 1 state when one or more discriminators fire in a given clock cycle.
- 3.3.3 The signal TINT shall be formed on the rising edge of the clock. The states of the discriminators are evaluated at that time (see Section 3.2), and the state of the TINT is determined accordingly.
- 3.3.4 A new trigger decision TINT shall be made on each clock cycle. The circuitry must be capable of operation well in excess of the Fundamental Clock Frequency, specified in Section 3.1.
- 3.3.5 It is acceptable for the processing time in the formation of the signal TINT to cause one or more clock cycles of delay. This delay may be in series or in parallel with the pipeline delay, as specified in Section 3.4, at the chip designer's discretion.
- 3.3.6 The signal TINT shall be used to create an output signal from the chip, called **Trigger Out, or TRIGOUT**. When TINT is asserted as described above, TRIGOUT shall have duration equal to half of a clock period. (The rising edge of TRIGOUT shall be used on the receiving end to process triggers.)
- 3.3.7 The chip shall be capable of driving the output signal TRIGOUT out of the chip. It is desirable to use a differential, balanced, current-drive technique. It is desirable that the output driver be capable of driving a terminated transmission line. The impedance of the transmission line is left to the chip designer's discretion. The driver must adhere to a standard, chosen at the chip designer's discretion, and interface on the receiving end to a commercially available chip set. Note that the maximum TRIGOUT rate is equal to the Fundamental Clock Frequency.

3. Specifications (Cont.)

3.4 Pipeline Section

3.4.1 The chip shall have a pipeline for storing the discriminator states and the Timestamp Counter bits. This is used to provide time delay for the case where the chip read out is triggered from an external trigger. (See Section 3.5 for a description of the Timestamp Counter.)

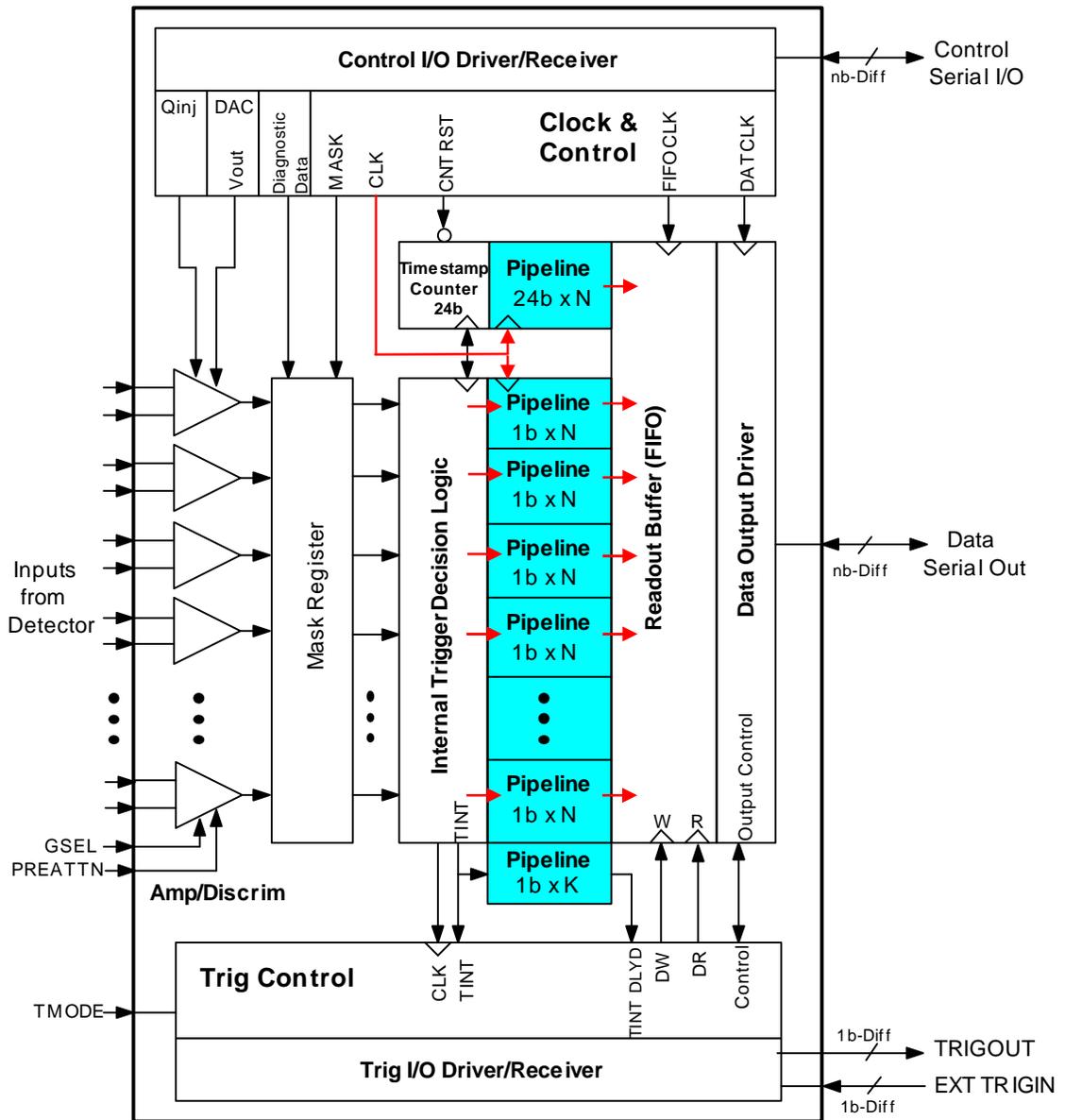


Figure 3.4.1. Configuration of the Pipeline Section

3. Specifications (Cont.)

3.4 Pipeline Section (Cont.)

- 3.4.2 Data written to the first stage of the pipeline shall be advanced to the next stages synchronously with the clock, using shift register techniques.
- 3.4.3 Data shall be advanced to subsequent pipeline sections on the rising edge of the clock.
- 3.4.4 When data is advanced to the end of the pipeline, it shall either be advanced to the next section of circuitry (the Readout Buffer), or not, depending on the result of a trigger decision on that data. See Section 3.7.
- 3.4.5 The pipeline section shall be configured so that there are 20 clock cycles of delay.
- 3.4.6 The pipeline section must be capable of operation well in excess of the Fundamental Clock Frequency (see Section 3.1.)

3. Specifications (Cont.)

3.5 Timestamp Section

3.5.1 The chip shall have a 24-bit counter called the **Timestamp Counter**, which counts clock cycles from a reference time. This will be used to correlate triggered events in time across the entire read-out system.

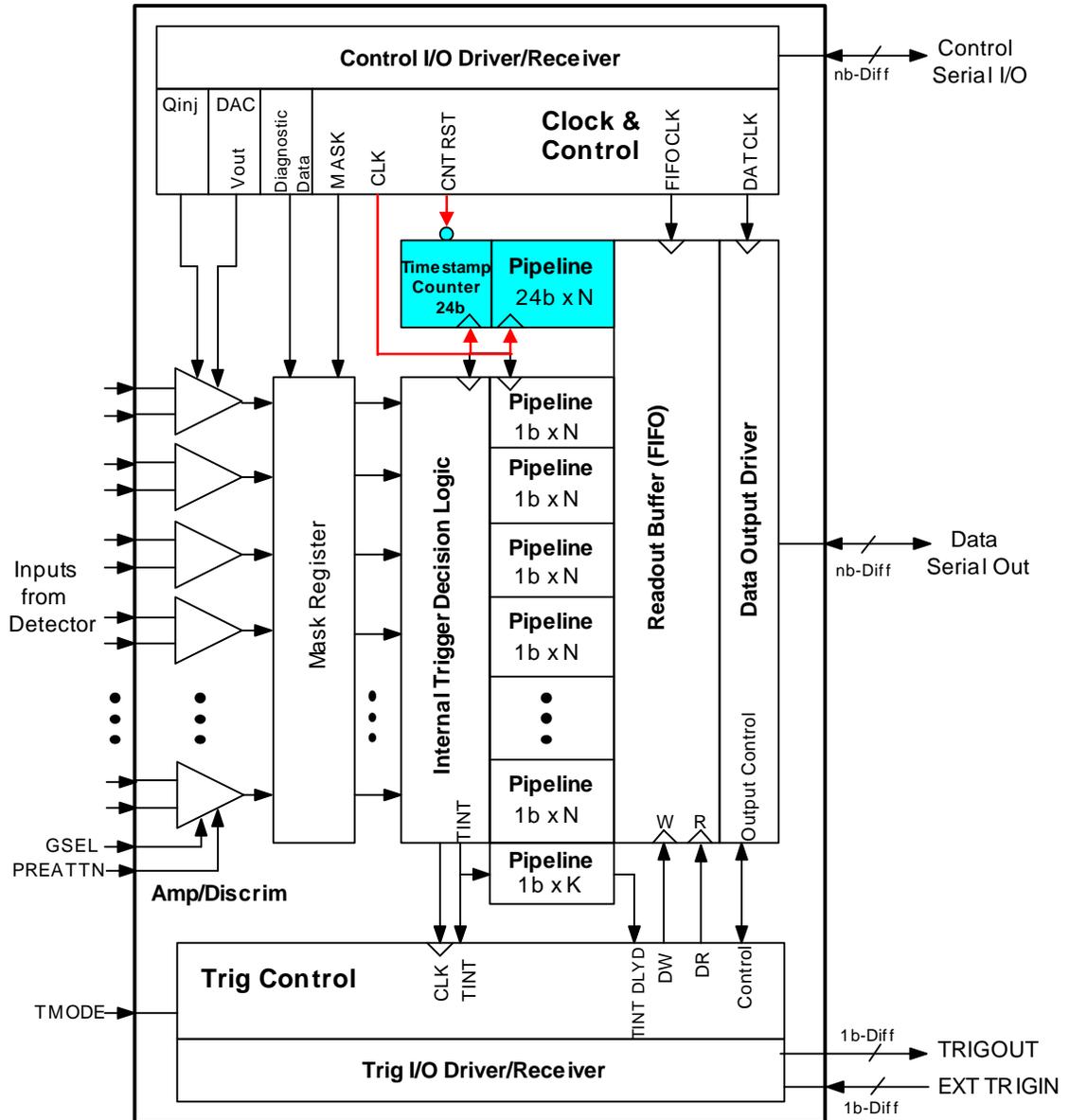


Figure 3.5.1. Timestamp Circuitry

3. Specifications (Cont.)

3.5 Timestamp Section (Cont.)

- 3.5.2 The Timestamp Counter shall be configured to advance on the rising edge of the clock (up-counter.) The ability to count down is neither required nor desired.
- 3.5.3 The Timestamp Counter must be capable of operation well in excess of the Fundamental Clock Frequency (see Section 3.1.)
- 3.5.4 The Timestamp Counter shall have a reset called **Counter Reset, or CNTRST**, provided from outside the chip. The reset signal shall be arranged as a synchronous clear with respect to the rising edge of the clock. The counter reset shall be provided as one of the functions of the control circuitry (see Section 3.9.)
- 3.5.5 The Timestamp Counter shall be configured to overflow gracefully, advancing from a full-scale count to 0 without glitch or error.
- 3.5.6 The output bits of the Timestamp Counter shall be written into the Readout Buffer when a Trigger Accept occurs (see Section 3.7), becoming part of the event data.
- 3.5.7 It is *desirable* to have the output of the counter delayed with a pipeline at the same depth as that for the data. (Thus, an event that fires a discriminator at the same time as the counter reset occurs would be marked as having a timestamp of 0.) (This feature may have consequences for power consumption and area on the chip, and is open for discussion with.)
- 3.5.8 For noise considerations, it is desirable (but not required) to have the Timestamp Counter operate with grey-coding, such that one and only one bit changes on each clock cycle. (Note that this is different from having a conventional counter and simply grey-coding the output bits.) This is left to the chip designer's discretion, as part of meeting noise performance.

3. Specifications (Cont.)

3.6 Triggering Data for Readout - Trigger Control

3.6.1 The discriminator states and the timestamp bits are clocked continuously through the pipeline section. An explicit state, the **Trigger Accept**, is to be asserted in order to capture data from a particular period in time, to make the data available to be read out of the chip.

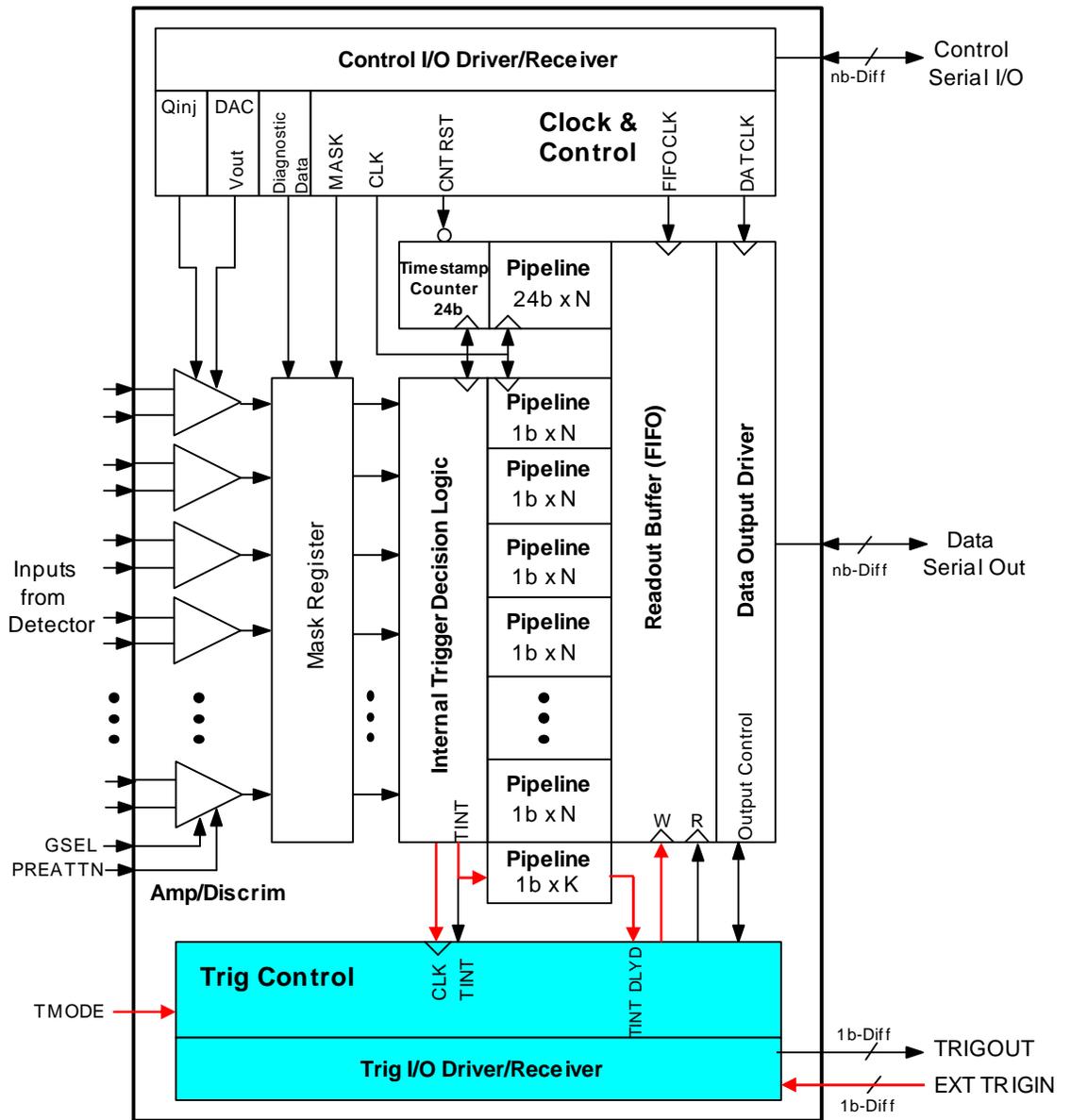


Figure 3.6.1. Triggering Data for Read Out

3. Specifications (Cont.)

3.6 Triggering Data for Readout - Trigger Control (Cont.)

- 3.6.2 The Trigger Accept state may be asserted through one of two modes of operation: Self-Trigger Mode, and External Trigger Mode.
- 3.6.2.1 In Self-Trigger Mode, the chip shall use the internally trigger decision signal TINT (see Section 3.3.) In this case, the assertion of TINT shall cause data to be written from the output of the Pipeline Section into the Readout Buffer (see Section 3.7.) The timing must be arranged so that this action is delayed appropriately, to capture the event of interest as it emerges from the output of the pipeline.
- 3.6.2.2 In External Trigger Mode, data from the output of the Pipeline Section shall be written into the Readout Buffer when an External Trigger Signal is received by the chip.
- 3.6.3 In both modes, data from the pipeline shall be written to the Readout Buffer synchronously with the clock, synchronized with the rising edge of the clock.
- 3.6.4 The formation of the Trigger Mode State is achieved through an external pin of the chip called the **Trigger Mode signal, or TMODE**. **Self-Trigger Mode** is formed when TMODE is asserted to logic 0 externally. **External Trigger Mode** is formed when TMODE is asserted to logic 1 externally. The chip shall be configured such that an open external connection defaults to the Self-Trigger Mode.
- 3.6.5 Data is acquired from the output of the Pipeline (see Section 3.4) and stored in the Readout Buffer (see Section 3.7) through the assertion of a signal **called Data Write, or DW**. This must be a prompt signal arising from the Trigger Accept state, arranged to capture the event of interest associated with a particular trigger.

3.7 Readout Buffer

3.7.1 **Event data** is defined as the state of all discriminators and the value of the Timestamp Counter at the end of a given clock cycle.

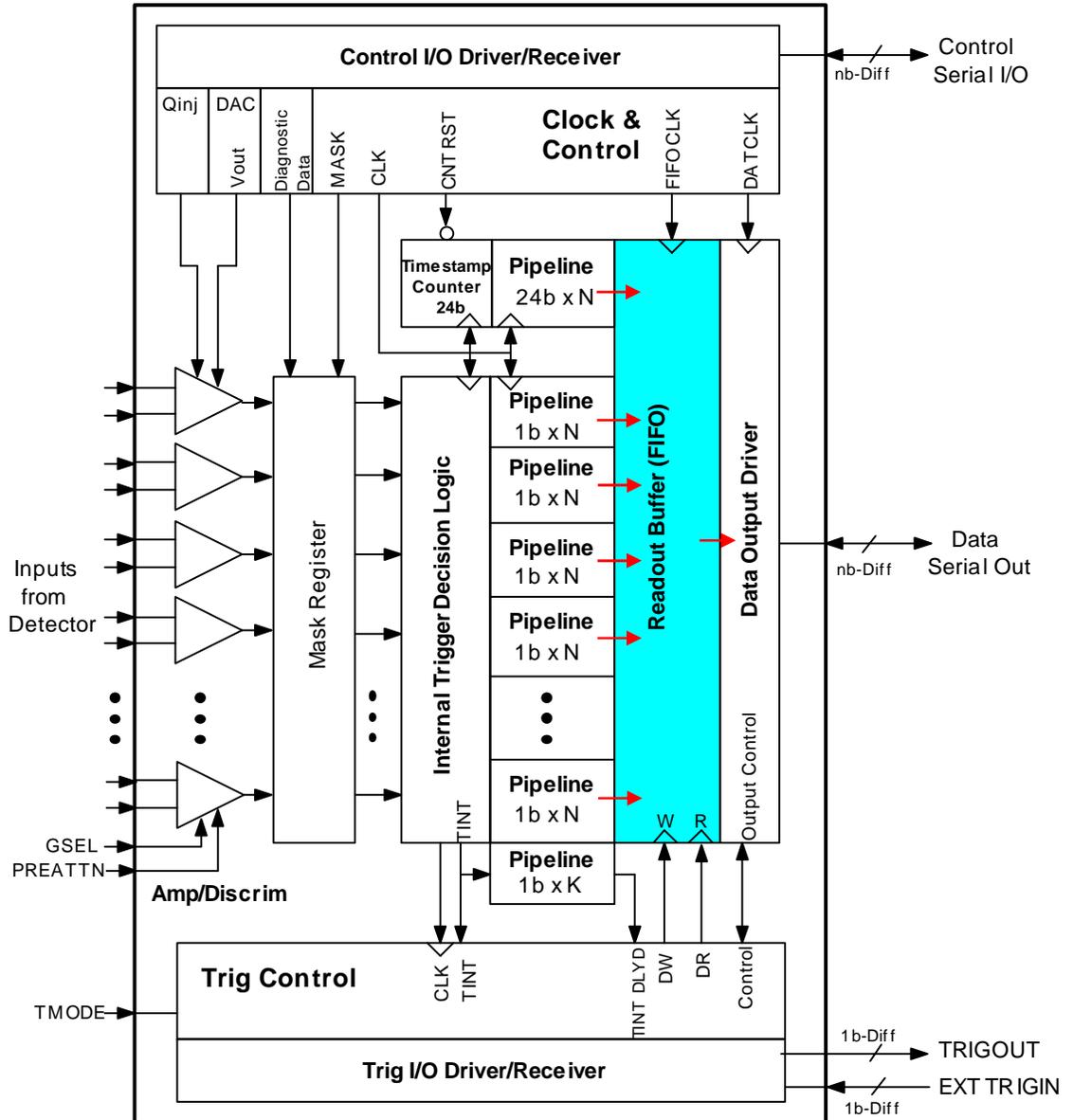


Figure 3.7.1. Readout Buffer Circuitry

3. Specifications (Cont.)

3.7 Readout Buffer (Cont.)

- 3.7.2 Event data shall be written into the Readout Buffer in response to the formation of a Trigger Accept state (see Section 3.6.)
- 3.7.3 The Readout Buffer shall be capable of storing 16 events. The transmission of events out of the chip shall occur as a “first in, first out” (FIFO) process.
- 3.7.4 If the Readout Buffer is nearly full and contains only one free location to store a new event, this is defined as the **Nearly Full State, or NF State**. If this state is reached and another Trigger Accept occurs, the chip must generate a message, to be passed along either with the data or as a special data word, that the FIFO has become full. (The details and format are yet to be defined.)
- 3.7.5 Once event data is written into the Readout Buffer, the transmission of data out of the chip shall be automatic, i.e. not dependent on external processes, communication, or intervention. See Section 3.8.

3. Specifications (Cont.)

3.8 Data Output Driver

3.8.1 When one or more events are stored in the Readout Buffer, the chip shall execute operations to transfer event data to the Output Driver for transmission out of the chip, one event at a time.

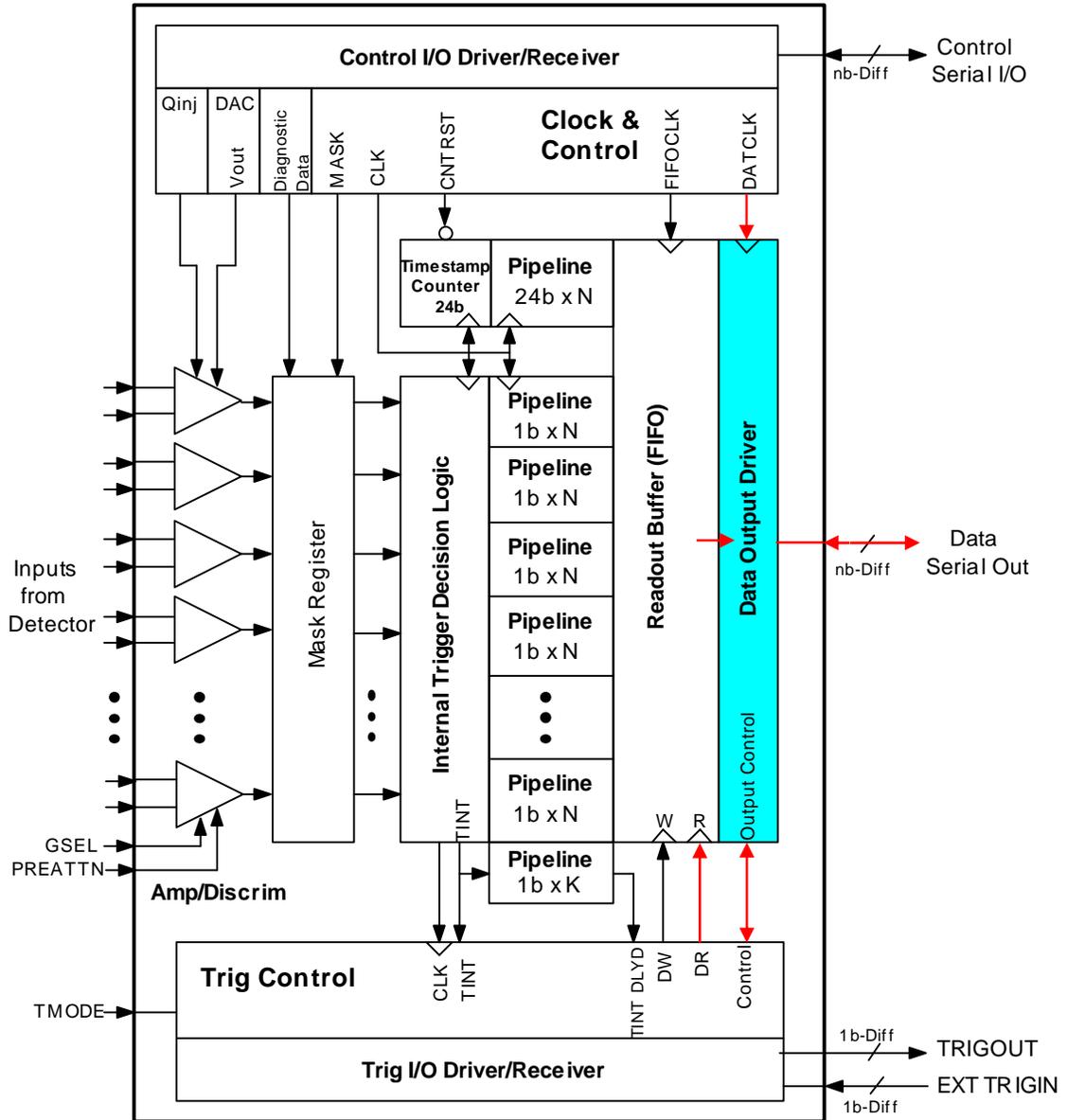


Figure 3.8.1. Output Driver Circuitry

3. Specifications (Cont.)

3.8 Data Output Driver (Cont.)

- 3.8.2 On-board control circuitry shall monitor the state of the FIFO in the Readout Buffer. If there is an event pending in the Readout Buffer, this control circuitry shall arrange to transfer data to the Output Driver when the Output Driver circuitry is in an idle state.
- 3.8.3 The data stored in the Readout Buffer is written to the Output Driver through the assertion of a signal called Data Read, or DR. Once data is transferred, it shall be cleared from the Readout Buffer, making memory space in the Readout Buffer available for a new event.
- 3.8.4 Data shall be transmitted out of the chip using a serial transmission format. This shall be a dedicated link, defined as the **Data Output Link**, and shall be independent and separate from chip control I/O (see Section 3.9.)
- 3.8.5 The chip must transfer an event out of the chip within 10 microseconds, to meet event rate requirements. This assumes that the receiver is capable of receiving data without any limitations from flow control.
- 3.8.6 The format of the serial transmission scheme (number of start bits, stop bits, frame length, parity, error detection/correction, NRZ, etc.) is left to the chip designer's discretion. The encoding scheme must be a standard, so that a commercial chip can be used as the receiver.
- 3.8.7 The data shall be self-clocking at the receiver, consistent with standard serial-transmission techniques.
- 3.8.8 The timing for the serial transmission shall be derived from the clock provided to the chip. The frequency used for the serial transmission shall be the same as the Fundamental Clock Frequency, although the framing of data bits may send and receive an integer number of bits in one clock cycle.
- 3.8.9 The use of flow control or a handshake between the driver and receiver is desirable. However, in general, the readout of data from the chip shall use the concept of "data push," where data is not requested by the receiver but instead pushed out of the chip as it is acquired.

3. Specifications (Cont.)

3.8 Data Output Driver (Cont.)

- 3.8.10 The format of the data shall have a header that can uniquely be detected at the receiver, and identified as the beginning of the transmission of a new event.
- 3.8.11 The use of a trailer is not required, since the format of the data always has the same number of bits.
- 3.8.12 The hardware implementation of the serial transmission may use one or more pairs of lines. It is desirable to keep the number of signal pairs to a minimum. It is desirable to use a differential, balanced, current-drive technique. It is desirable that the output driver be capable of driving a terminated transmission line. The impedance of the transmission line is left to the chip designer's discretion. The driver must adhere to a standard, chosen at the chip designer's discretion, and interface on the receiving end to a commercially available chip set

3. Specifications (Cont.)

3.9 Control Section

3.9.1 Control of the chip shall be realized using a serial communication protocol. This shall be a dedicated link, defined as the **Control Communication Link**, and be independent of and separate from the Data Output Link (see Section 3.8.)

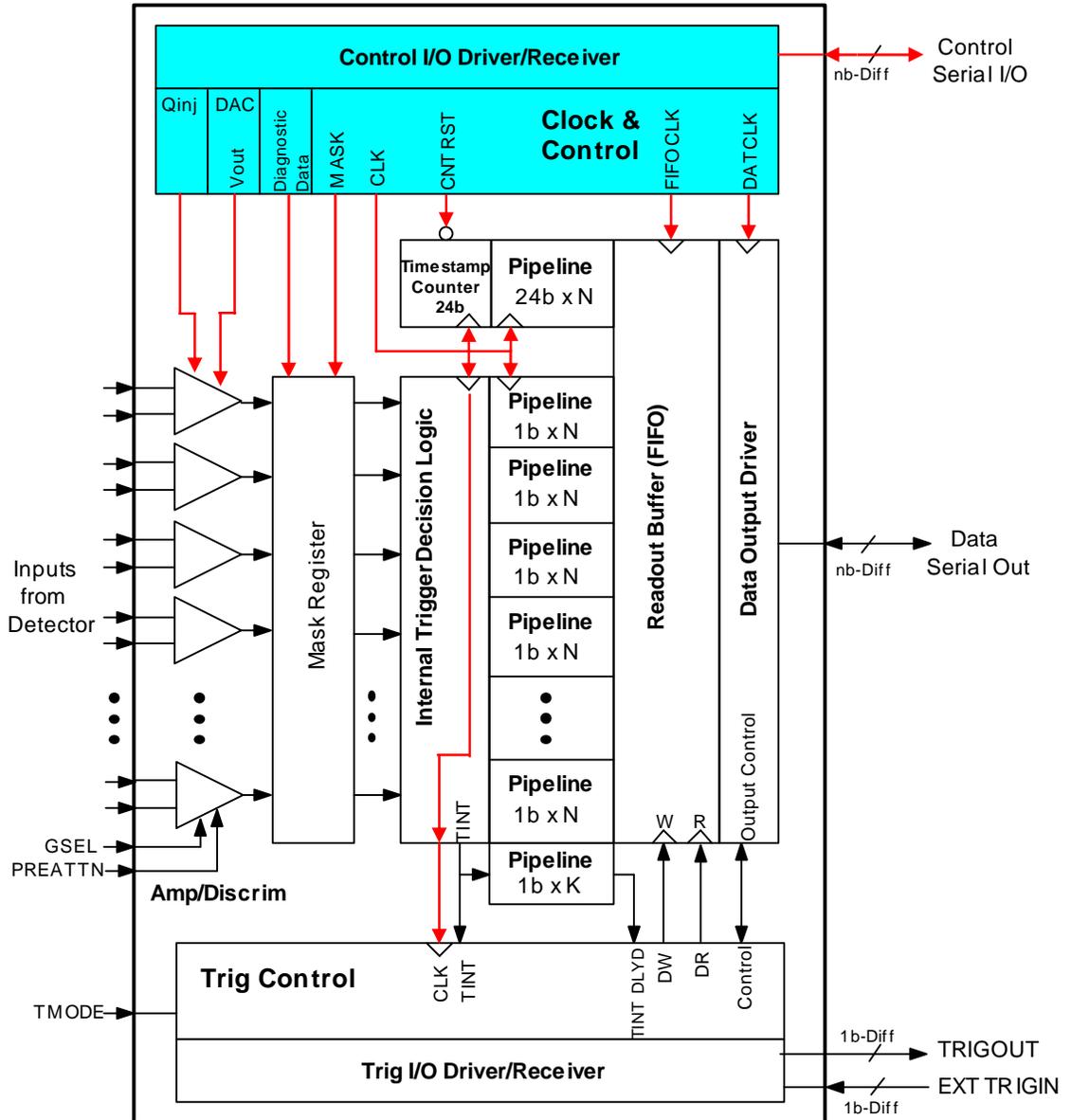


Figure 3.9.1. Output Driver Circuitry

3. Specifications (Cont.)

3.9 Control Section (Cont.)

- 3.9.2 The functionality of the Control Communication Link is divided into three parts:
 - 3.9.2.1 The Control Communication Link shall provide the clock for the chip.
 - 3.9.2.2 Certain time-critical functions must be executed promptly, or with determinate delays, on any arbitrary clock cycle. These functions are to be synchronized across many parts of the system.
 - 3.9.2.3 Certain functions of the Control Communication Link are not time-critical, and are related to writing or reading static control words to or from registers on the chip.
- 3.9.3 The clock for the chip has certain timing specifications. See Section 3.10 for these specifications.
- 3.9.4 The time-critical functions are as follows:
 - 3.9.4.1 Counter Reset for the Timestamp Counter shall be provided on the Control Communication Link. This needs to be a precision signal, capable of being synchronized across the entire system on a given clock cycle. The communication protocol must provide the capability to send a Counter Reset on any given clock cycle. The protocol may have one or more clock cycles of delay from the time that the Counter Reset command is received to when it is actually asserted at the Timestamp Counter. However, any such delay must be a constant, and uniform from chip to chip.

3. Specifications (Cont.)

3.9 Control Section (Cont.)

- 3.9.4 The time-critical functions are as follows (cont.):
- 3.9.4.2 It is desirable to implement a global Charge Injection Command (see section 3.12.) If implemented, it would need to be a precision signal, and would need to be synchronized across the entire system. The communication protocol would need to provide the capability to send a charge Inject Command on any given clock cycle. The protocol may have one or more clock cycles of delay from the time that the Charge Inject Command is received to when charge injection actually occurs. However, any such delay must be a constant, and uniform from chip to chip.
- 3.9.5 Control of the chip shall be realized with the use of registers, which are accessed via the Control Communication Link:
- 3.9.5.1 There shall be a **Threshold Register**, which shall control an on-board DAC for setting the threshold voltage for the discriminators. See Section 3.11.
 - 3.9.5.2 A **Mask Register** is needed, which is capable of turning off input channel discriminators at the front end. N bits are required, one for each discriminator channel.
 - 3.9.5.3 It is desirable to have a **QINJ Register**, which shall control the operation of an on-board charge injection circuit. See Section 3.12.
 - 3.9.5.4 It is desirable, but not required, to have a **Diagnostic Data Register**, capable of sending diagnostic data out of the chip through the data output driver. If implemented, the configuration should include a way to trigger such an event.
- 3.9.6 The Control Communication Link shall be bi-directional, providing both read and write capability to all registers implemented. The chip should be regarded as a slave with respect to the Control Communication Link, where control of the read/write states is assumed to reside outside the chip.

3. Specifications (Cont.)

3.9 Control Section (Cont.)

- 3.9.7 The format of the serial transmission scheme (number of start bits, stop bits, frame length, parity, error detection/correction, NRZ, etc.) is left to the chip designer's discretion. The encoding scheme must be a standard, so that a commercial chip can be used as the receiver.
- 3.9.8 The data shall be self-clocking at the receiver, consistent with standard serial-transmission techniques.
- 3.9.9 The timing for the serial transmission shall be derived from the clock provided to the chip. The frequency used for the serial transmission shall be the same as the Fundamental Clock Frequency, although the framing of data bits may send and receive an integer number of bits in one clock cycle.
- 3.9.10 The use of flow control or a handshake between the driver and receiver is desirable.
- 3.9.11 The format of the data shall include both address and data. The format should have a header that can uniquely be detected at the receiver, and identified as the beginning of the transmission of new data.
- 3.9.12 The use of a trailer is not required, if the format of the data always has the same number of bits.
- 3.9.13 The hardware implementation of the serial transmission may use one or more pairs of lines. It is desirable to keep the number of signal pairs to a minimum. It is desirable to use a differential, balanced, current-drive technique. It is desirable that the output driver be capable of driving a terminated transmission line. The impedance of the transmission line is left to the chip designer's discretion. The transceiver must adhere to a standard, chosen at the chip designer's discretion, and interface on the receiving end to a commercially available chip set

3. Specifications (Cont.)

3.10 Clock Specifications

- 3.10.1 The clock used by the internal circuitry of the chip shall be derived from the serial communication interface received through the Control Communication Link. See Section 3.1 for the specification of the Fundamental Clock Frequency.
- 3.10.2 The clock used by the internal circuitry of the chip shall have a 50% duty cycle.
- 3.10.3 The digital functions of the chip operate synchronously, with state changes occurring on the rising edge of the internal clock.
- 3.10.4 The rise and fall times of the internal clock shall be less than 5% of the Fundamental Clock Frequency.
- 3.10.5 The jitter of the internal clock shall be less than 2% of the Fundamental Clock Frequency.
- 3.10.6 The temperature stability of the phase of the internal clock shall not be worse than 0.2 nSec/Degree C.
- 3.10.7 Chip-to-chip variations of the phase of the internal clock, assuming identical clock source circuitry and transmission lengths, shall be better than 5% of the Fundamental Clock Frequency.
- 3.10.8 It may be desirable to implement a Phase-Lock Loop (PLL) in the chip, in order to meet clock performance specifications. This is left to chip designer's discretion.

3. Specifications (Cont.)

3.11 Threshold DAC

- 3.11.1 The least count resolution of the Threshold DAC must correspond to approximately half of the smallest signal size shown in Table 3.2.1, reflected in the equivalent output voltage of the DAC.
- 3.11.2 The low end of the Threshold DAC must meet the Headroom Band requirements discussed in Section 3.2.4.
- 3.11.3 It is desirable for the range of the Threshold DAC to be capable of discriminating on signals approximately 50 times larger than the smallest signal size shown in Table 3.2.1, reflected in the equivalent output voltage of the DAC.
- 3.11.4 For this application, the requirements for differential and integral nonlinearity of the DAC output voltage as a function of digital code are not critical. The DAC voltage should be monotonic, over the range, with no missing codes.
- 3.11.5 The requirements of 3.11.1 through 3.11.3 imply approximately 7 bits of dynamic range. It is acceptable for the dynamic range to be achieved with fewer bits, using a nonlinear scale. (This is open for discussion.)
- 3.11.6 The voltage levels of the DAC are left to the chip designer's discretion, to meet the other performance specifications.
- 3.11.7 It is neither necessary nor desired to change the Threshold DAC range or resolution as a function of the Gain Select state or the Pre-Attenuator activation state (see Section 3.2.) It is desirable to have the range and resolution of the Threshold DAC be a constant, and that signal conditioning be done upstream of the Discriminator.
- 3.11.8 It is desirable for the DAC to have an on-board reference. If implemented, the noise and stability of the reference, and the DAC itself, must be such that DAC voltage stability and noise are less than one DAC count in equivalent voltage. The alternative is to provide the reference voltage to the chip from an external source using an I/O pin.
- 3.11.9 It is requested that both the DAC voltage and the reference voltage be brought out of the chip as test points.

3. Specifications (Cont.)

3.12 Charge Injection

- 3.12.1 It is desirable for the chip to have the capability to inject charge into the front-end amplifier. It is not necessary to have the capability to inject charge into the Pre-Attenuator.
- 3.12.2 At a minimum, capability should exist to inject charge at one known, stable value. If implemented this way, a value should be chosen to function above minimum threshold settings (see discussion of the Oscillation Band in Section 3.2), and function for both Gain Select states (see Section 3.2.) It is desirable to have two set values of the charge injected, corresponding to the two different Gain Select states.
- 3.12.3 It is desirable, but not required, to have the capability to inject charge over a range of value. This would facilitate the mapping and calibration of the discriminator as a function of the threshold voltage. This might be implemented using a DAC to set a voltage on a capacitive discharge circuit. If implemented, the DAC should have a range appropriate for both Gain Select states (see Section 3.2.)
- 3.12.4 A means should be provided to fire the charge injection circuit. It is desirable for this to be provided as a timing signal, defined as the **Charge Inject Command**, to facilitate the firing of two or more chips simultaneously across the system. (This is desirable to test the timing of Timestamp Counter.) If implemented this way, the Charge Inject Command should be incorporated through the Control Communication Link, and be treated in a similar way as Counter Reset (see Section 3.9.)

3. Specifications (Cont.)

3.13 Power and Packaging

- 3.13.1 The power supply levels are left to the chip designer's discretion. It is desirable for the chip to use a minimum number of external supplies. It is desirable for the voltage levels to be +5V, common, and -5V. Non-standard voltage levels are discouraged. Voltage regulation and ripple requirements are to be specified by the chip designer. It is desirable for the chip to have a large range of insensitivity to power supply variation, so that local, external regulation is not required.
- 3.13.2 It is desirable for the power dissipation of the chip to be 2-3 mW per channel, averaged over the entire chip, when operated at the Fundamental Clock Frequency. Power dissipation should not exceed 5 mW per channel, averaged over the entire chip.
- 3.13.3 The device should be packaged such that it can be assembled onto a printed circuit board using "conventional" techniques, such as SMT assembly or BGA technology.
- 3.13.4 The height of the packaged chip from the assembly surface must not exceed 1 mm.

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