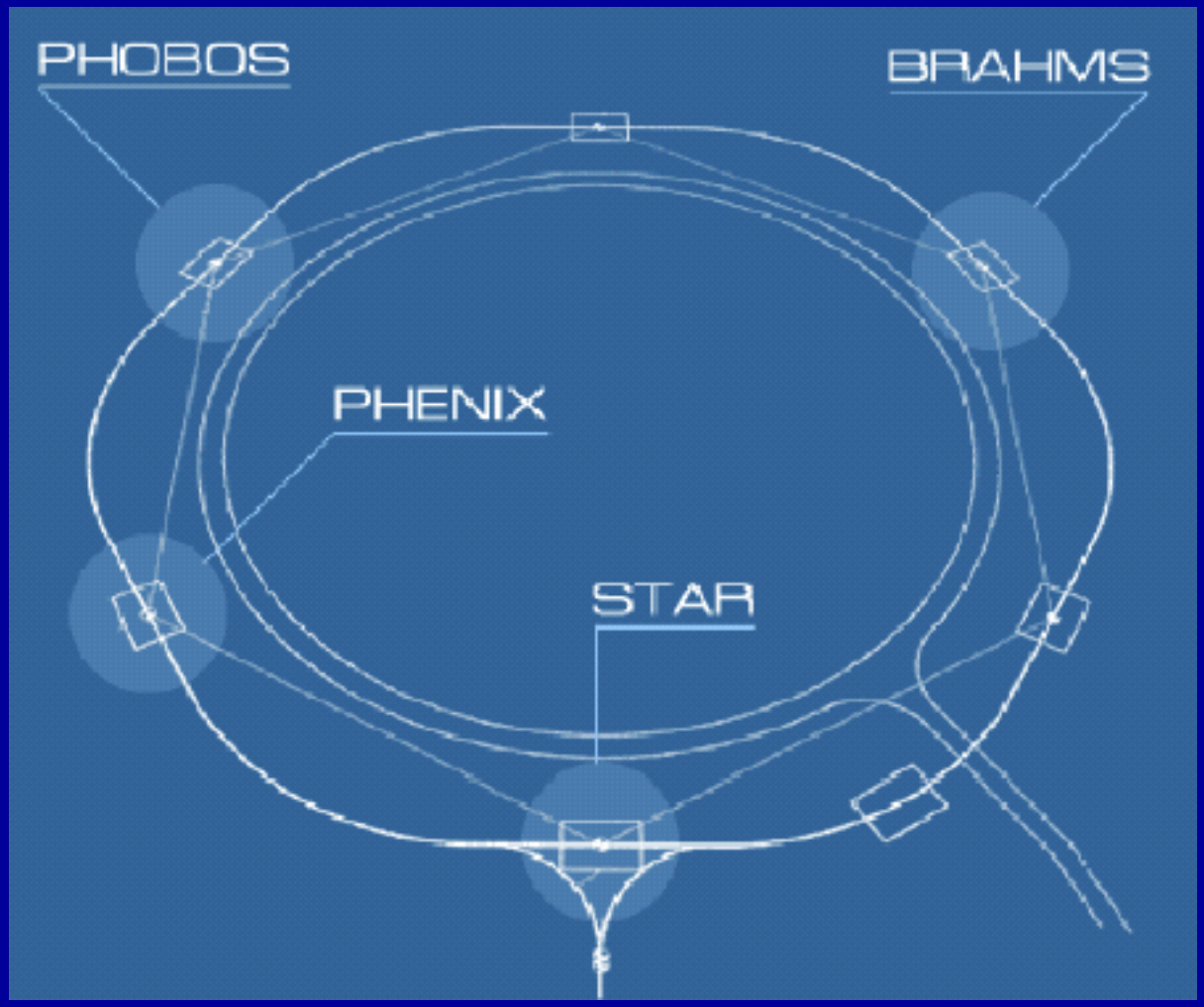
# APV25 READOUT ARCHITECTURE

Feb 2005



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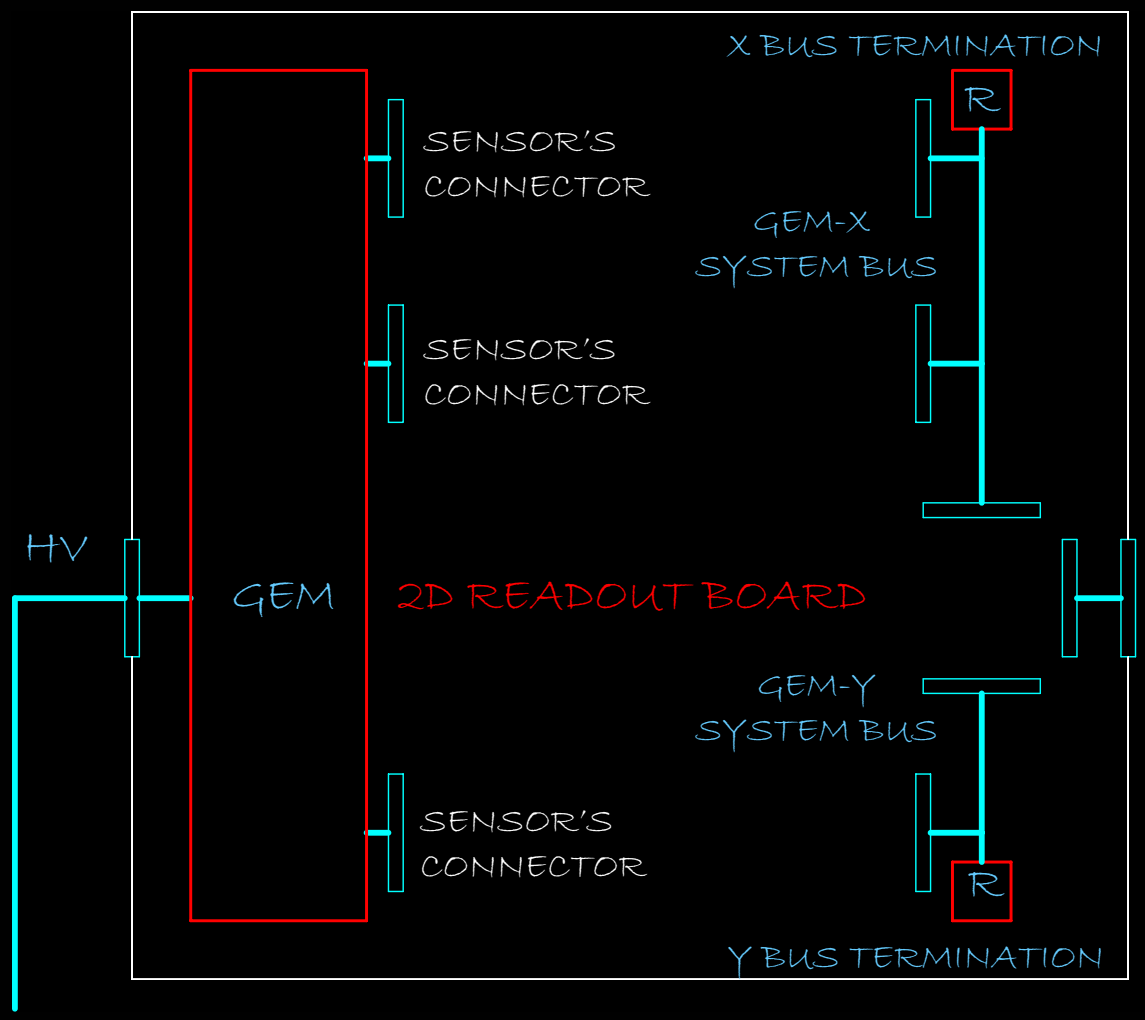


2D READOUT BOARD:
- ACTIVE AREA 4"x 4"
- 2MIL (1MIL) KAPTON COATED WITH 9MICRON COPPER FROM BOTH SIDES
- CORE 62MIL FR4
- X AND Y STRIP'S PITCH 25MIL
- X STRPS WIDTH 5MIL (9MIL)
- Y STRIPS WIDTH 20MIL
- PLATING WITH EMMERSION GOLD OVER NICKEL

CONNECTOR FOR LVDS I/O COMMUNICATION

TRIPLE GEM DIMENSIONS FROM HV DOWN TO SENSORS:
- 3.175 mm
- 2.38 mm
- 2.38 mm
- 2.38 mm

2D READOUT BOARD FORM BASE FOR READOUT ELECTRONICS

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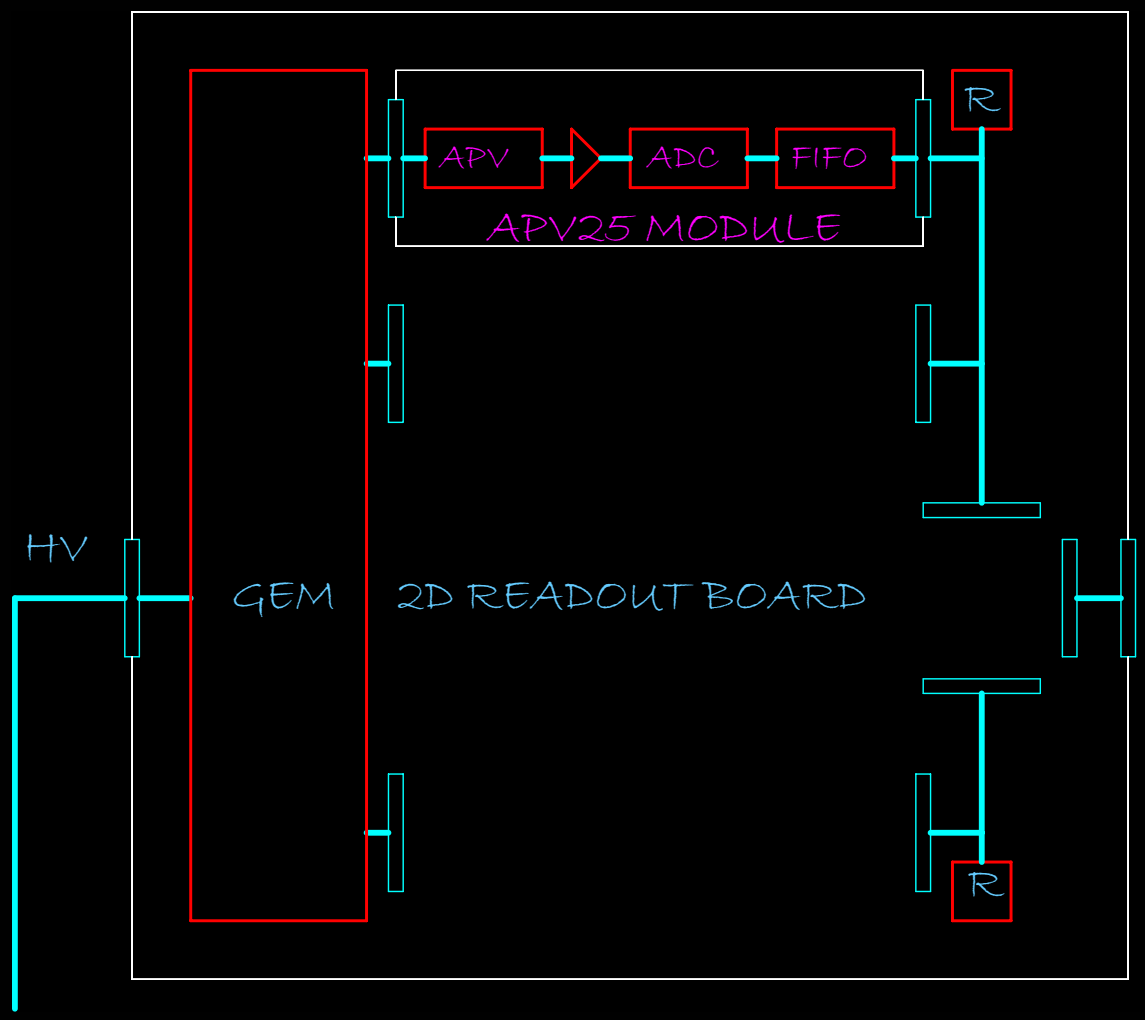


APV25 MODULE IS BASIC MODULAR ELEMENT FOR 2D GEM READOUT ELECTRONICS.

APV25 MODULE IS CONNECTED TO SENSOR'S AND SYSTEM BUS CONNECTORS.

ARCHITECTURE OF APV25 MODULE IS CREADED FROM:

- APV25-S1 CHIP
- LTC2248 FAMILY HIGH SPEED ADC
- ST74215-10 18 BITS/100MHz FIFO

APV25 MODOLES ARE CONNECTED VIA CONNECTORS INTO 2D BOARD

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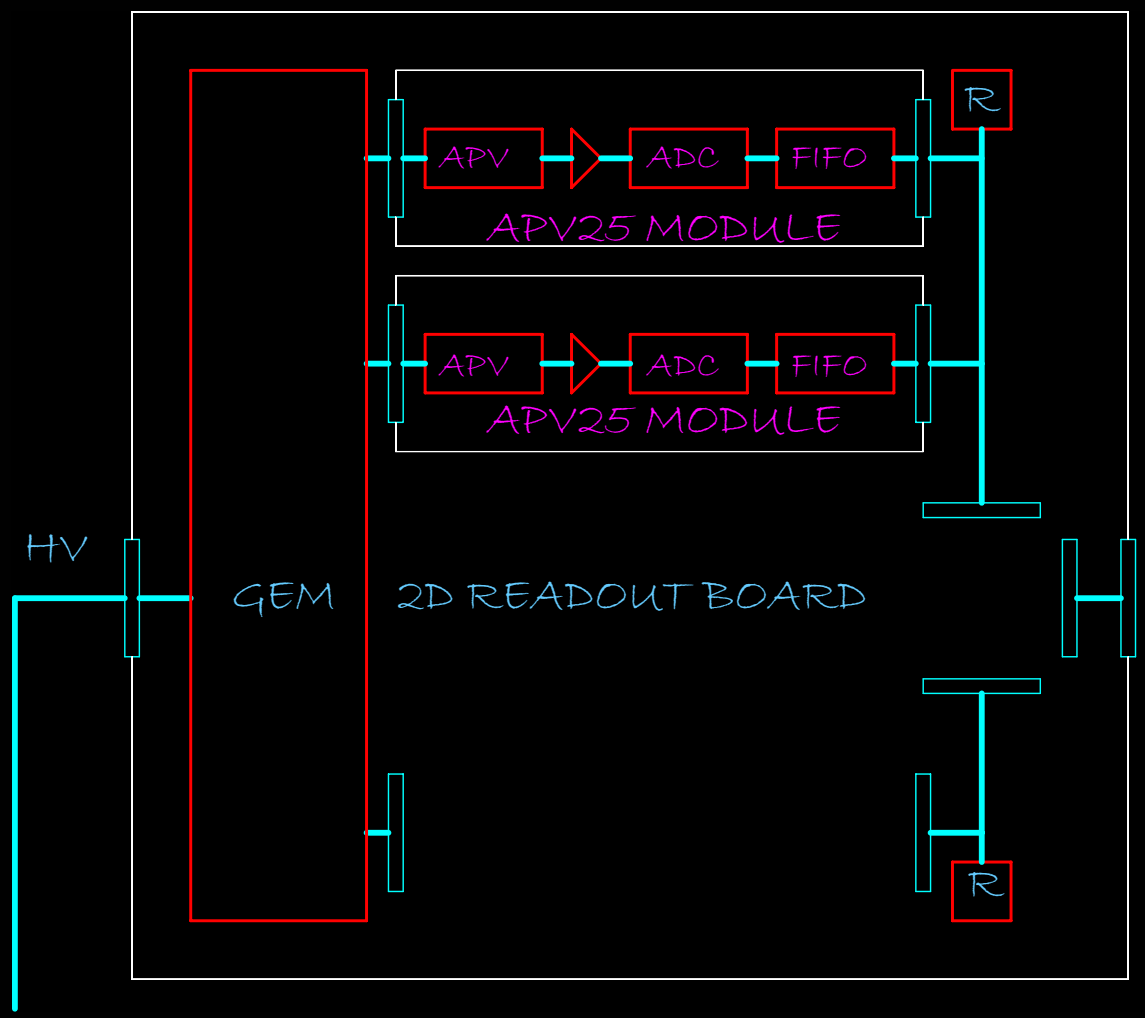


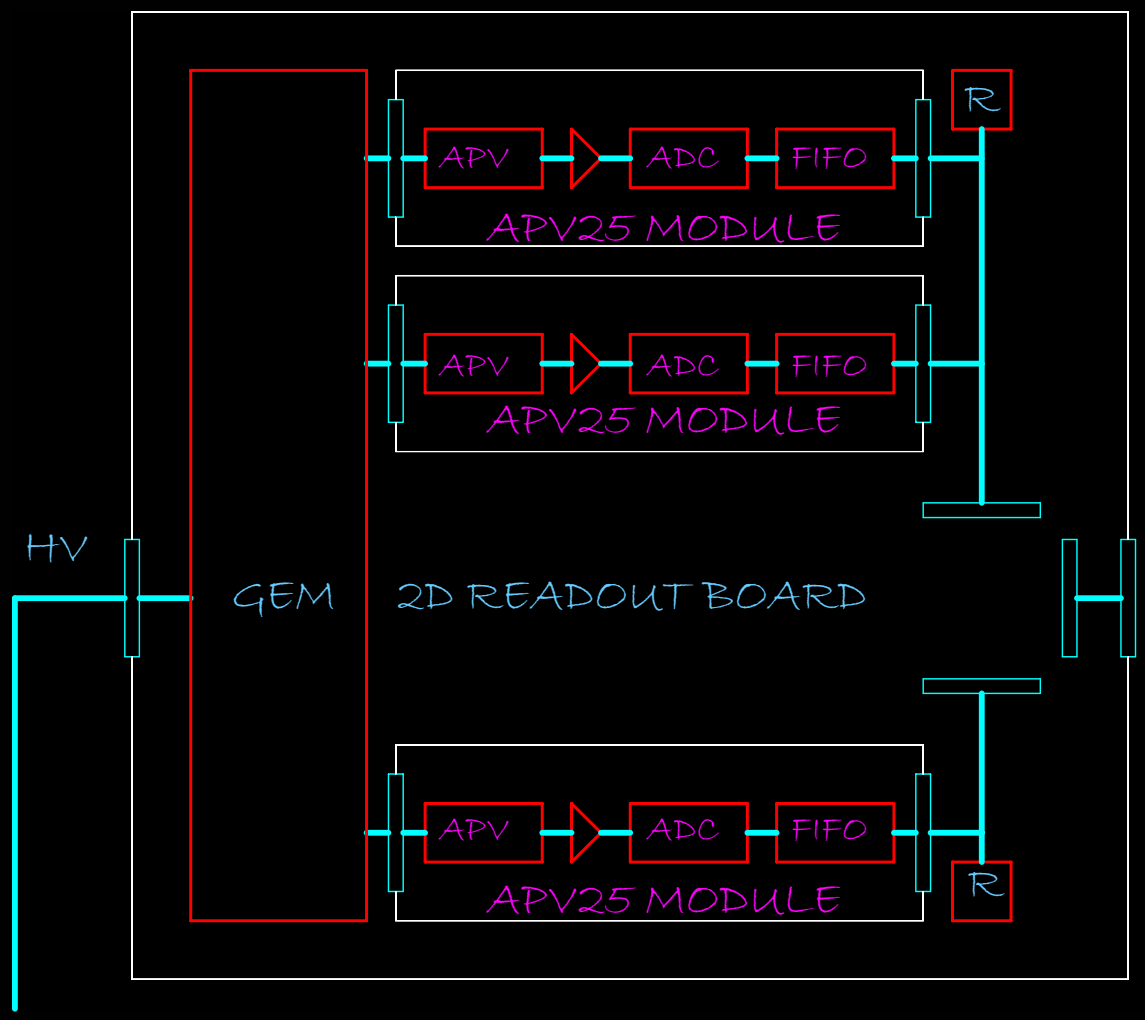

ON ONE 2D GEM READOUT BOARD THERE CAN BY EMPLOYED UP TO 31 APV25 MODULES.

EACH APV25 MODULE IS CONNECTED INTO 64 SENSOR STRIPS.

INTO ONE 2D GEM READOUT SYSTEM CAN BE CONNECTED UP TO 1984 SENSOR CHANNELS.

APV25 MODOLES ARE CONNECTED VIA CONNECTORS INTO 2D BOARD

# APV25 READOUT ARCHITECTURE




IN CASE OF 40MHz READOUT CLK:

DEAD TIME

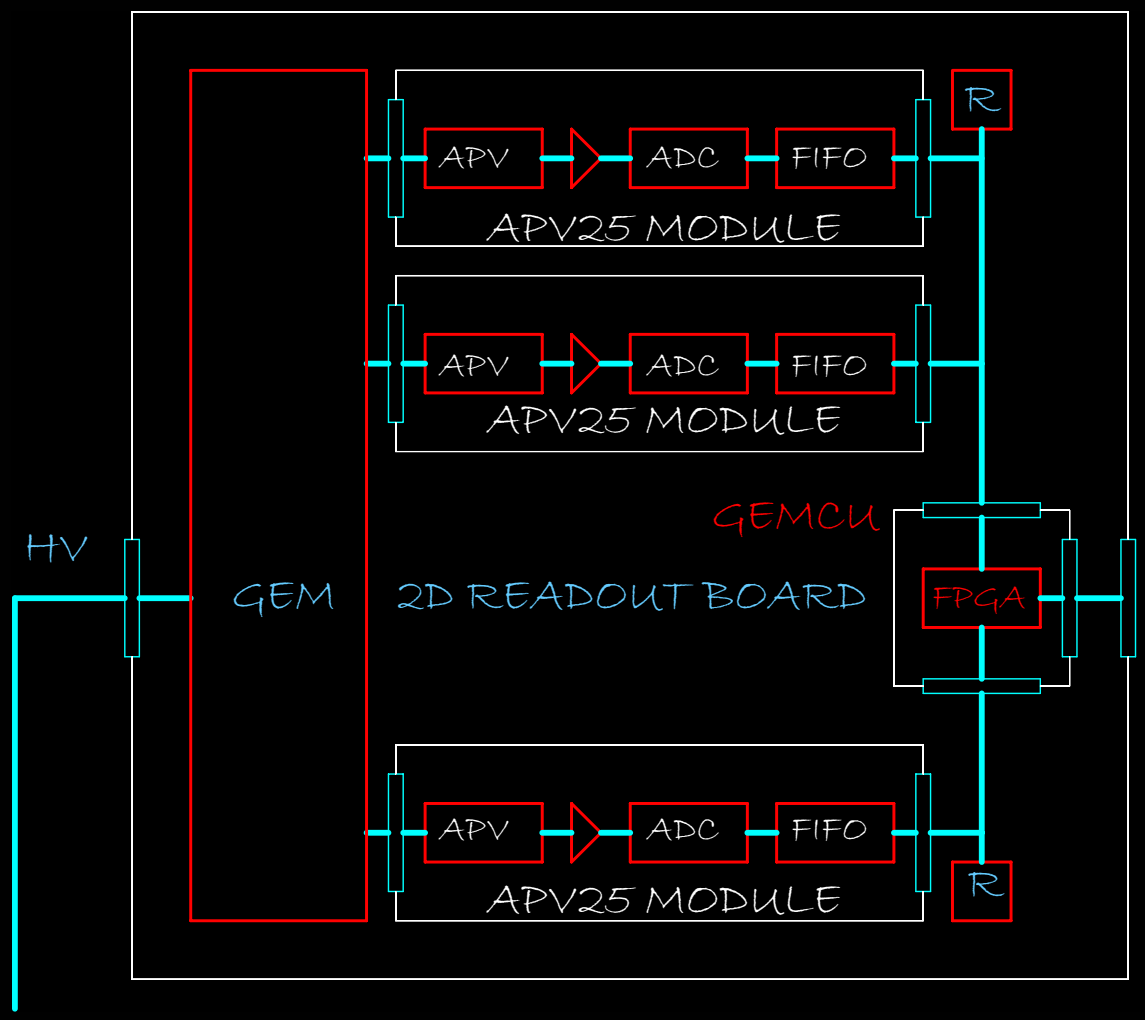
FOR WHOLE 2D GEM READOUT SYSTEM WITH MAXIMUM NUMBER OF 1984CHANNELS (31 MODULES) IS LESS THEN 1 MILISECOND.

NOTE:

BECAUSE ALL GEMs ENGAGED IN DETECTOR SYSTEM WORK PARALLEL, THE DEAD TIME FOR WHOLE DETECTOR SYSTEM WITH N 2D GEMs IN SYSTEM WILL BE LESS THEN 1 MILISECOND.

APV25 MODOLES ARE CONNECTED VIA CONNECTORS INTO 2D BOARD

# APV25 READOUT ARCHITECTURE



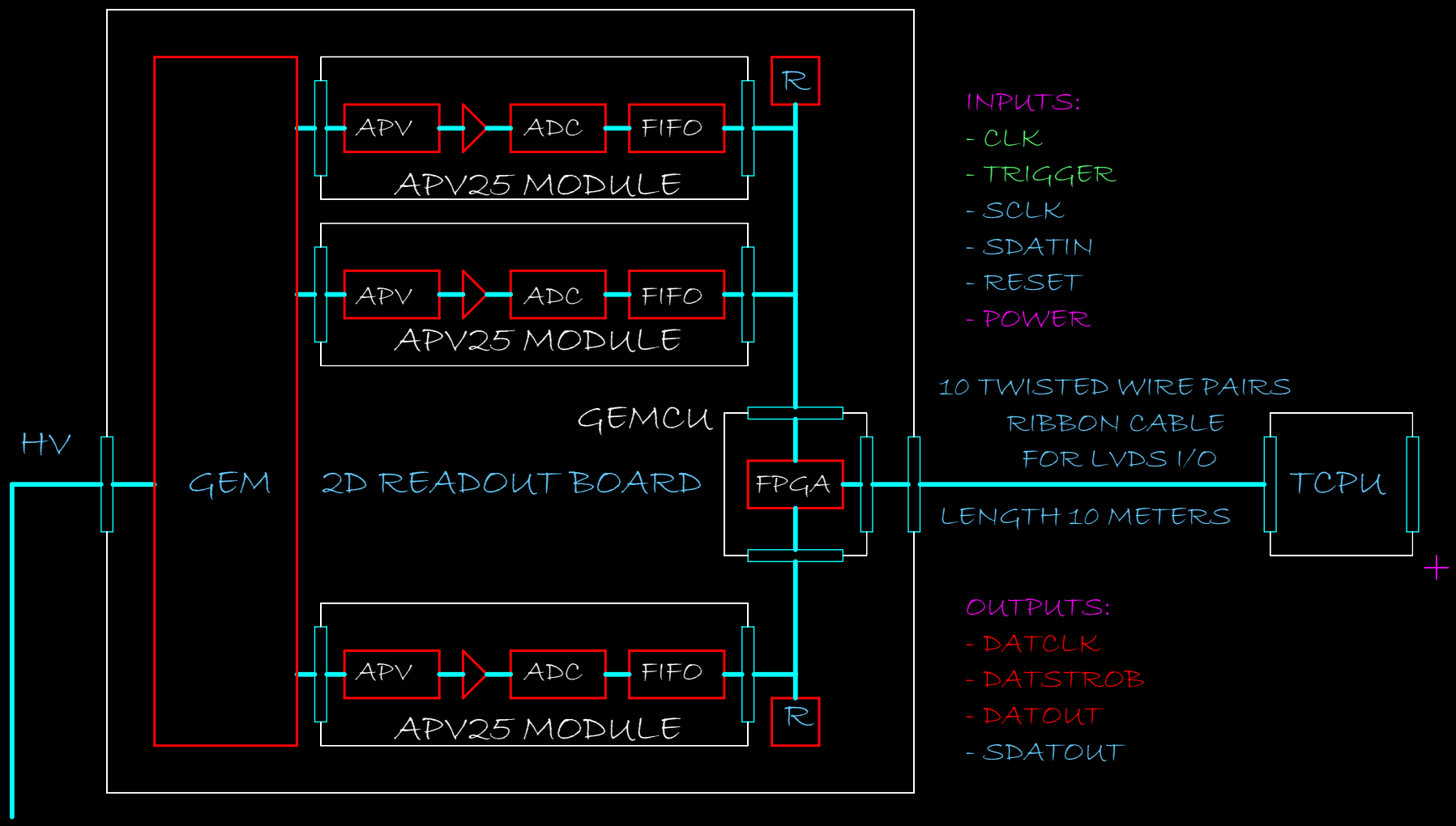

MAIN COMPONENT FOR GEM CONTROL UNIT (GEMCU) IS XILINX FPGA DEVICE, VIRTEX-II XC2V80-6FG256.

THIS FPGA WILL BE PROGRAMMED FOR COMMUNICATION WITH DAQ SIDE AND FOR PROCESSING, FORMATING, ORGANIZING SERIALIZING AND DATA TRANSMITTING DOWN TO DAQ SIDE.

ALSO WILL BE PROGRAMMED FOR I/O STANDARDS CONVERSIONS.

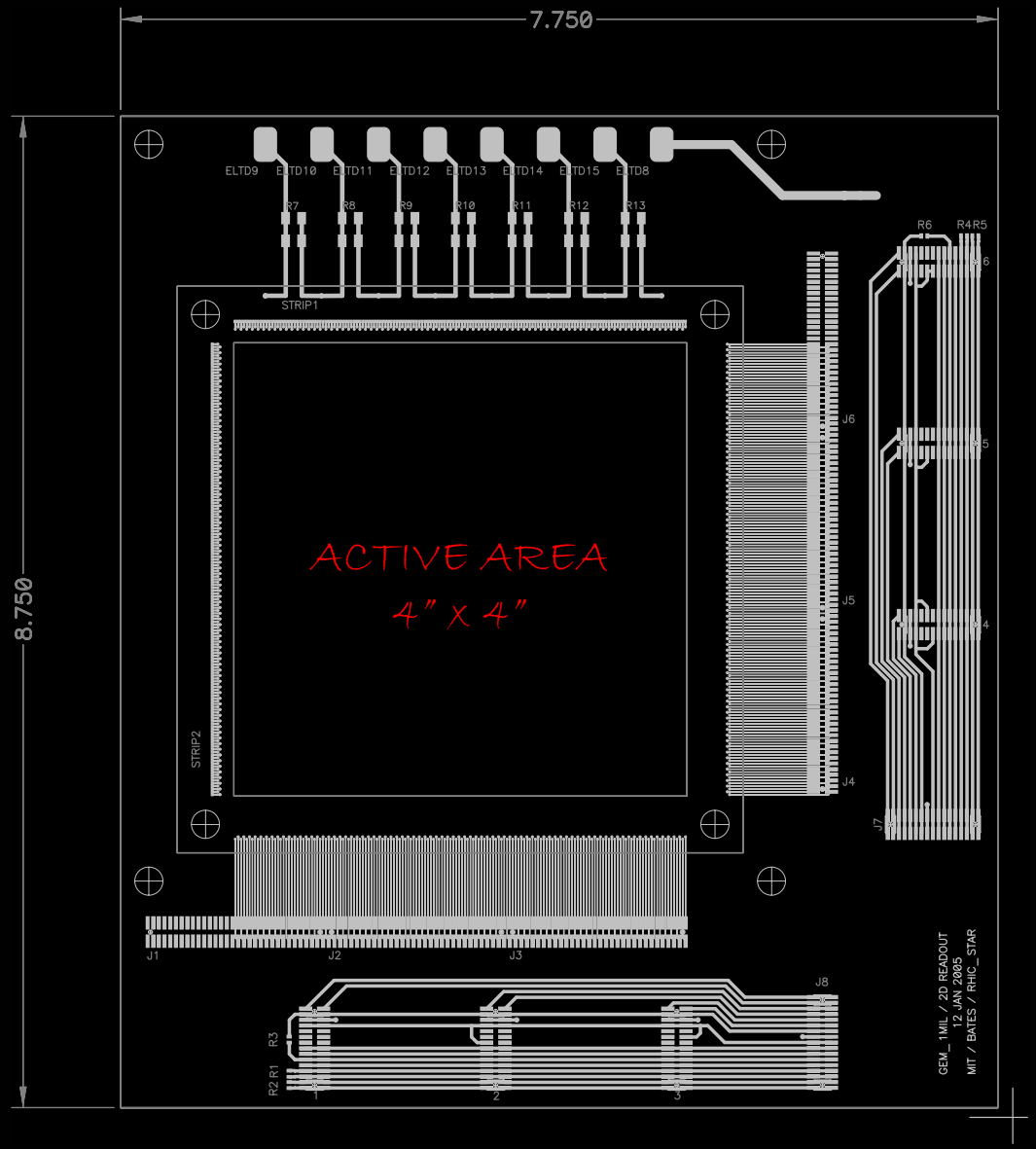
ALSO GEMCU HAS CONNECTION VIA CONNECTOR INTO 2D BOARD

# APV25 READOUT ARCHITECTURE

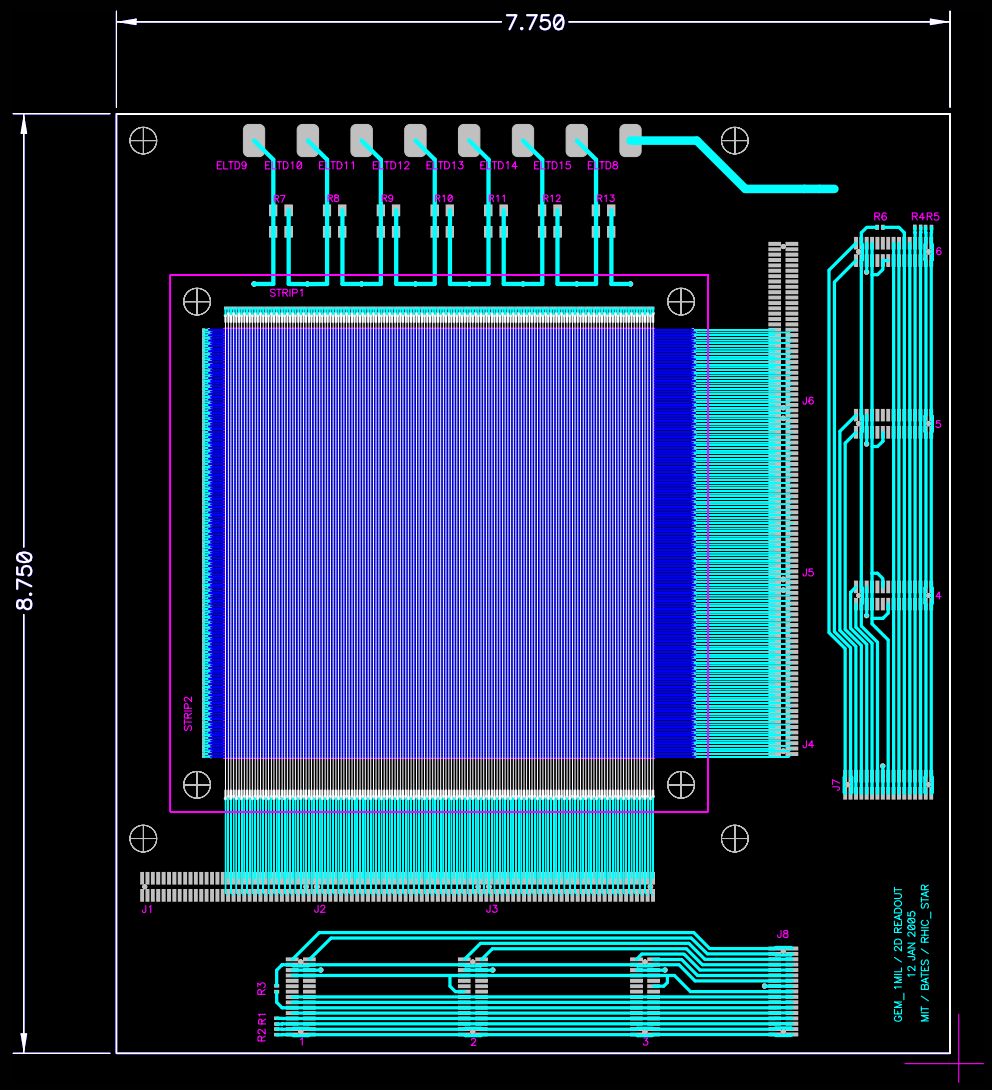



GEMCU IS CONNECTED VIA TCPU UNIT (FROM CERNTECH) TO DAQ

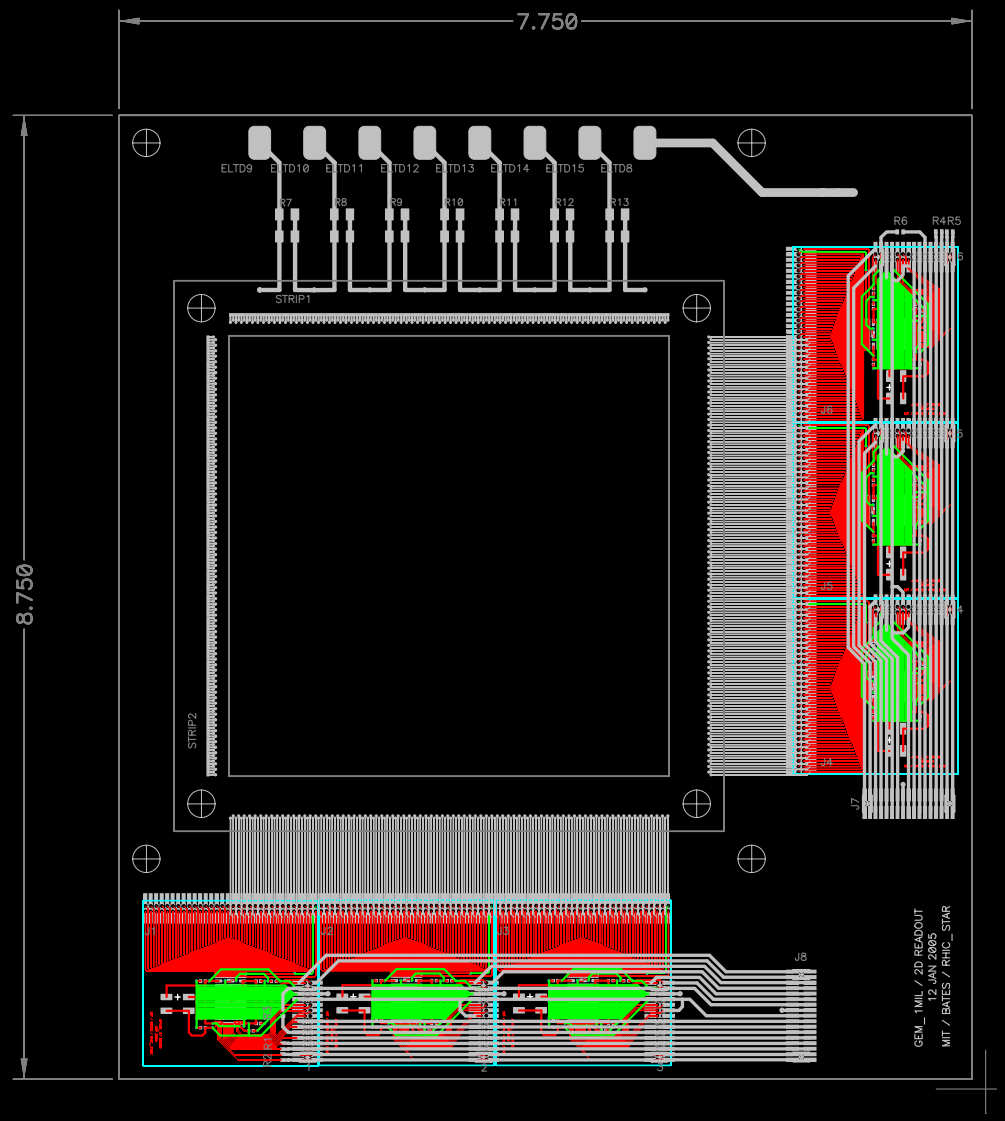
# READOUT ELECTRONICS IMPLEMENTED ON BACKSIDE OF GEM DETECTOR



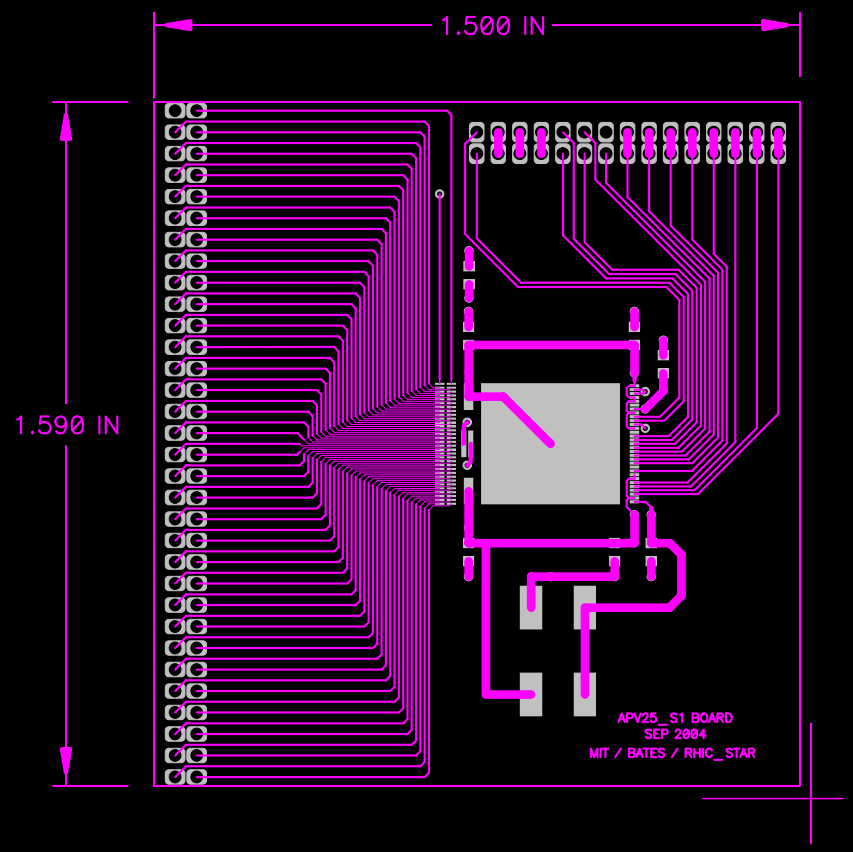
# X-RAY PICTURE OF GEM DETECTOR
# VIA CONNECTING SENSOR STRIPS WITH READOUT LINES



# GEM DETECTOR ASSEMBLED WITH SIX APV25 READOUT MODULES



# APV25 READOUT MODULE



# APV25-S1 READOUT CHIP / 8.1mm x 7.1mm

0.5 MICRON CMOS PROCCESS
128 CHANNELS EACH WITH
192 ANALOG MEMORY CELLS

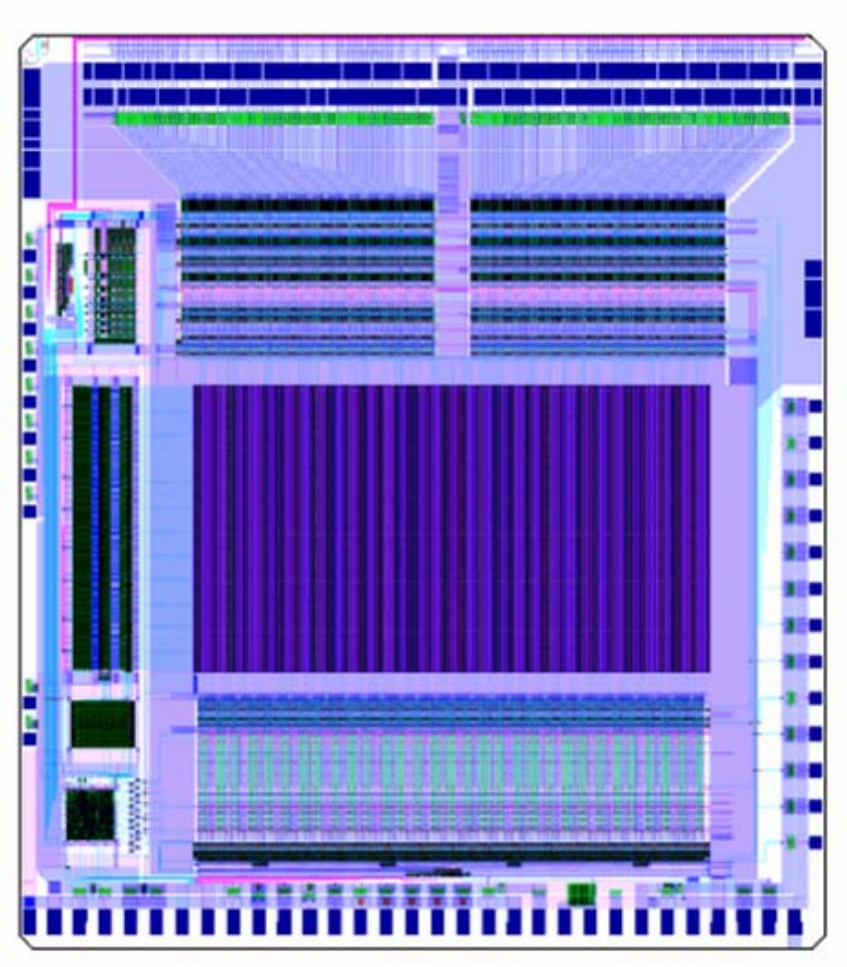
40 MHz SAMPLING FREQUENCY
3 MODES OF READOUT
25ns / 50ns SHAPING TIME

+ / - 1.25V OPERATIONAL VOLTAGE
194mW / CHIP POWER CONSUMPTION
I2C CONTROL / PHILIPS STANDARD

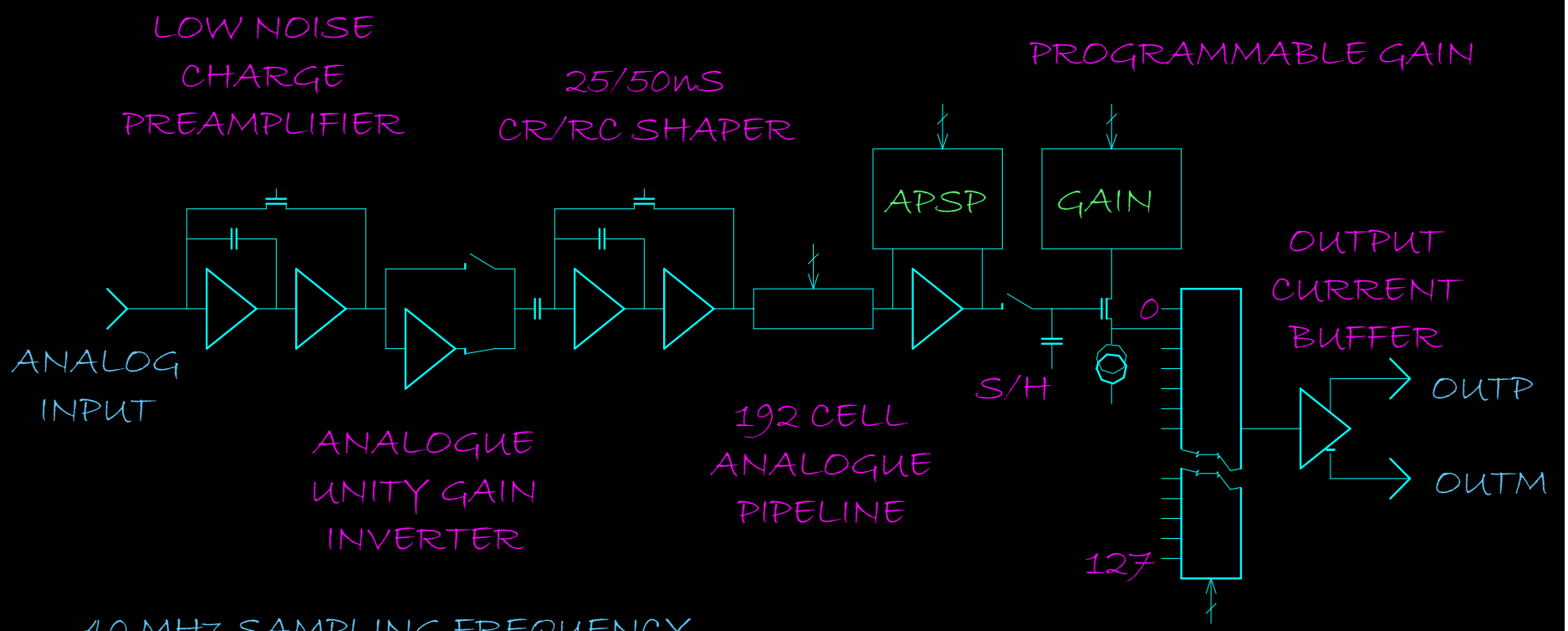
ON CHIP PROGRAMMABLE
BIAS GENERATORS AND TEST PULSE

GAIN 1mA / MIP

MIP = 22400e- = 3.6fC



# APV25-S1 / 1 OF THE 128 CHANNELS



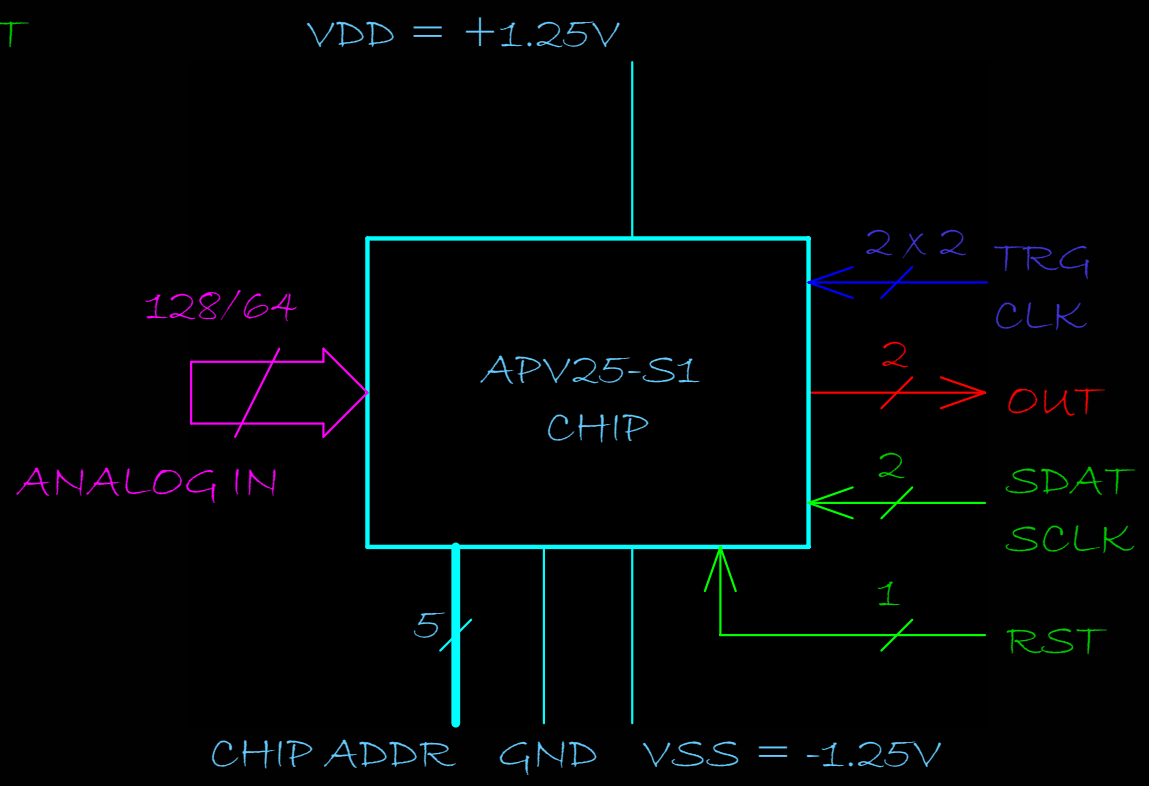

40 MHz SAMPLING FREQUENCY
+/- 1.2 OPERATIONAL VOLTAGE
GAIN 1mA / MIP

# CONTROL SIGNALS FOR APV25-S1 CHIP

TRG/CLK
LVDS = 1.2V +/_ 0.2V

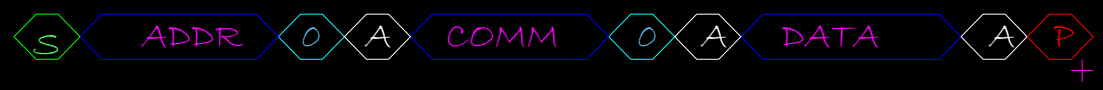
SDAT/SCLK/RST
I/O = +/- 1.25V

OUT = +/- 4mA

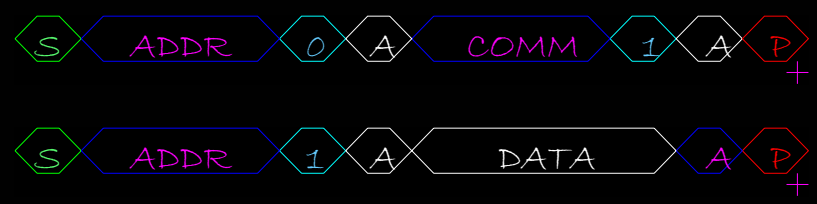


# APV25-S1 / I2C COMMUNICATION FORMAT

## WRITE TO APV25-S1 CHIP




## READOUT FROM APV25-S1 CHIP



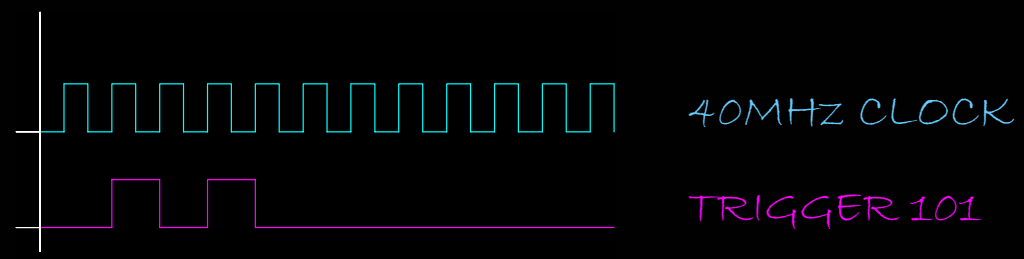
# I2C COMMAND CODES:

(WE HAVE THERE 18 APV25-S1 COMMANDS)

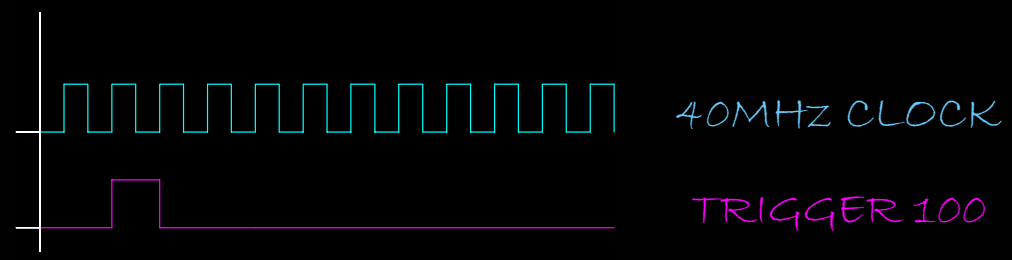
| | | |
|---|---|---|
| IPRE | 001 0000 X | PREAMP INPUT FET CURRENT BIAS |
| IPCASC | 001 0001 X | PREAMP CASCODE CURRENT BIAS |
| IPSF | 001 0010 X | PREAMP SOURCE FOLLOWER CURRENT BIAS |
| ISHA | 001 0011 X | SHAPER INPUT FET CURRENT BIAS |
| ISSF | 001 0100 X | SHAPER SOURCE FOLLOWER CURRENT BIAS |
| IPSP | 001 0101 X | APSP CURRENT BIAS |
| IMUXIN | 001 0110 X | MULTIPLEX INPUT CURRENT BIAS |
| ISPARE | 001 0111 X | NOT USED |
| ICAL | 001 1000 X | CALIBRATE EDGE GENERATOR CURRENT BIAS |
| VFP | 001 1001 X | PREAMP FEEDBACK VOLTAGE BIAS |
| VFS | 001 1010 X | SHAPER FEEDBACK VOLTAGE BIAS |
| VPSP | 001 1011 X | APSP VOLTAGE LEVEL ADJUST |
| CDRV | 001 1100 X | CALIBRATE OUTPUT MASK |
| CSEL | 001 1101 X | CALIBRATE DELAY SELECT |
| MODE | 000 0001 X | MODE OF CHIP OPERATION |
| LATENCY | 000 0010 X | DELAY BETWEEN WRITE AND TRIGGER POINTERS |
| MUXGAIN | 000 0011 X | SET GAIN OF MULTIPLEXER |
| ERROR | 000 0000 1 | HOLDS ERROR FLAGS |

# RUNNING THE APV25-S1 CHIP

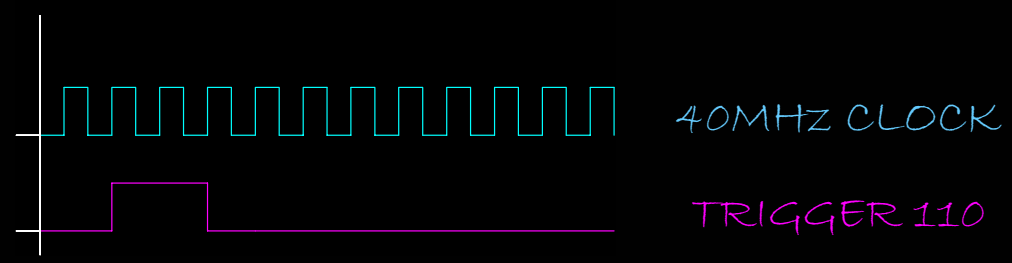
A) RESET




B) TRIGGER

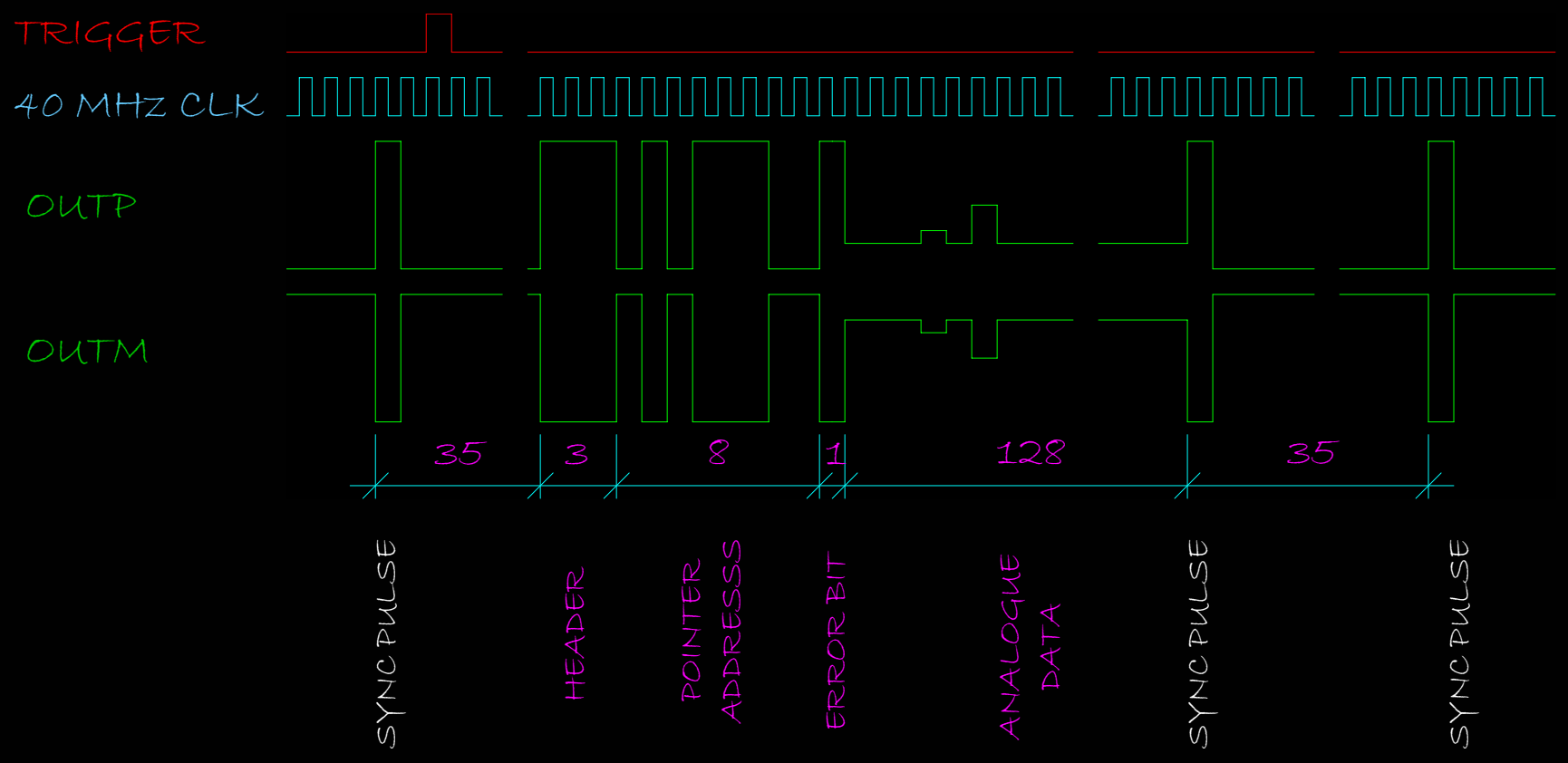


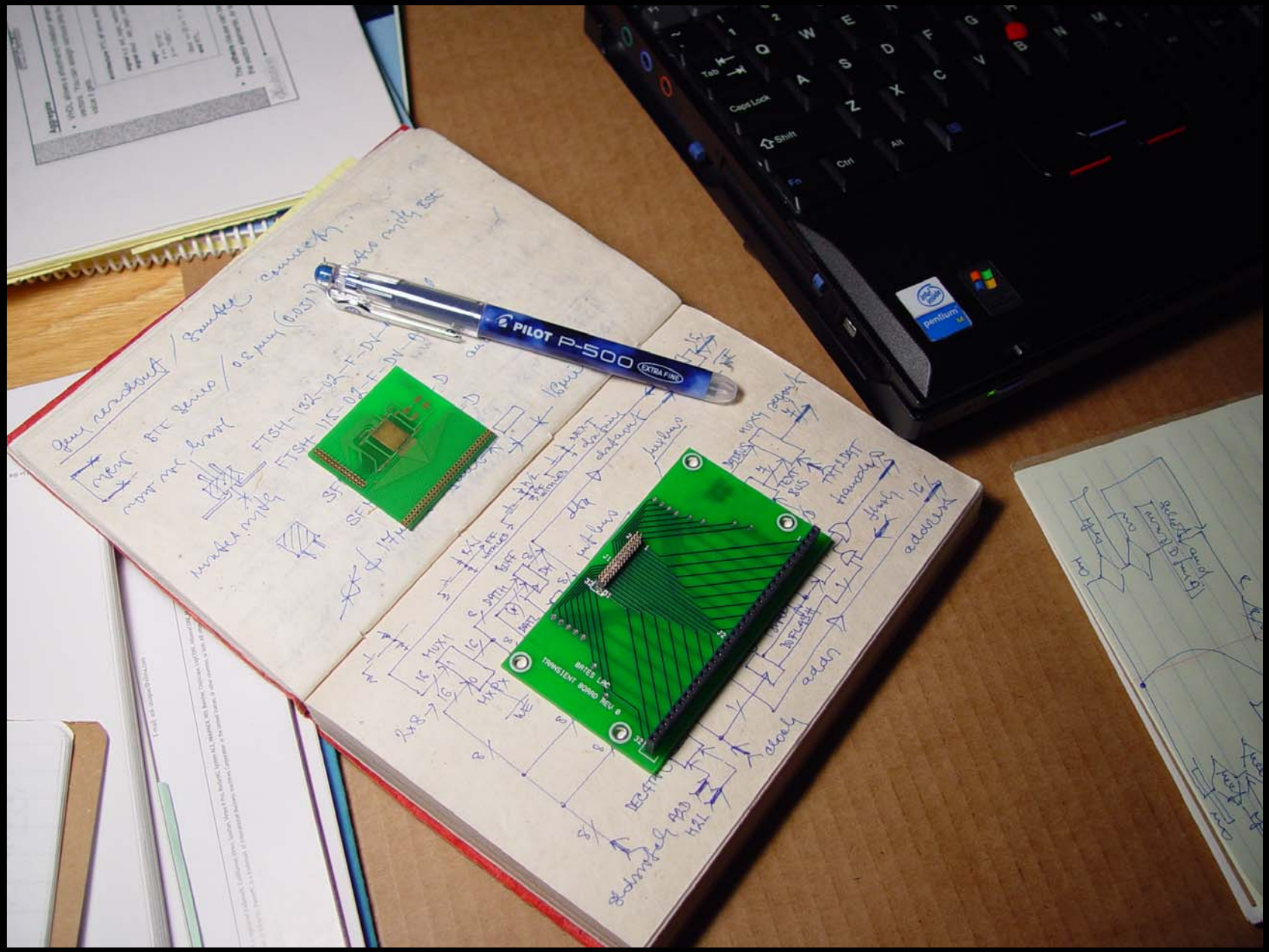

C) TEST PULSE



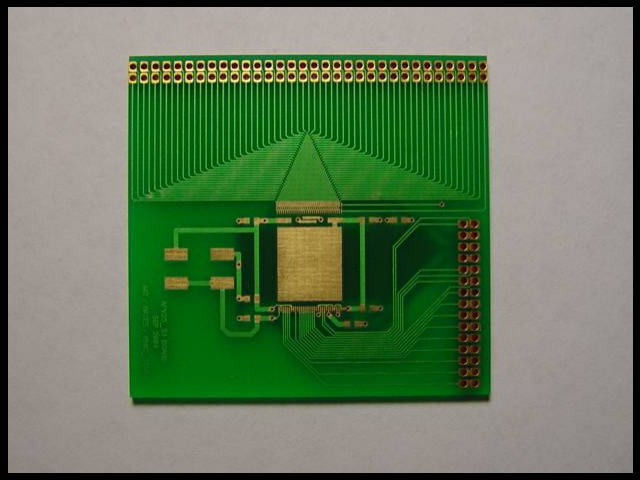
# DATA OUTPUT FORMAT

CHANNEL NO. = 32*(nMOD4) + 8*INT(n/4) - 31*INT(n/16)

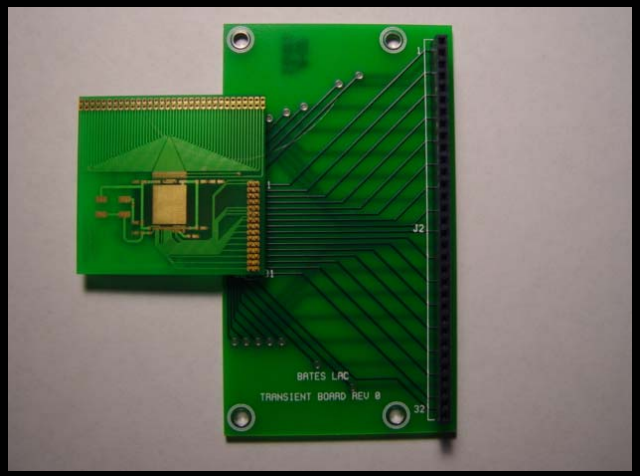



PILOT P-500
EXTRA FINE
BATES LPC
TRANSIENT BOARD REV 0

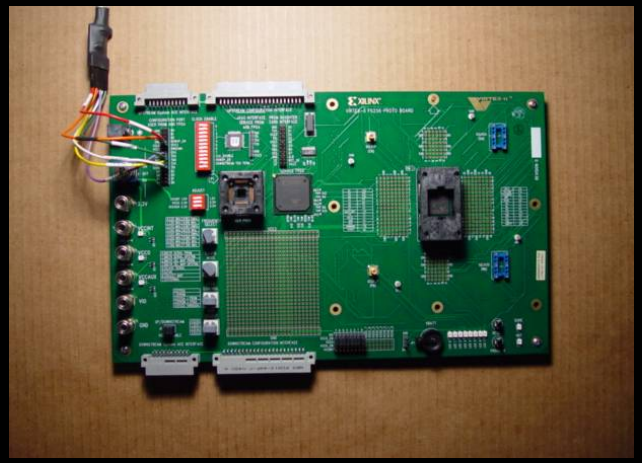
# ELECTRONICS FOR TEST APV25 READOUT



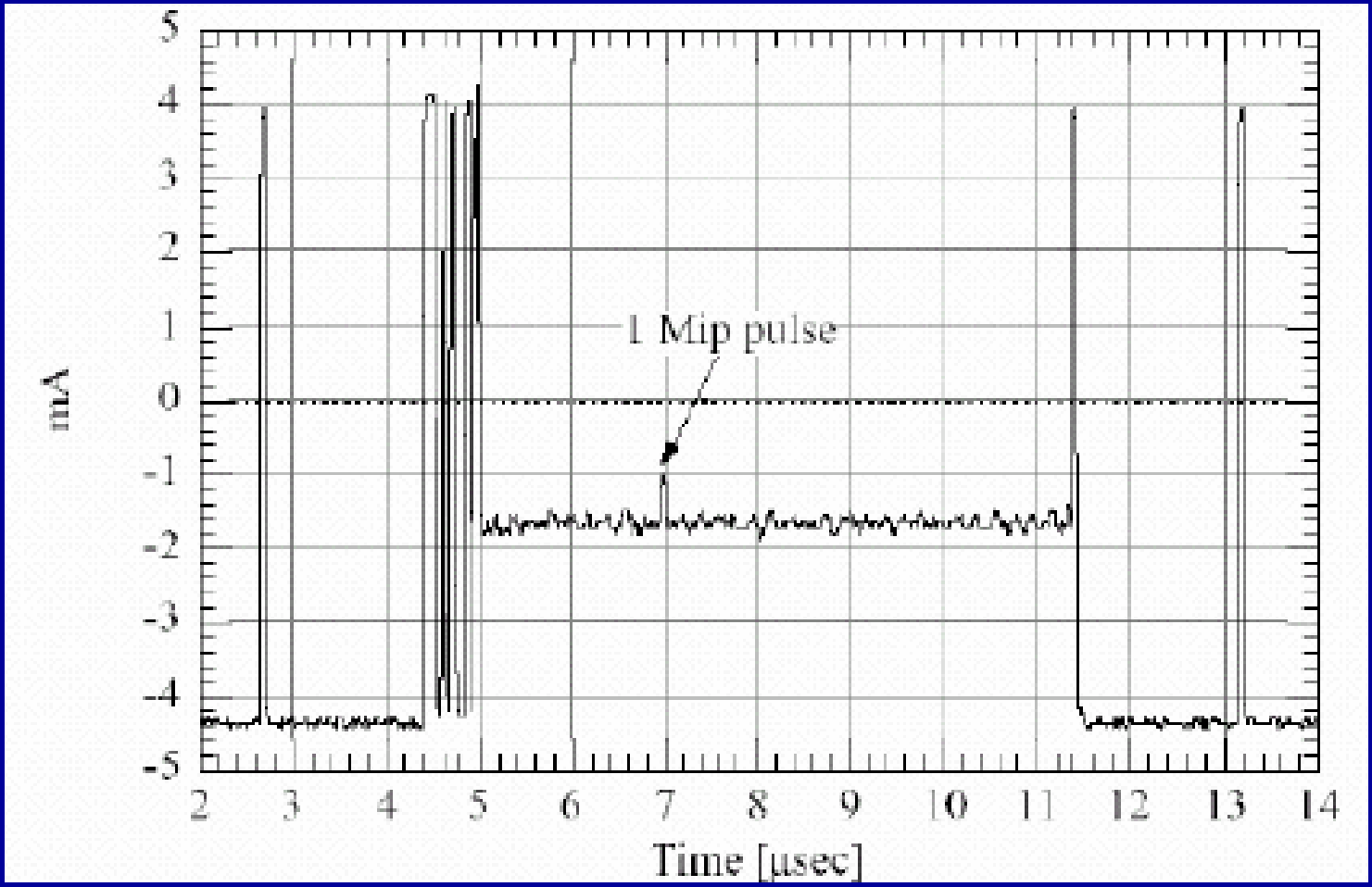
APV25 MODULE




RTANSIENT BOARD



FPGA MODULE / XC2V80-6FG256

ADC / LTC2248

# APV25-S1 READ WITH OSCILOSCOPE