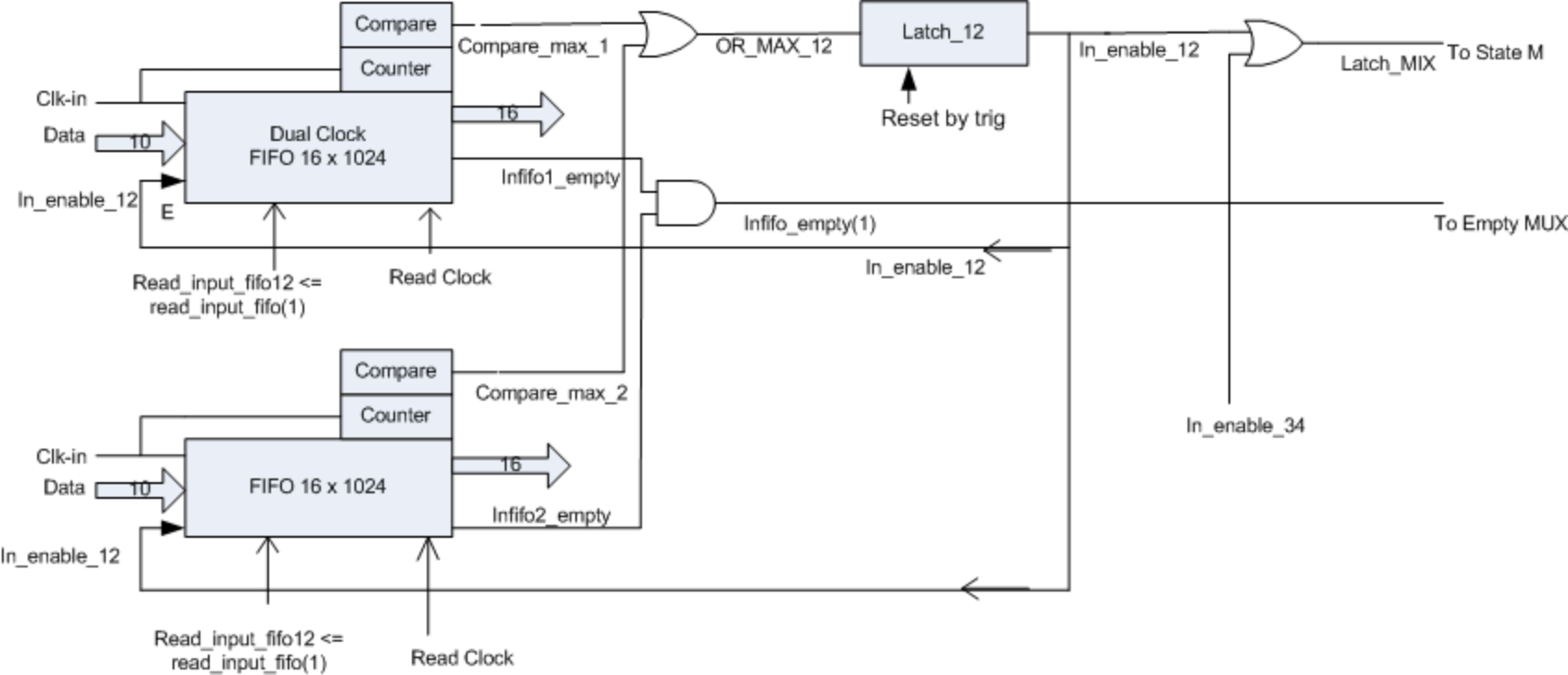
Compare
Counter
Compare_max_1
OR_MAX_12
Latch_12
In_enable_12
Latch_MIX
To State M
Clk-in
Data
10
Dual Clock
FIFO 16 x 1024
16
Reset by trig
Infifo1_empty
In_enable_12
E
Infifo_empty(1)
To Empty MUX
Read_input_fifo12 <=
read_input_fifo(1)
Read Clock
In_enable_12
Compare
Counter
Compare_max_2
In_enable_34
Clk-in
Data
10
FIFO 16 x 1024
16
Infifo2_empty
In_enable_12
Read_input_fifo12 <=
read_input_fifo(1)
Read Clock