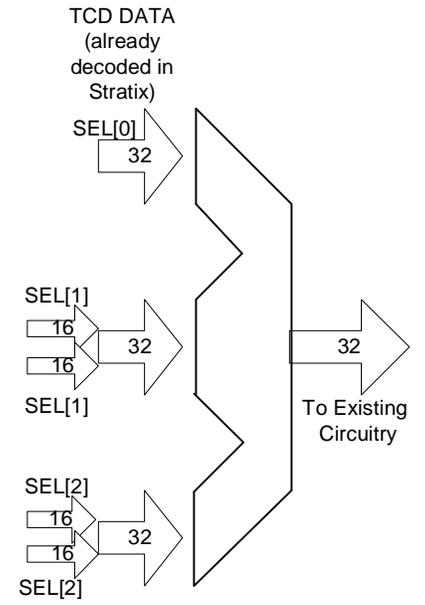
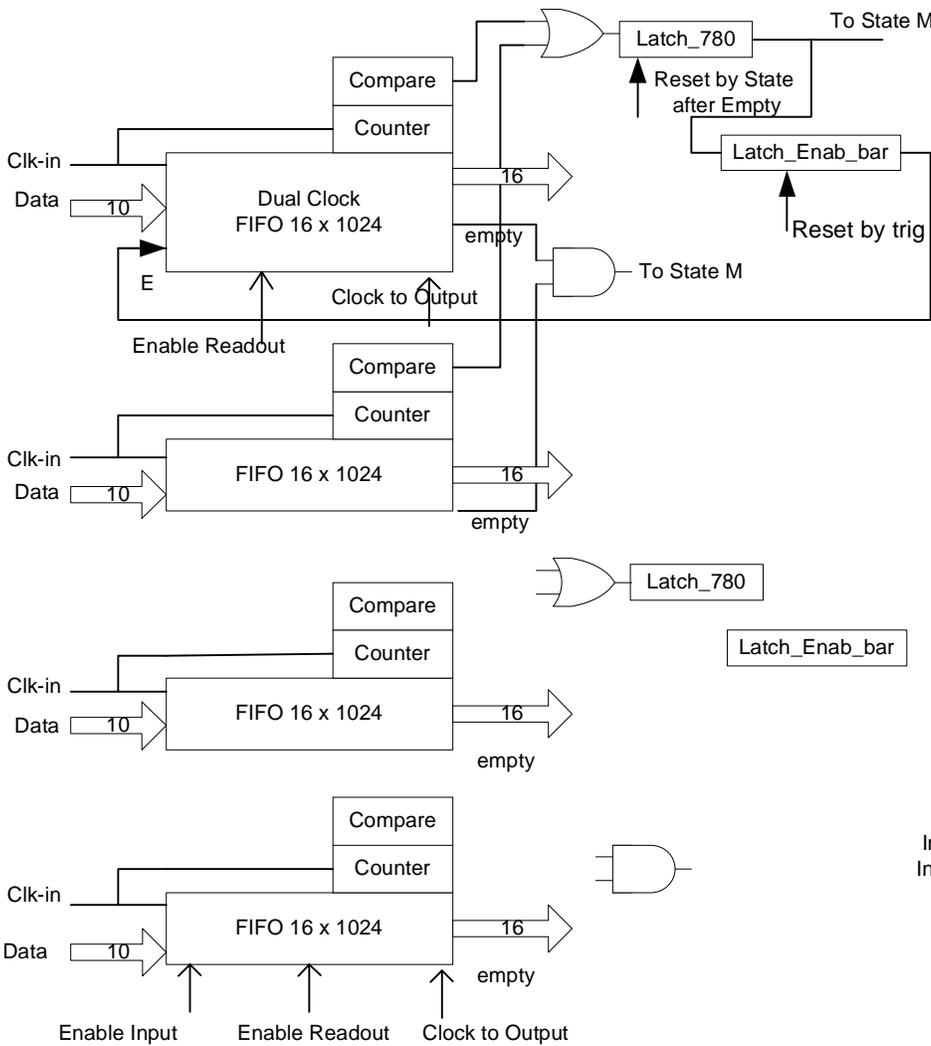
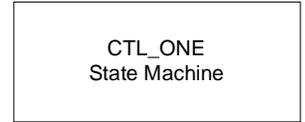
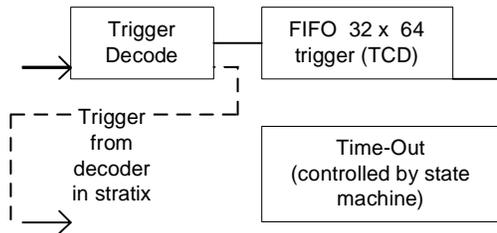


# Conceptual drawing of new TCPU input and Multiplexer

Rev. Nov 22, 2005

Counter is part of FIFO  
State Machine somewhat different than for TOF  
Decodes for 5 MUX from both MCU and FPGA  
but last 2 decodes don't do anything



Previously a 5-way mux

In(15 down to 0) <= Sig1(15 down to 0);  
In(31 down to 16) <= Sig2(15 down to 0);