

4.6 Electronics Design

A Time-of-Flight system measures time intervals, which are defined by independent electronic measurements of one “start time” and some number of “stop times” in each experimental event. While different detectors are used on the start and stop sides, important advantages are gained by performing both the start and stop digitization in the same electronics. This is a common trait of all successful TOF detector systems. In the STAR TOFp [4] and TOFr systems, digitization is performed on the platform using the pVPD signals as direct electronic starts for both the stop detector and the pVPD digitization (see section 4.9 and appendix B). However, for the proposed system, one cannot possibly distribute electronic signals from the start detector to each stop detector (*i.e.* each tray) in time. Also, one could not possibly integrate a system into STAR that digitizes 23k detector channels using long cables and a huge bank of CAMAC or Fastbus electronics. For the proposed system, one must instead digitize versus a clock, and transmit from the detector digital data, instead of logic signals to be digitized elsewhere. The information ultimately needed for timing analyses are still available, as $(\text{stop-clock}) - (\text{start-clock}) = \text{stop-start}$, so long as the clocks used on both the start and stop sides are the same to 10-20 ps in every event. Additional comments on the start detector are presented in section 4.9 below.

The following discussion of the proposed electronics for the large-area TOF system is unchanged from when it was first written in May 2002 except as noted below. It was reviewed by STAR in September 2002 and by the BNL Detector Advisory Committee in December 2002 and November 2003. There are number of small changes that have occurred during two years of R&D that are reflected in the WBS, presented in Appendix C. A top level description of the electronics using the current nomenclature also is available in Appendix C.

The following changes have occurred. The fast comparator has been moved from the TFEE card to the TDIG card and the TFEE card is now called TAMP. We are using the Maxim 9601 comparator on TDIG and the Maxim 3664 preamplifier on TAMP. The interface between the start detector PMTs and TDIG is now called TPMT instead of TFEEb. The TMIT card will be mounted outside the pole tip instead of on the tray. There will be only 4 TMIT cards and they will be daughter cards to 4 THUB cards. Each THUB/TMIT will interface 30 or 31 TCPU cards to trigger and DAQ. We plan to use the CERN/ALICE DDL-SIU optical interface cards for the TMIT function. We plan to use the CERN/ALICE RORC (read-out receiver card) for the TDRC function and the description of the DAQ receiver in section 4.6.6 has been updated to reflect this. The description of HPTDC R&D at the end of section 4.6.2 has been updated to reflect the current status.

Shown in Figure 32 is the top-level diagram of the electronics for the start and stop sides of the present system. The electronics chain on the start side is very similar to that on the stop side by design. The individual electronics boards seen in this figure are discussed in detail in this and the following subsections.

Each tray consists of 192 detector channels and three different types of circuit cards. These types are called TFEE, TDIG, and TCPU, listed in order of the flow

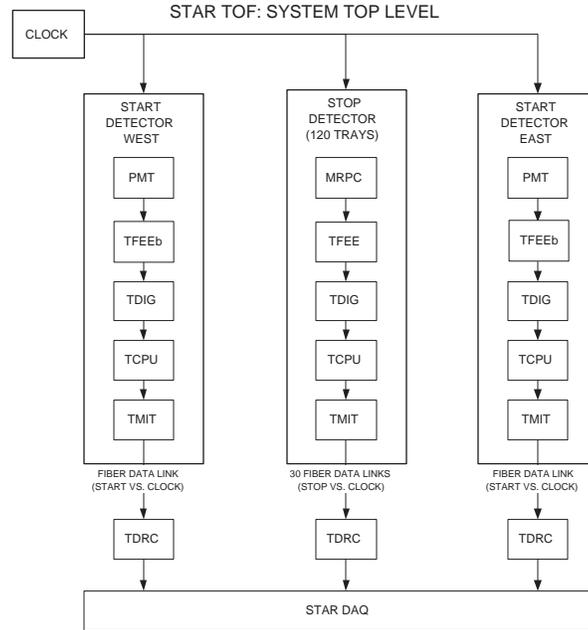


Figure 32: The highest-level diagram of the electronics for the proposed system.

of information from the detector. Every fourth tray also contains a TMIT card that transmits the data to STAR DAQ. The TFEE contains the analog front end electronics and also serves as the top of the gas box and the signal feedthrough. The $\sim 10''$ long twisted-pair cables from the detector pickup pads are connected to the feed-through. The TFEE pass their output to the TDIG, which digitizes and buffers the detector information. This information is passed to TCPU which formats and buffers the digital detector information. This formatted data is passed to TMIT, which transmits it over an optical fiber to the data receiver TDRC in the STAR DAQ room.

Shown in Figure 33 is the top level electronics diagram at the tray level. The system interfaces include:

- a fiber optic data communication link via the TDRC to the STAR DAQ (TDC data and command echo),
- a high speed differential data link (PECL or LVDS) for multiplicity data to the STAR Level-0 trigger,
- a command link for acquisition commands from the STAR trigger,
- a high speed differential line (1 signal) for the beam crossing timing signal from the STAR trigger, and
- a serial bus for connecting the system's embedded CPUs to the network for configuration and status.

STAR TOF: TOP LEVEL ELECTRONICS

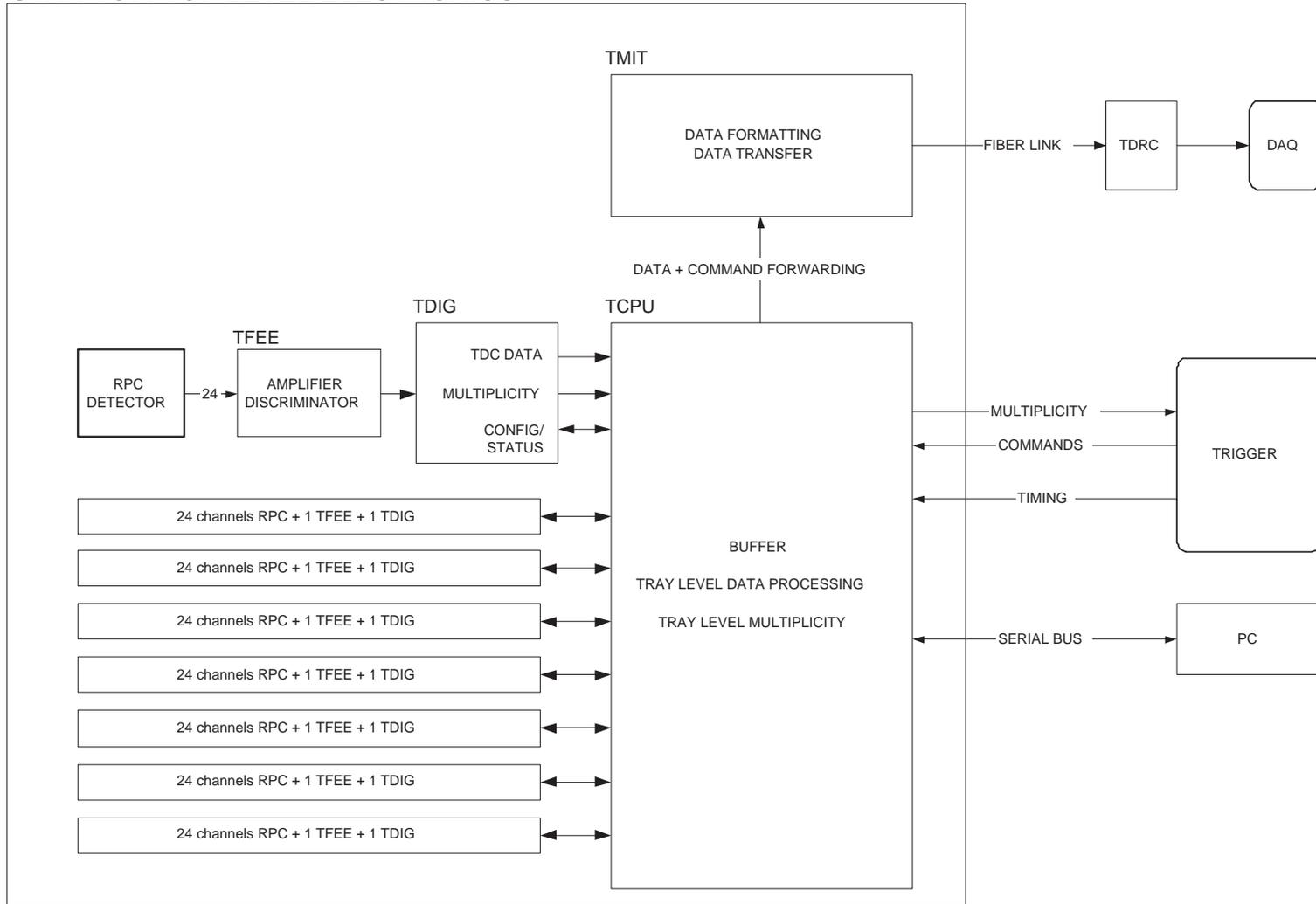


Figure 33: The top level electronics diagram at the tray level.

STAR TOF: PARTITIONING AND DATA FLOW FOR 1 DETECTOR TRAY

NOTE: CLOCK AND CONTROL NOT SHOWN

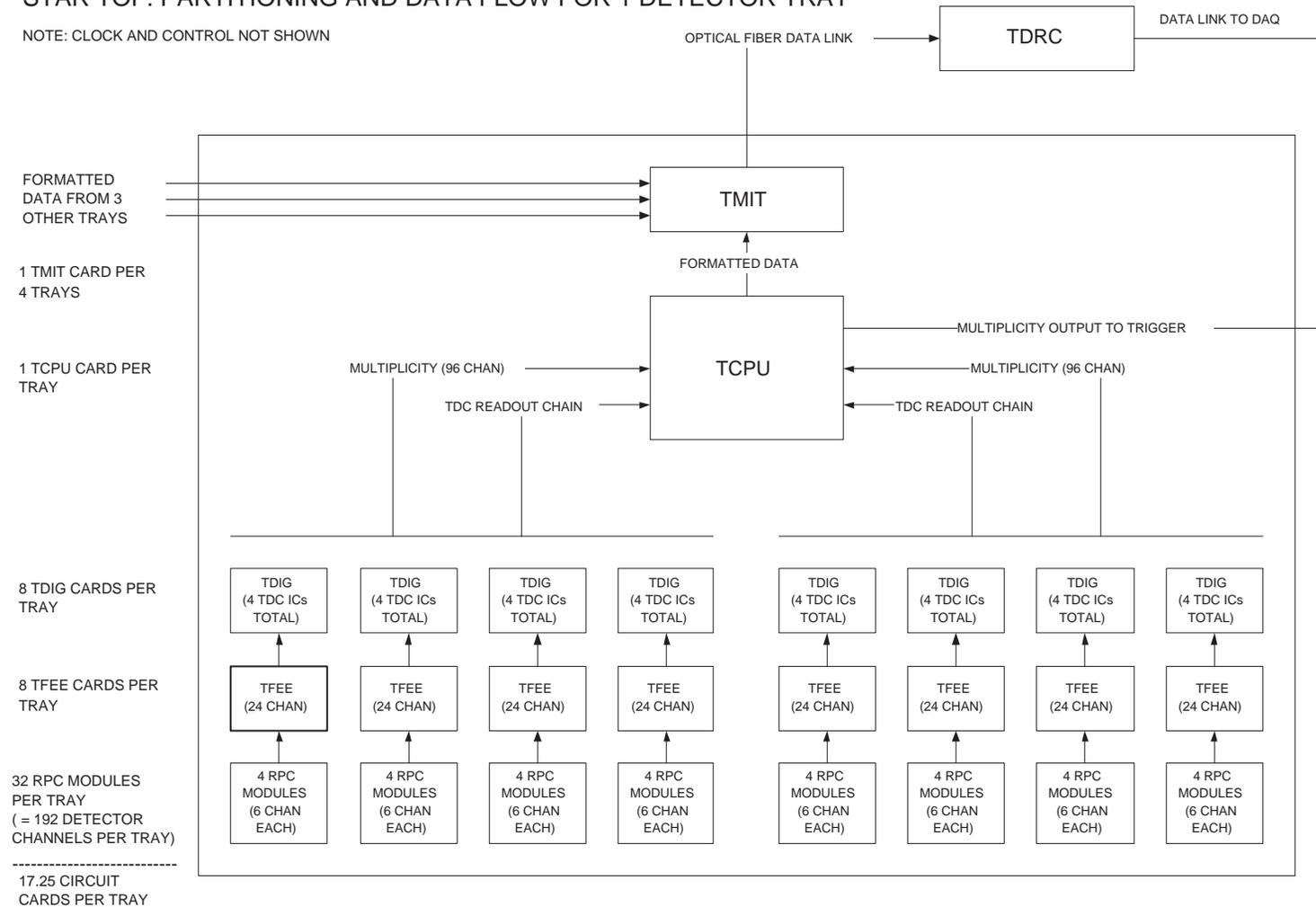


Figure 34: The partitioning of electronics functions between circuit cards.

Each MRPC module contains 6 detector channels. Four modules feed into one TFEE. Each TFEE feeds one TDIG. The 8 TDIG cards in a tray feed into a single TCPU. Data from 4 TCPUs will feed into a single TMIT located as a daughter board on one of the TCPUs. Figure 34 shows the physical partitioning of these different electronics boards and the data flow between them.

Each TFEE card contains the high-bandwidth amplifiers and leading-edge discriminators for 24 detector inputs (4 modules). These two functions are performed by the Maxim 3760 preamplifier and the Analog Devices AD96687 dual comparator. To reduce noise into the low level MRPC output signal, the TFEE is designed as an integral part of the tray mechanical structure. The TFEE will have test inputs and outputs to allow the simulated MRPC signal input and front-end performance measurements using external test equipment (ADCs, TDCs and high performance oscilloscopes) that is independent of the embedded TDC circuitry. This will allow isolated performance measurements of the pre-amplifier, discriminator, and TDC, as well as the comparison of the TDC measurements by TDIG to those when digitizing in CAMAC or in a fast oscilloscope.

Each TDIG card comprises the time-to-digital conversion function for the discriminator outputs from a TFEE, using the HPTDC ASIC under development at CERN for ALICE and CMS. There are eight TDIG cards per tray, and each sees 24 detector channels via one TFEE card. The 4 HPTDC chips on each TDIG card sample rising and falling edges of the discriminated input pulse, giving both leading edge timing and time-over-threshold information (for the slewing correction). The HPTDC chip also contains a buffer for 256 recorded times where stop times are held until read out by the TCPU card. The amplifier/discriminator and TDC functions are physically and electrically separated onto two boards, TFEE and TDIG, to reduce the chance that digital noise from the TDC circuitry will interfere with (i.e. add jitter to) the analog signals in the amplifier/discriminator section.

Each TDIG card also performs the first layer of logic for the multiplicity output, producing the (5-bit) total of active discriminator outputs at each beam crossing interval. This information, aggregated at the tray level by the TCPU card, will be used as an input to the STAR Level-0 trigger. Since the installation of the proposed system implies the removal of the STAR CTB, the system will provide the same kind of multiplicity information for $|\eta| < 1$ to the Level-0 trigger that the CTB did.

There is one TCPU card per detector tray. The TCPU card configures the eight TDIG and TFEE pairs in the tray and controls data acquisition cycles based on commands from the trigger. The TCPU also receives TDC data from the TDIG cards, formats and buffers the data, and transfers the buffered data to the TMIT daughter board for transmission to the DAQ via the TDRC card.

The TMIT circuit implements a high-speed serial communications protocol at the physical layer. Separating this function into a separate daughter board allows a protocol change to occur transparently to the TCPU hardware - only embedded CPU or PLD firmware changes would be necessary.

The TCPU receives a beam crossing timing signal from the trigger, cleans it up (if necessary) and distributes it to the TDCs on the TDIG boards. In normal operation,

the TCPU will configure itself and operate based on embedded firmware, but the TCPU includes a serial bus connection to a host PC to directly control configuration and obtain status during testing and system integration. This data link will be available for remote diagnostics during final assembly and operation of the system.

The TCPU performs the second layer of logic for the multiplicity output, summing 5-bit inputs from four TDIG cards into a 7-bit multiplicity output for a half-tray (96 channels). The TCPU performs this function for each of the two half-tray signal groups and sends the 7-bit result for each group as a 7-bit differential signal during each beam crossing interval. There are 2 multiplicity outputs for each tray; each is 7 bits in parallel, and each bit is differential (2 signal wires).

In the subsections below, we describe each of the five STAR TOF electronics boards in more detail.

4.6.1 TFEE

This card contains preamplifier and discriminator circuits to accommodate 24 pad signals from 4 MRPC modules. A TOF detector tray will have 8 TFEE cards. Each TFEE card will be 8.4"×10.5". The power dissipation will be about 14 Watts per card, or 110 Watts per tray. The principal functions of the TFEE and TDIG are shown in Figure 35.

The preamp device, a Maxim 3760, is a low noise input trans-impedance integrated circuit whose gain and rise time characteristics are well-defined by internal feedback. This part is commercially available for use as a photodiode receiver preamp in data communication applications. Several designs employing this chip have shown excellent timing performance when connected to actual MRPC pads - the Maxim 3760 has been used extensively for the past two years by both the STAR and ALICE TOF groups.

An ultra-high speed integrated circuit comparator, the AD96685, serves as a simple leading-edge discriminator with externally controlled threshold. This circuit has also been demonstrated successfully in both the TOFp and TOFr systems. The output pulse width, *i.e.* the "Time Over Threshold," will be used to infer the input signal pulse height for the slewing correction.

The TFEE is an integral part of the tray mechanical assembly. This results in the shortest signal path and the maximum shielding. The TDIG cards are stacked above their respective TFEE card to reduce RF cabling. Multiplicity sums have dedicated parallel data paths from each TDIG card to the TCPU. The TDCs on the TDIG cards are read over a dedicated bus in groups of 16 TDCs (four TDIG cards), giving 2 data paths from the TDIG cards to the TCPU. All the TDCs are configured via a JTAG serial bus. The threshold DACs and temperature monitors are configured/read from a separate low speed serial bus.

Provisions will be made during the design of the TFEE cards to optionally bypass the preamp section. This will allow these boards (TFEEb) to operate when the inputs are photomultiplier signals, not MRPC signals. This will allow the identical signal processing chain to be used on the start side with no additional board designs. Access to the preamp outputs will also be included for evaluation of MRPC ADC spectra

during the final testing and QA of fully assembled final trays.

A 6-channel version of TFEE was produced for the prototype TOF tray, TOFr (see section 5). This circuit for TOFr had additional functions that will not be required on TFEE such as an amplified analog output and NIM logic signal output. The pre-amplifier, discriminator, and related circuitry will remain the same, so we have a proven design for this card and experience building and testing production boards.

Table VI shows the bench test results for 41 TOFr FEE cards. The jitter in the pre-amplifier was of order 20 ps or less in all but one channel. This is an outstanding result.

These TOFr FEE cards have proved to be reliable. They have been used for testing MRPC modules at CERN, Rice, and in China and 28 six-channel cards were used for the TOFr tests at the AGS. There was one field failure in a single channel, but this channel proved good when re-tested on the bench, so the failure was likely a poor connection to the interface card.

4.6.2 TDIG

The TDIG card measures leading and trailing edge timing for 4 MRPC modules (24 detector channels). These cards are mounted directly on the TFEE cards - one TDIG card per TFEE card. The discriminator signals, clock, multiplicity gate, and L0 trigger readout commands are primary inputs while the hit edge timing data and 5-bit partial multiplicity sums are outputs. The calculation of the pulse width for the time-over-threshold slewing correction, and any resultant data formatting, will occur downstream of this card.

The multichannel HPTDC ASIC developed at CERN for the ALICE and CMS experiments is our first choice for the TDC measurement. In addition to meeting our time resolution requirements, it has efficient and flexible triggering and readout features. The trigger matching function allows acquired data to be read out from the built-in buffer in an order that accounts for trigger latency. As a backup, we will evaluate a device under development at the University of Oulu in Finland. The Oulu device as specified has adequate timing resolution but does not include readout features of the CERN HPTDC. However, the Oulu TDC is a full custom CMOS ASIC achieving 20 picosecond timing precision with very low power consumption of <5 mW/channel. NASA is currently evaluating chips they have received from Oulu.

Leading edge timing for 24 channels with 25 ps binning will be provided by 3 HPTDC devices operating in 8 channel, Very Hi Res mode. The trailing edge times of all 24 channels will be determined by 1 device operating in 32 channel Hi Res mode with 100 ps time bins. A built in hardware handshake protocol allows 16 HPTDC devices to share a 80 Mbit/sec serial output port so that only 2 data cables are required per CTB tray (4 TDIG boards, 96 MRPC pads each).

Additionally, this card will have slow serial interfaces for TDC and logic configuration, control of discriminator threshold and temperature monitoring. Estimated power consumption is about 10 watts per board or 80 watts per tray.

We have on hand 250 HPTDC chips from the first CERN production run and have

Board	Status	Chan 1	Chan 2	Chan 3	Chan 4	Chan 5	Chan 6
4	OK	16.0	16.0	18.0	16.0	18.0	17.0
5	OK	15.0	16.0	16.0	16.0	16.0	16.0
6	OK	16.2	16.7	15.8	18.8	17.8	16.1
7	OK	16.0	14.0	18.0	18.0	17.0	20.0
8	OK	16.0	19.0	16.0	19.0	16.0	16.0
9	OK	16.7	17.2	15.8	14.8	16.3	16.0
10	OK	16.9	18.6	17.3	18.9	19.7	17.8
11	OK	16.9	18.0	15.0	19.4	16.8	17.3
12	OK	17.4	17.4	20.1	20.5	15.2	16.5
13	OK	17.7	21.0	18.9	17.8	17.8	17.3
14	failed						
15	failed&fixed	14.8	13.9	22.0	15.5	23.2	21.1
16	OK	18.4	18.4	15.8	20.0	19.2	19.7
17	OK	16.5	14.8	20.3	18.5	16.5	20.7
18	OK	15.7	15.0	16.3	19.0	19.2	16.9
19	OK	16.3	16.4	18.0	18.2	17.4	18.8
20	OK	16.2	19.6	17.3	19.7	15.6	18.8
21	OK	16.8	17.0	17.6	17.9	15.3	17.0
22	OK	15.8	15.1	17.1	20.2	20.4	16.9
23	OK	18.3	19.3	15.0	17.6	19.8	16.7
24	don't use	18.2	18.9	33.8	15.5	16.4	17.3
25	OK	15.8	14.5	16.5	15.4	16.7	18.6
26	OK	17.7	18.5	16.2	16.8	17.7	19.2
27	OK	14.7	20.3	20.5	19.3	20.1	18.1
28	OK	18.1	16.8	17.8	16.5	17.5	16.8
29	OK	17.0	16.4	19.2	20.2	18.4	18.2
30	OK	15.8	16.6	18.0	17.3	14.2	17.3
31	OK	19.3	16.8	17.4	17.1	17.9	15.4
32	OK	16.3	17.7	16.2	18.4	19.6	15.4
33	OK	18.1	14.1	18.1	17.7	16.1	16.9
34	OK	13.8	18.0	15.0	15.6	19.3	16.3
35	failed&fixed	16.7	16.1	18.6	23.1	16.9	15.1
36	OK	15.2	14.7	14.1	17.4	17.5	15.1
37	OK	19.8	16.3	16.3	15.6	15.6	15.6
38	OK	14.8	18.1	14.4	16.0	15.4	13.9
39	OK	16.1	17.8	17.3	18.7	15.0	15.7
40	OK	19.3	16.5	19.3	20.3	18.4	14.7
41	OK	17.8	16.7	15.6	15.9	14.6	16.1
43	OK	18.3	17.2	20.2	22.0	21.0	19.2
44	no. not used						
45	bad PCB						
46	OK	15.3	19.1	15.0	24.1	20.1	21.6

Table VI: The bench test results for the TOFr FEE cards. The columns are standard deviations (*i.e.* the resolution) in units of picoseconds. These TOFr FEE cards are very similar to cards proposed for the full system called TFEE.

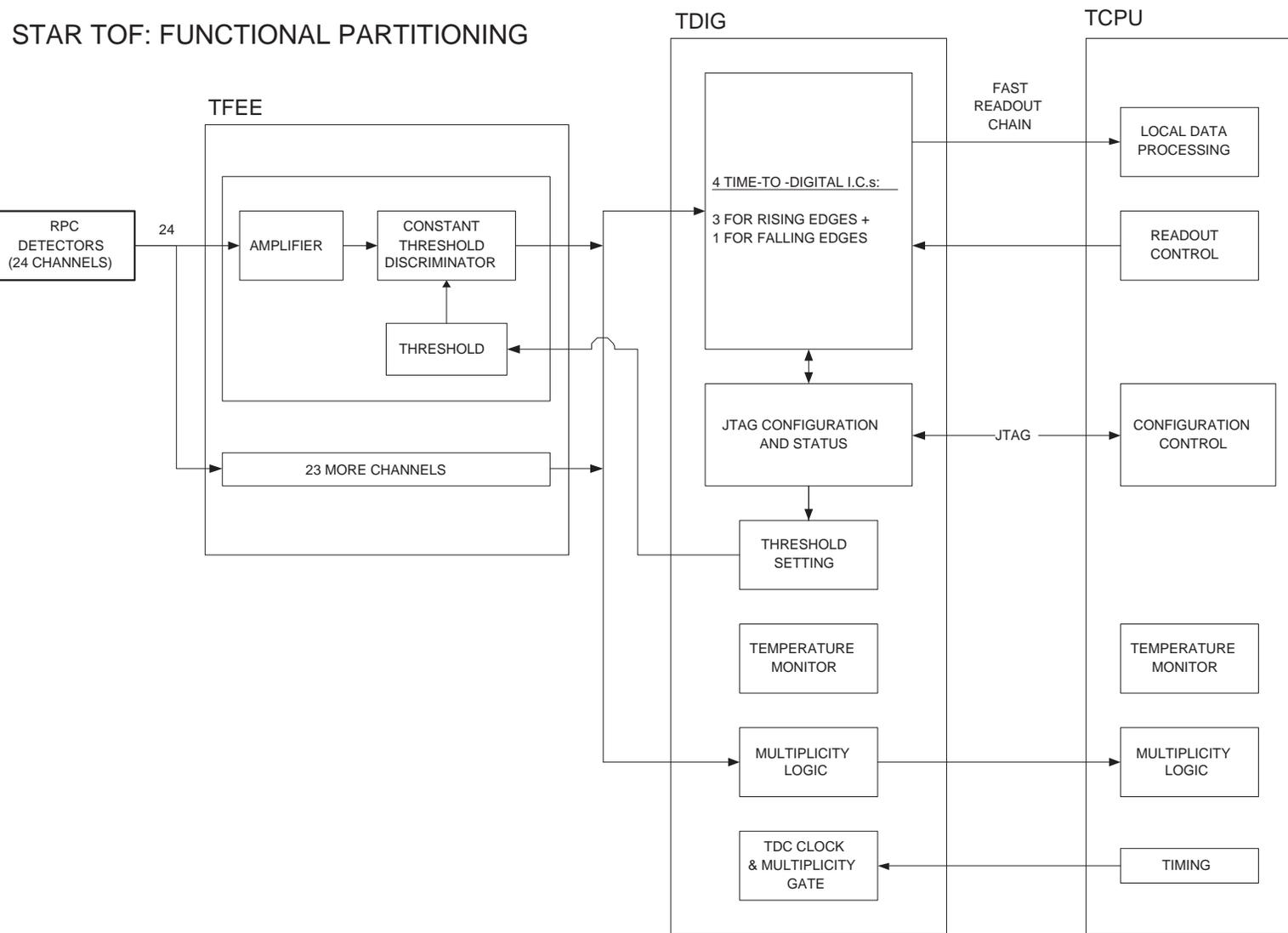


Figure 35: The front end electronics (TFEF) and digital sampling (TDIG) circuit cards.

built a prototype TDIG circuit using the HPTDC. The HPTDCs have been bench tested at CERN and have successfully demonstrated 15 ps timing resolution. The high-resolution mode of the HPTDC is available now in a CAEN VME-based TDC module offering 25 ps resolution (LSB).

4.6.3 TTST

The purpose of this card is to serve as an interface to allow convenient testing of the completed trays (MRPC modules plus TFEE) without having to communicate with the full STAR DAQ to get the data out. This board has the same footprint as TDIG and plugs into TFEE in the same way as TDIG. The TTST board contains NIM signal level conditioning circuits to make the TFEE preamp and discriminator outputs compatible with CAMAC TDC & ADC modules. The combination of TFEE and TTST has exactly the same electronic functionality as the TOFr FEE boards (see sections 4.6.1 and 5). Only a few of the TTST boards are needed at each location in the project where fully-assembled trays are being tested.

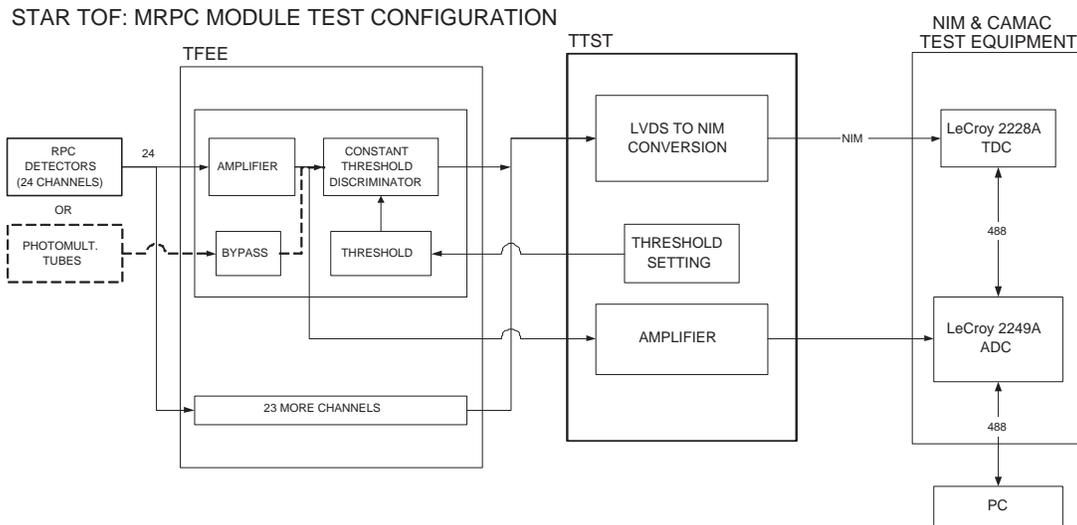


Figure 36: The functional diagram of the construction test electronics chain TFEE to TTST to CAMAC.

4.6.4 TCPU

The TCPU circuit card functions as a data concentrator and interface between the external experimental environment and the STAR TOF data acquisition electronics (TFEE and TDIG). The TCPU is implemented as a combination of embedded CPU and programmable logic. The TCPU functions at the detector tray level, and our design has one TCPU per tray. The TCPU concentrates data from 192 detector channels.

The TCPU performs the following functions (see Figure 37):

- **Multiplicity** – Once per beam crossing, the 8 TDIG cards in a tray each provide multiplicity data as a 5-bit value representing from 0 to 24 hits. From these data, the TCPU computes 2 multiplicity sums, each the sum of 4 TDIG inputs, or 96 channels. Each half-tray multiplicity sum is sent to the STAR Level 0 trigger as 7 differential signal pairs, using either PECL or LVDS drivers.
- **TDC readout** – The TCPU will provide readout signals to the 32 TDCs in the tray. It will receive data from the TDCs, buffer the data, format the data, and send it out via the TMIT daughter board. In the process of building data packets from buffered data for transmission via the TMIT board, the TCPU will perform data token management, using tokens received via trigger commands.
- **System configuration** – Prior to data acquisition, the TCPU configures the TDCs, sets the discriminator thresholds, and initializes the trigger command processing and high speed data transmission blocks. Configuration parameters are loaded from on-board EEPROM storage or read from a host PC over the host serial bus. The TCPU sends configuration data to the TDCs over a JTAG daisy chain. The threshold DAC configuration data travels over a separate 2-wire communication path.
- **System status** – System status information includes TDC configuration echo via JTAG, threshold DAC echo via the 2-wire communication path, and temperature monitor information via the 2-wire communication path. We will likely implement limited built-in self-test capabilities in the TDIG and TCPU cards. This information will be included in the system status.
- **System timebase conditioning** – The TCPU will receive a system level beam crossing clock from the RHIC V124 modules. It conditions this signal by PLL frequency multiplication and filtering techniques to produce a TDC sampling clock with acceptably low jitter characteristics.
- **Trigger command processing** – The TCPU will receive and process commands from the trigger. It will also simply pass some commands such as Abort and L2 Accept on to DAQ via the TMIT card.

4.6.5 TMIT

The TMIT takes formatted data from the data/command buffer, serializes it and transmits it over a fiber optic link to the TDRC. The TMIT will be implemented as a PLD (or a communications chip specific to the communications protocol) and an optical transmitter.

4.6.6 TDRC

The TOF data acquisition (DAQ) system, represented by the TDRC block in the preceding figures, has to receive the digitized data from 120 trays and the start

STAR TOF: TCPU FUNCTIONS

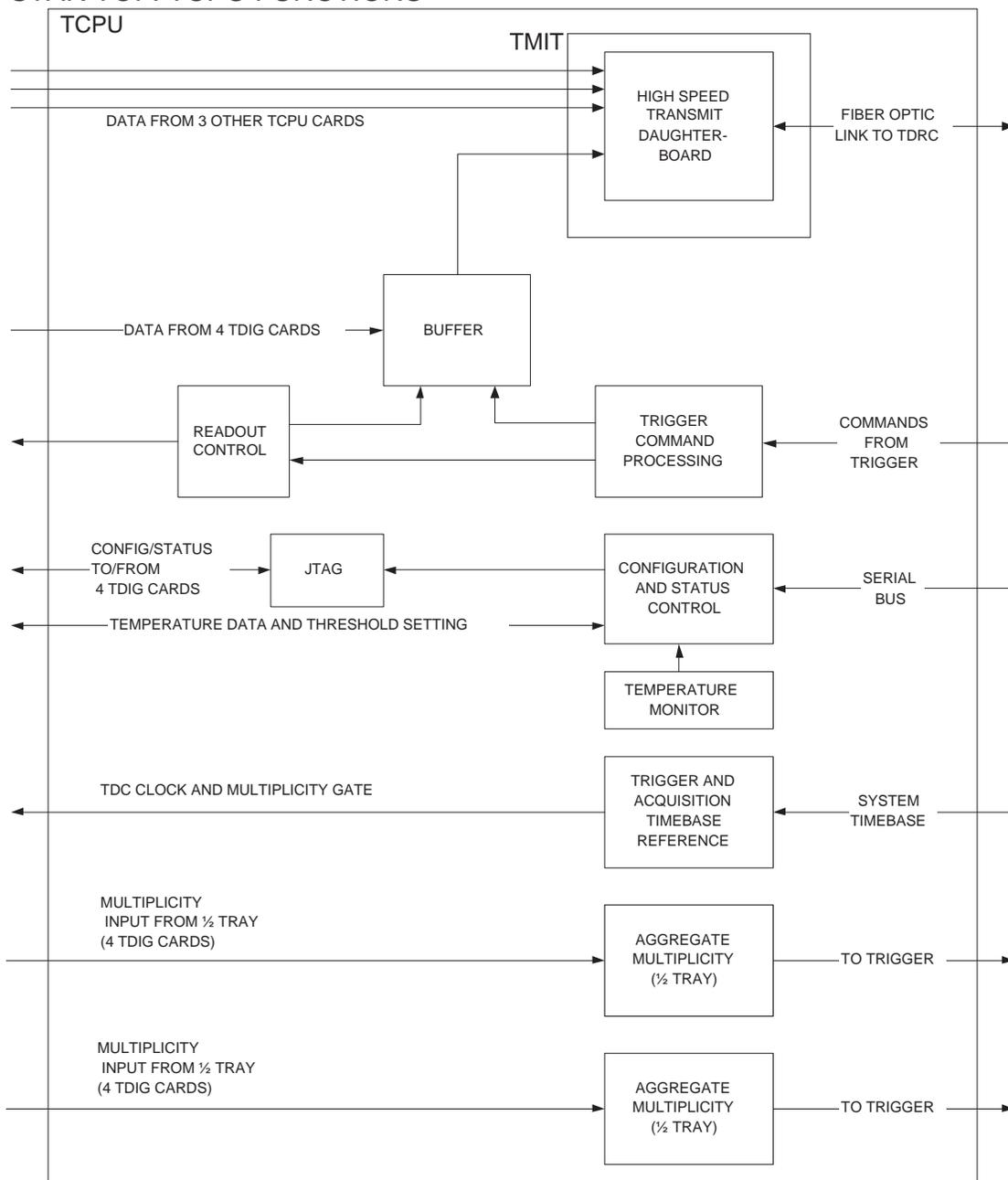


Figure 37: The tray level CPU (TCPU) and high speed data transmit (TMIT) circuit cards.

detectors via optical fiber and present it to the rest of the STAR DAQ system. The data from TOF is provided by 4 fiber links, each carrying the data from 30 trays collected by THUB. The data from TOF to the Level-2 trigger system will be sent over the same fiber to the same receiver.

While most of STAR DAQ is currently implemented in VME, future development

of the STAR DAQ system will be moving into PC based systems running Linux. These systems are ideally suited for the TOF DAQ system as well, so the data needs to be received by an interface that can plug into a PC. Every modern PC has a PCI extension bus, so the most logical choice of a DAQ receiver would be implemented as a fiber receiver that plugs into the PCI bus (or its future extensions like PCI-X).

The CERN experiment ALICE has developed such a system to use in its DAQ system. This system consists of a set of cards that provide the optical link called the Detector Data Link (DDL), one of which is housed on the detector side, the other in the DAQ computer, and a PCI interface card to connect the DDL card to the PCI bus called the Read-Out Receiver Card. (RORC).

The DDL system consists of 2 kinds of cards: the (Source Interface Unit) (SIU) which interfaces to the front-end electronics in the case of ALICE, and the Destination Interface Unit (DIU), which connects to the DAQ front-end processors. Initially, these two cards were implemented as two distinct physical cards, but in their latest implementation in ALICE, these are now the same cards with different firmware running in their programmable logic devices. The two DDL interface units are connected through two multi-mode optical fibers running at 2.5GB/s, so the connection is bi-directional. The DIU is connected to a PCI based RORC in the DAQ computers. The RORC receives data from the detector via the SIU-DIU connection, and provides it to the PC via the PCI bus. At the same time, the RORC can also provide commands to the detector as well as get status information from the detector via the downlink of the fiber connection. The theoretical limit of the 32bit/33MHz version of the PCI bus is 132MB/s, while using the 64bit/66MHz version of PCI one could in principle achieve 528MB/s. The cooperation between the RORC firmware and the PC software allows autonomous data transfer into the PC memory with little CPU assistance. The ALICE DAQ interface is described in [147].

For the PC, we have chosen a dual Intel Xeon system based on a motherboard with 6 PCI-X slots to provide sufficient slots for all four RORCs needed in the TOF DAQ as well as a network card to interface this PC to the rest of STAR DAQ. Currently, the network of choice in STAR DAQ is Myrinet, which exists as an implementation in a PCI-X extension card.

4.7 Power Systems

Low voltage supplies on the STAR platforms are needed to power the on-detector electronics which require roughly +4.5V and -8.5V. High voltage of ± 8 kV is needed to power each MRPC detector. We will evaluate high-channel-density commercial supplies to fill these two roles.

We have used a CAEN SY127 control unit with A631 power modules to provide the high voltage to the TOF prototype trays in the last two RHIC runs (3 and 4). We are comfortable with the performance of this unit and plan to use it in the final system.

4.8 Test & Monitoring Software

A small-scale DAQ system has been developed for MRPC testing. The digitization is done using CAMAC TDC and ADC modules. To allow flexibility and possibly further test automation a GPIB-based CAMAC controller was used in these test experiments. Object oriented DAQ software, already successfully used in earlier TOFp tests, allows for optimum flexibility in introducing new or adding additional CAMAC modules, controllers, or online analysis software modules. The CERN HBOOK functionality is wrapped in the C++ code such that the output files are written in the standard ntuple format and therefore directly analyzable on any platform at any institution.

For the AGS tests of the TOFr prototype (discussed in section 5 below), additional scripting software allowed the operation of this DAQ in a daemon-like fashion. The software ran extremely reliably and has collected many millions of test beam events so far.

The main purpose of the online software for this system will be monitoring and control. The STAR Slow Controls system is now mature and well-understood and most if not all operational parameters will be set and monitored through this system. Typically the operations include monitoring of temperatures, controlling and monitoring the high voltage and low voltage, monitoring the comparator thresholds, reading/setting the TDC configuration, and monitoring the parameters of the gas system. Including these parameters in STAR Slow Controls system also means that they are automatically added to the online database. This will be helpful in advanced stages of the data analysis to correct for long term drift such as that related to electronics temperatures or from the gas system parameters.

4.9 Start Detector Design

In this section, we present comments on the current start detector, the pVPD, and discuss the advantages of an upgrade to this detector. This detector is described in detail in Ref. [4]. This detector was constructed and commissioned within the contingency of the STAR TOFp construction funding. Its purpose is to provide copies of the raw PMT signals and high-resolution discriminator logic signals to be used in NIM electronics on the platform as the the electronic start for the TOFp and pVPD digitization. The pVPD was installed in STAR in Spring 2001 and ran throughout RHIC Runs 2, 3, and 4. This detector subsystem of STAR TOFp consists of two identical assemblies of three magnetically-shielded Pb+Scintillator+PMT+Linear Base detectors in the “flashlight” design. These detector assemblies are mounted very close to the beam pipe at a STAR $|Z|$ position of ~ 5 m; one on the East and one on the West. The front-end electronics are single boards of the same TOFp FEE as are used inside the TOFp tray.

In RHIC Run-2’s full-energy Au+Au collisions, we observed that the pVPD is practically 100% efficient for all but perhaps the most peripheral 5% of the (ZDC/CTB triggered) STAR-standard minimum bias events. (The zero degree calorimeter, ZDC, is detects remnant neutrons at zero degrees.) Another observation was that the pVPD

fired in $\sim 60\%$ of the BBC triggered STAR events taken in Run-2 p+p running. (The beam-beam counter, BBC, coincidence is the minimum bias trigger in p+p running.) After the ZDC, the pVPD is the most forward detector in STAR. There are areas of common acceptance between the pVPD detectors and a few of the most-inner BBC detectors.

In the Au+Au data from that run, we observed sub-50 ps timing resolution of the pVPD. This was achieved by running the pVPD “hot,” meaning we ran the pVPD PMT high voltage to the largest possible values for which the pulse area distributions were still $>90\%$ on-scale for the LeCroy 2249A ADCs and 8 dB attenuators at each pVPD ADC input. In the Au+Au data, there are numerous hits in each detector channel from very energetic photons which convert in the Pb layer resulting in a large number of prompt photoelectrons. The result is an excellent start time resolution. For the p+p running, the 8 dB attenuators were removed from the TOFp ADC inputs and the pVPD PMT gains were increased by approximately a factor of nine (9) above that used (with ADC attenuators) during the Au+Au running. The data from the p+p run indicate that, when a pVPD channel fires, it is firing on a single particle. The probability that one detector on the east fired and one detector on the west fired in the p+p part of RHIC Run-2 was approximately 12%.

There are immutable penalties to the start time resolution when comparing the operation of such a “small-area” start detector in p+p or d+Au to that in Au+Au. The fact that p+p or d+Au data means single particle start timing in detectors of this size implies a relatively low number of photoelectrons and hence the intrinsic resolution of the detectors are worse compared to Au+Au (which has many 10’s of prompt hits per detector channel per event). Also, the sparse number of final state particles in p+p and d+Au data implies that only rarely can one use the average times of many start detectors in the same event in order to further improve the total start time resolution beyond the intrinsic single channel timing resolution.

The requirements on the performance of the start detector for the proposed large-area TOF system in full energy Au+Au collisions are minimal. In Au+Au with many tens of square meters of TOF coverage, there are many TPC tracks matched to TOF channels. In this case, the start time can be inferred event by event from the stop times with nearly arbitrary precision. According to simulations performed for the TOFp proposal [3], one only needs ~ 10 TPC \rightarrow TOF track matches to be able to infer the event start time solely from the stop times with a resolution of ~ 40 ps. This is sufficient to meet the physics requirements for the whole system (start plus stop plus corrections).

However, for p+p, d+Au, and peripheral light-ion collisions, an increase of the acceptance of the start detector would have a significant positive impact on the system as a whole. Obviously the efficiency per event improves. The resolution of the start detector adds in quadrature to the stop resolution of the large area TOF system. An increased acceptance on the start side also enables multiple independent measurements of the prompt particles in the same event, improving the start resolution. This makes some aspects of the offline analysis, which involves a number of corrections independent of those related to the start detector, easier. Initiating an analysis with an

intrinsically high-resolution start time in a “large” acceptance reduces the magnitude and uncertainty in all other corrections. Examples of stop corrections made considerably easier by better start timing are the hit position correction and the slewing correction.

The pVPD upgrade would involve:

- replacing the 3+3 pVPD shielded PMT assemblies with approximately 20+20 unshielded mesh-dynode PMT assemblies. This number of unshielded mesh-dynode PMTs fits easily into the same volume occupied by the present pVPD. As almost all of weight of the pVPD is in the six steel plus μ -metal shield assemblies, the upgraded detector as a whole may be lighter than the present pVPD despite the increased channel count.
- replacing the FEE and CAMAC digitization with the same electronics being developed for the stop side in this proposal (see 4.6). The only modification in the electronics chains on the start and stop sides is in the use of the TPMT board instead of TAMP just after the detectors.
- building two new small light-weight aluminum and Delrin mounting assemblies. Since magnetic shielding is unnecessary for the mesh-dynode PMTs, there are no longer magnetic forces on the mounting structure, which simplifies the design.

The upgraded pVPD would occupy the same integration volume as the present pVPD, which is close to the beam pipe near $|Z| \sim 5$ m. This volume does not conflict with the PMD, FPD, and BBC detectors in the vicinity. With the pVPD’s magnetic shields gone, the largest source of backgrounds in other detectors from particle interactions in the pVPD is removed. The same FEE plus digitization plus communication electronics chain that is presently proposed for the stop side will be used for this upgraded system. The start side, like the stop side, will be digitized on-detector versus a common clock, and digital data is transmitted off the detector. The economy of using the same basic electronics design for both the start and stop sides of this system requires that the TAMP boards (see section 4.6.1) be modified to include input protection and to accept PMT inputs. This modified board is called TPMT.

The PMTs could be obtained in principle from the STAR CTB, which will have to be decommissioned to make way for the proposed system. However, these PMTs have been damaged by large LED pulses and they afterpulse, a typical problem for Hamamatsu mesh-dynode PMTs as they age. If the TOFp system were decommissioned in the Summer of 2004, there would exist ~ 40 more mesh dynode PMTs which will have higher gains and better resolution than the CTB PMTs (but which may also afterpulse by then). A possible approach would be to decommission both TOFp and the CTB in stages as final TOF trays begin to appear, and then take the best ~ 50 PMTs available. The cost estimate for the pVPD upgrade includes the purchase of new Hamamatsu R5946 PMTs which would be installed when the construction of the TOF barrel is nearly complete.

Twenty detector channels per upgraded PVPD detector is well-matched to the 24 channel TPMT boards. There would be a single TPMT board and a single TDIG

board mounted close to the upgraded pVPD detectors, one on each side of STAR. Power to the PMTs would be provided by a standard LeCroy 1440 mainframe available from HEEP.

This upgraded pVPD system, with a high channel count and crossing-by-crossing clocking of the start timing information, will provide multiplicity information to the STAR Level 0 trigger in the same way as the TOF barrel. Providing Level 0 with the primary vertex location via east/west timing differences event by event requires further design but appears to be feasible using the electronics model described in section 4.6.

radiated into the gas volume by about a factor of 8.

Water flow is used for heat removal from the on-board electronics in both TOFp and TOFr'. Included in the design of TOFr5 is a new type of cooling water path based on 1/4" square copper tubing that makes direct thermal contact with both TAMP and TDIG via thermally conductive shims along the full length of the tray. This method is expected to more efficiently remove heat from the main power source (TDIG) than would air flow across these electronics.