

```

1  -- *****
2  -- LIBRARY DEFINITIONS
3  -- *****
4
5  LIBRARY altera; USE altera_maxplus2.all;
6  LIBRARY ieee; USE ieee_std_logic_1164.all;
7  LIBRARY lpm; USE lpm_lpm_components.all;
8
9  -- *****
10 -- TOP LEVEL ENTITY
11 -- *****
12
13 -- Note mux is hardwired to come from J23
14
15 entity smalla is port (
16     gclk1 : in std_logic;    -- clock from clock muxes
17     gclk2 : in std_logic;    -- clock directly from oscillator
18
19     -- watchdog timers
20     -- watchdog1 (U11) receives a pulse from U8 (pld clock)
21     -- watchdog2 (U25) receives a pulse from the MCU
22
23     wd1_rsout : in std_logic; -- power on reset signal from watchdog1
24     wd2_rsout : in std_logic; -- power on reset signal from watchdog2
25
26     wd1_out : in std_logic;   -- "no pulse" signal from watchdog1
27     wd2_out : in std_logic;   -- "no pulse" signal from watchdog2
28
29
30     mcu_reset : out std_logic; -- reset output to MCU (based on watchdog)
31     -- ACTIVE LOW, default is HI
32     -- goes to U21/pin9 "NMCLR" pin
33
34     pll_in_sel : in std_logic; -- clock source select signal from mcu pin RC2
35     -- Normally this will map straight thru to "EXT TO PLL",
36     -- and this output will cause
37     -- HI = external osc into PLL
38     -- LO = local osc into PLL
39     -- power on = LO
40     -- default = LO
41
42     mcu_enable_local : in std_logic; -- PIN 8
43     -- clock input select from mcu pin RC1
44     -- Normally this will map straight thru to
45     -- "DISABLE LOCAL OSC"
46     -- HI = disable local clock to U6
47     -- LO = enable local clock to U6
48     -- power on = LO
49     -- default = LO
50
51     ext_to_pll : out std_logic; -- PIN 24
52     -- function of mcu_enable_local and ...
53     -- controls U6 mux
54     -- HI = ext osc is input to U2 PLL
55     -- LO = int osc in from J33/J34 is input to U2 PLL
56
57     disable_local_osc : out std_logic; -- PIN 25 controls tristate output from U14 to U6 mux
58
59     -- HI = disable local clock to U6
60     -- LO = enable local clock to U6
61     -- power on = LO
62     -- default = LO
63     -- operational = LO for slaves and HI for master
64
65     -- Disabling clock is default operational mode for slave TCPUs
66     -- to reduce crosstalk to external clock signal inside U6
67
68     sel_local_to_board : out std_logic; -- PIN 26 SELECT INPUT FOR U4 MUX
69     -- '0' selects PLL for U4 mux
70     -- '1' selects local oscillator from U14
71
72
73     pushbut2 : in std_logic; -- prototyping test input from contact switch SW3
74
75     master : in std_logic; -- signal from large PLD telling whether this board is a master
76
77     clk_20_mhz : out std_logic; -- gclk divided by 2 for MCU clock
78     -- this clock should switch with any switch in the main pld clock
79     -- so that the MCU and the main PLD have synchronous clocks
80
81     hdr_tck : in std_logic; -- large pld jtag signals from header
82     hdr_tdo : out std_logic;
83     hdr_tms : in std_logic;
84     hdr_tdi : in std_logic;
85
86     mcu_tck : in std_logic; -- large pld jtag signals from mcu
87     mcu_tdo : out std_logic;
88     mcu_tms : in std_logic;
89     mcu_tdi : in std_logic;
90
91     cfg_tck : out std_logic; -- output of jtag mux to large pld
92     cfg_tdo : in std_logic;
93     cfg_tms : out std_logic;
94     cfg_tdi : out std_logic );
95
96 end smalla;
97
98 -- *****
99 -- TOP LEVEL ARCHITECTURE
100 -- *****
101
102 architecture version_a of smalla is
103
104 component TFF_LB PORT (
105     clock : IN STD_LOGIC ;
106     scir  : IN STD_LOGIC ;
107     q     : OUT STD_LOGIC );
108 END component;
109
110 component mux_2in_3bit PORT (
111     data1x : IN STD_LOGIC_VECTOR (2 DOWNTO 0);
112     data0x : IN STD_LOGIC_VECTOR (2 DOWNTO 0);
113     sel    : IN STD_LOGIC ;
114     result : OUT STD_LOGIC_VECTOR (2 DOWNTO 0) );
115 end component;
116
117 component mux_2in_1bit PORT (
118     data1 : IN STD_LOGIC ;
119     data0 : IN STD_LOGIC ;
120     sel   : IN STD_LOGIC ;
121     result : OUT STD_LOGIC );
122 end component;
123
124 begin
125     mcu_reset <= wd1_rsout; -- ACTIVE LOW, default is HI
126     -- This statement maps the power on reset output of watchdog1
127     -- to the reset input of the MCU. The watchdog "RSOUT" signal
128     -- is active low.
129
130     -- ***** SIGNAL THAT DETERMINES MASTER / SLAVE CONFIGURATION
131     -- DEFAULT = '0' TO SELECT INTERNAL CLOCK TO PLL
132
133     ext_to_pll <= not master;
134

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```
135 -- HI = ext osc is input to U2 PLL
136 -- LO = int osc in from J33/J34 is input to U2 PLL
137
138 sel_local_to_board <= '0'; -- selects PLL to go thru U4 mux to
139 -- J30, J28, and J27 sysclock cable drivers
140
141 disable_local_osc <= '0'; -- default LO = enable local clock to U6
142
143 -- divide 40 Mhz by 2 for 20 Mhz MCU clock
144
145 div2 : TFF_LB PORT MAP (clock => gc1k1, sclr => wdl_rsout, q => clk_20_mhz);
146
147 -- mux selects between header and MCU as JTAG source for programming large PLD
148 -- 3 signals going to large pld
149
150 jtag_mux_out : mux_2in_3bit PORT MAP (
151     data1x(0) => hdr_tdi,
152     data1x(1) => hdr_tms,
153     data1x(2) => hdr_tck,
154
155     data0x(0) => mcu_tdi,
156     data0x(1) => mcu_tms,
157     data0x(2) => mcu_tck,
158
159     result(0) => cfg_tdi, -- JTAG TDI to large PLD
160     result(1) => cfg_tms, -- JTAG TMS to large PLD
161     result(2) => cfg_tck, -- JTAG TCK to large PLD;
162
163     sel => '1' );
164
165 -- tdo coming back from large pld goes to both header and mcu
166 hdr_tdo <= cfg_tdo;
167 mcu_tdo <= cfg_tdo;
168
169 end architecture version_a;
```