DRAFT

The Development of Large-Area Fast Photo-detectors

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GOAL

The goal of this R&D program is to develop a basic family of large-area economical photo-detectors that can be tailored for a wide variety of uses, much as the basic principles of photomultipliers are used now. Progress in modern micro-electronics, materials science, and nano-technology give us an opportunity to apply micro-channel plate technology to produce large-area economical photo-detectors with good space and time resolution and quantum efficiencies and signal gains similar to those of phototubes. The new devices should be simpler to produce in quantity than photomultipliers, being a sandwich of layers rather than an assembly of discrete parts. The plan of generic R&D that follows is intended to solve the basic technical issues and deliver proto-types that are ready to be commercialized within 3 years and a fixed budget.

Possible applications include large-area particle detectors in high-energy physics, nuclear physics, and astrophysics, medical imaging, and scanners for transportation security, with many possibilities for new products and spin-off technologies. Also because the new devices are thin, planar and physically robust, they will require less volume and infrastructure in large-area applications for which photomultipliers are presently the current solution, providing additional economies and offering new opportunities for uses.

1 Milestones

1.1 Year 1

1. **Select and characterize ALD Materials**

   (a) Understand and verify secondary emission and photo-electric properties of materials: literature search, IP from industry, sample preparation and emission tests at APS and MS
   (b) Identify and characterize the top candidate ALD materials for pores
   (c) Identify and characterize the top candidate ALD materials for photocathodes
   (d) Evaluate the need/use of ALD on other non-metallic surfaces for monolithic assembly and reduced aging.
   (e) Make necessary fixtures and test facilities for applying ALD to $1'' \times 1''$ AAO plates

2. **Select and test the AAO Process**

   (a) Develop and document the AAO process for making pores with diameter $\geq$ 250nm
   (b) Develop and document the AAO process for making funnels suitable for photo-cathode ALD
   (c) Make necessary fixtures and test facilities for making and testing $1'' \times 1''$ AAO plates

3. **Photo-Cathode Development and Selection**

   (a) Understand and verify QE, spectral response, robustness, and assembly requirements of materials: literature search, IP from industry, sample preparation and emission tests at APS and MS
   (b) Identify and characterize (transmission vs λ) window material
   (c) Solve the internal reflection problem with adequate transmission
   (d) Define facilities necessary for photocathode fabrication, assembly
   (e) Make/acquire and test prototype $1'' \times 1''$ panels with photocathode

4. **Simulation**

   (a) Optimize funnel and pore shapes
   (b) Extend simulation to the complete shower and pore exit
   (c) Compare simulation and laser test-stand data for commercial tubes.
   (d) Compare simulation and test data for $1'' \times 1''$ single plate, double plate
   (e) Expand code to simulation of photo-cathode, front and back gaps, anode and charge collection
   (f) Simulate 2-panel stack; optimize interface of the 2 panels
   (g) Interface MCP simulation to MATLAB/SPICE electronics simulation

5. **Make Working $1'' \times 1''$ MCP Prototype Single Panels (test in vacuum chamber- no independent frame)**

   (a) Identify/create/populate a vacuum lab for MCP assembly/testing
   (b) Make and characterize 1" AAO proto-type with suitable L/D, pore size, funnels, uniformity, top and bottom surfaces.
   (c) Develop process for plating top and bottom electrodes
   (d) Test gain, QE, risetime, uniformity, ringing of $1'' \times 1''$ MCP Photo-Cathode Funnel Prototype (ALD/AAO)
   (e) Measure vacuum, characterize residual gases, measure outgassing, aging.

6. **Make Working $1'' \times 1''$ MCP Prototype Double Panels (test in vacuum chamber- no independent frame)**

   (a) Design mechanical assembly and necessary fixturing/tools
   (b) Test gain, QE, risetime, uniformity, ringing, ion feedback

7. **Ready Facilities and Processes for $2'' \times 8''$ MCP Module Prototype (module implies frame, PC, anode)**
   (a) Make necessary fixtures and test facilities for applying ALD to $2'' \times 8''$ AAO plates
   (b) Make necessary fixtures and test facilities for making and testing $2'' \times 8''$ MCP panels
   (c) Make necessary fixtures and test facilities for photo-cathode application and tests
8. **Design and Test Mechanical Assembly/Windows/Vacuum for the $2'' \times 8''$ Module Prototype**
   (a) Design and construct the necessary vacuum chambers/equipment for assembly of $2'' \times 8''$ modules
   (b) Select materials, design, and test seals for layers in the module
   (c) Decide on whether or not we need a getter, bake-out procedures, vacuum access
   (d) Complete the preliminary mechanical design for the $2'' \times 8''$ module
9. **Anodes and Transmission Lines for the $2'' \times 8''$ Module Prototype**
   (a) Select material and process for transmission-line anode
   (b) Fabricate transmission-line anode for $1'' \times 1''$ prototype
   (c) Measure velocity, dispersion for anode for $1'' \times 1''$ prototype
   (d) Fabricate and test transmission-line anode for $2'' \times 8''$ prototype
   (e) Solve signal connection from anode to front-end chip problem.
10. **Electronics and Readout (items c-h NSF supported at UC, hopefully)**
   (a) Design first-generation clock distribution for $2'' \times 8''$ unit
   (b) Design first-generation FPGA DAQ/control card for $2'' \times 8''$ unit
   (c) Fabricate $2'' \times 8''$ PC card with LAB3 or BLAB3 Hawaii chip and Photonis MCP
   (d) Test $2'' \times 8''$ PC card with LAB3 or BLAB3 Hawaii chip and Photonis MCP
   (e) Get all tools for 130nm IBM process
   (f) Design and layout timing block for 130nm chip
   (g) With Orsay, Hawaii (advice/review from PSI and Saclay), settle on design and layout for capacitor block for 130nm chip
   (h) Submit first IBM-8RF chip with test timing and capacitor chain blocks
11. **Management and Review**
   (a) Select Project Director, Deputy Director, Project Engineer, 1/2-FTE Assistant
   (b) Select Internal Biannual Review Committee and schedule reviews
   (c) Establish Risk Assessment Methodology
   (d) Establish Major Decision Points on Photo-cathode Geometry, Module Size and Assembly, and Cost, and 'Plan-B' Methodology
   (e) Survey and clarify IP and future production relationships with industry
   (f) Establish reporting/review/deliverables schedule with DOE

1.2 Year 2

1. **Second Generation ALD Materials: Higher QE, nano-structures, wavelength tuning**
   (a) Continue to identify and test ALD materials for pores
   (b) Continue to identify and test the top candidate ALD materials for photocathodes
   (c) Explore ring dynode structures in the pores (ANL patent on stripes)
2. **Second Generation AAO Process: $8'' \times 8''$ Panels and Batch Production**
   (a) Develop the AAO process and facilities for making $8'' \times 8''$ panels

(b) Develop a design for batch production of $8'' \times 8''$ panels
(c) Explore advanced processes and pore geometries for cheaper production and higher QE

3. **Continue Development with $1'' \times 1''$ MCP Prototypes**

   (a) Continue the program of assembling and characterizing $1'' \times 1''$ AAO/ALD proto-types

4. **Production of the $2'' \times 8''$ MCP Prototype**

   (a) Fabricate, instrument, and test multiple $2'' \times 8''$ units
   (b) If warranted, move advanced $1'' \times 1''$ technology to $2'' \times 8''$
   (c) Measure vacuum, characterize residual gases, measure outgassing, aging.

5. **Design and Test Mechanical Assembly/Windows/Vacuum for the $2'' \times 8''$ MCP Prototype and the $2' \times 2'$ Module**

   (a) Design and fabricate a 2-panel 'stack' for the $8'' \times 8''$ prototype
   (b) Test uniformity, TTS, wave-form shapes for 2-panel $8'' \times 8''$ 'stack'
   (c) Design and fabricate a prototype $2' \times 2'$ module (9 $8'' \times 8''$ panels in a $2' \times 2'$ module)
   (d) Design assembly and test facilites for the $2' \times 2'$ module
   (e) Continue program on advanced materials, design, and test seals for layers in the module

6. **Anodes and Transmission Lines**

   (a) Fabricate and test transmission-line anode for the $8'' \times 8''$ prototype
   (b) Fabricate and test transmission-line anode for the $2' \times 2'$ prototype module

7. **Electronics and Readout (items c-d NSF supported at UC, hopefully**

   (a) Design first-generation clock distribution for $2' \times 2'$ module
   (b) Design first-generation FPGA DAQ/control card for $2' \times 2'$ module
   (c) Test $2'' \times 8''$ PC card with LAB3 or BLAB3 Hawaii chip and $2'' \times 8''$ ALD/AAO unit
   (d) Submit second IBM-8RF chip with critical test blocks

8. **Simulation**

   (a) Continue to use code to optimize funnel and pore shapes for $1'' \times 1''$ unit.
   (b) Compare simulation and data for $8'' \times 8''$ unit.
   (c) Expand code to full 'end-to-end' simulation for charged particles, photons

9. **Management and Review**

   (a) Get Another Program Director

1.3 Year 3

1. **Second Generation ALD Materials: Higher QE, nano-structures, wavelength tuning**

   (a) Continue to identify and test ALD materials for pores
   (b) Continue to identify and test the top candidate ALD materials for photocathodes
   (c) Continue to identify and test ALD materials for module interior surfaces
   (d) Start program for industrialization: cost, facilities, throughput

2. **Second Generation AAO Process: $8'' \times 8''$ Panels and Batch Production**

   (a) Continue Explore advanced processes and pore geometries for cheaper production and higher QE

(b) Start program for industrialization: cost, facilities, throughput

3. **Continue Development with $1'' \times 1''$ MCP Prototypes**

   (a) Continue the program of assembling and characterizing $1'' \times 1''$ and $8'' \times 8''$ AAO/ALD prototypes

4. **Production of the $8'' \times 8''$ MCP Panels (9 panels per $2' \times 2'$ module)**

   (a) Fabricate, instrument, and test multiple $8'' \times 8''$ units
   (b) Test multiple $8'' \times 8''$ units in the Fermilab MTEST beam.
   (c) If warranted, move advanced $1'' \times 1''$ technology to $2'' \times 8''$
   (d) Measure vacuum, characterize residual gases, measure outgassing, aging.

5. **Production and Testing for the $2' \times 2'$ Module**

   (a) Produce several Pre-production Prototypes of the $2' \times 2'$ module (9 $8'' \times 8''$ panels in a $2' \times 2'$ module)
   (b) Test several Pre-production Prototypes of the $2' \times 2'$ module (9 $8'' \times 8''$ panels in a $2' \times 2'$ module)
   (c) Pressure test several Pre-production Prototypes of the $2' \times 2'$ module (9 $8'' \times 8''$ panels in a $2' \times 2'$ module)
   (d) Measure vacuum, characterize residual gases, measure outgassing, aging.
   (e) Continue program on advanced materials, design, and test seals for module layers

6. **Anodes and Transmission Lines**

   (a) Fabricate and test production transmission-line anodes for the $2' \times 2'$ module

7. **Electronics and Readout (items c-d NSF supported at UC, hopefully**

   (a) Design production generation clock distribution for $2' \times 2'$ module
   (b) Design production FPGA DAQ/control card for $2' \times 2'$ module
   (c) Submit third IBM-8RF chip
   (d) Assemble a 4-module system (8 square feet).
   (e) Test 4-module system

8. **Simulation**

   (a) Continue to use code to optimize funnel and pore shapes for $1'' \times 1''$ unit.
   (b) Compare simulation and data for $2' \times 2'$ unit.
   (c) Continue to expand code to user-friendly 'end-to-end' simulation for charged particles, photons in specific applications (PET, DUSEL, LHC, security).

9. **Management and Review**

   (a) Establish production handoff of $2' \times 2'$ unit to industry
   (b) Establish paths to application-specific modifications of the generic device for Medical Imaging, Transportation Security neutron and photon scanners, sub-picosecond particle timing, and other applications.

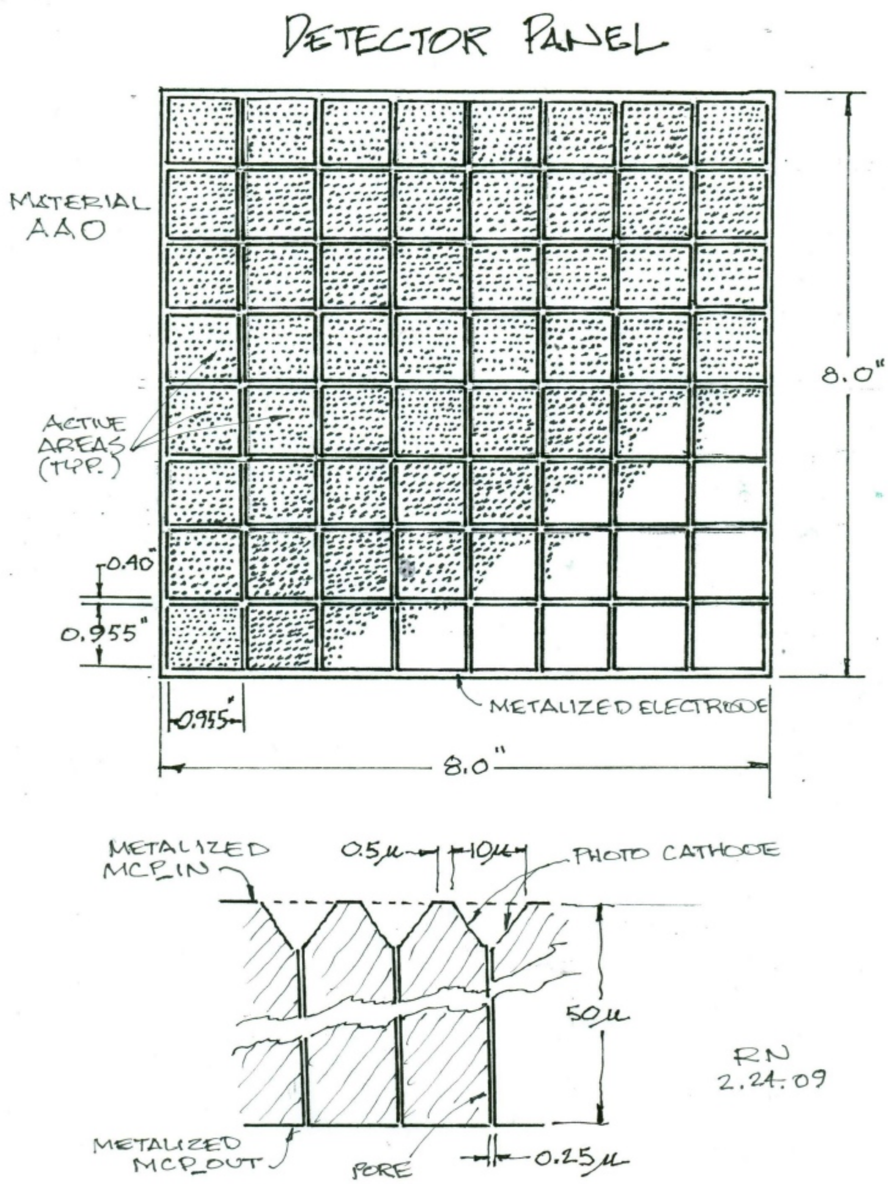

Figure 1: A sketch of the 8″ × 8″ MCP panel. This is constructed using AAO to activate (make pores) of 1″ × 1″ inch squares separated by a thin matrix of the aluminum sheet that has no pores. The top and bottom surface form electrodes across which there is approximately 1 KV. The stack of spacers and the two MCP planes has this matrix structure, with the spacers aligned with the inactive separating membranes, providing a very strong structure. The inset shows a side view, showing the 'funnel' entrance to the pores, on which the photocathode is deposited.

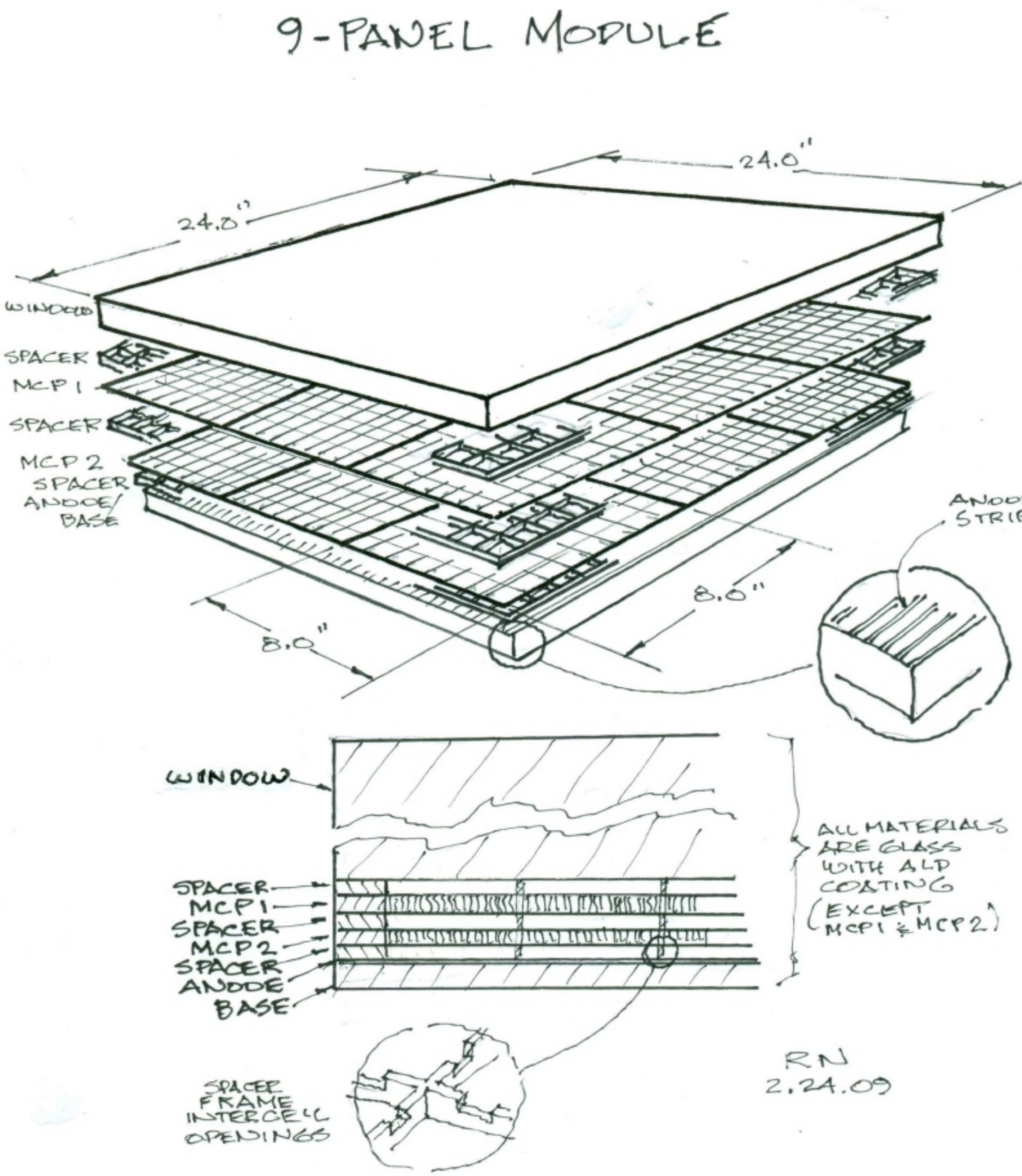

Figure 2: A sketch of the $2' \times 2'$ module, which consists of 9 $8'' \times 8''$ panels in a 3×3 array, sharing a common vacuum, window, and transmission line readout.