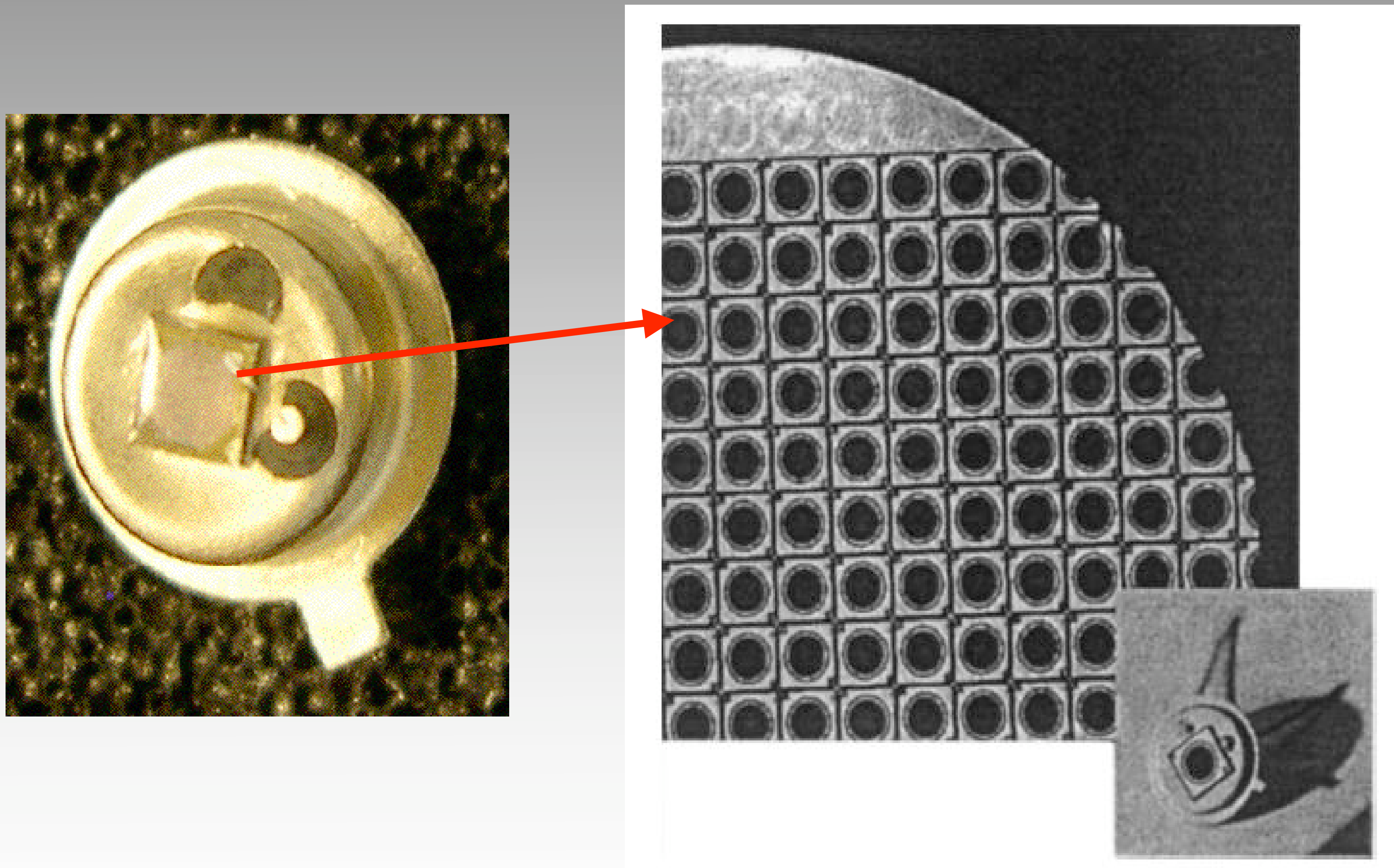
GM-APD arrays for PET detectors

Tom Lewellen, 2009

Silicon Photomultipliers
(Geiger-mode APDs)



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A few general thoughts

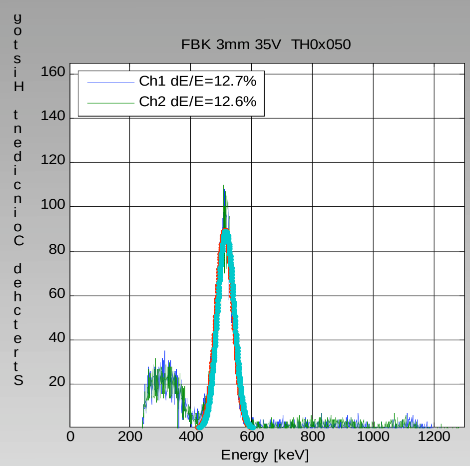
- GM-APD performance is still a moving target
- The potential cost advantage over PMTs has yet to be achieved
  - » Most arrays require manual placement of GM-APD “elements” cut from a wafer
  - » Only monolithic array with good performance shown so far is a 2x2 with 1x1 mm elements
- Not just a replacement for PMTs - the electrical characteristics are different
- But the potential of fine pitch arrays, one-on-one coupling, ability to work in magnetic fields, fast timing, make them very interesting indeed.

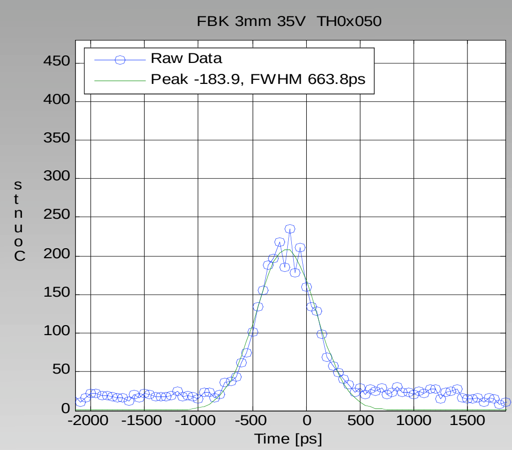
Some device parameters - works in progress

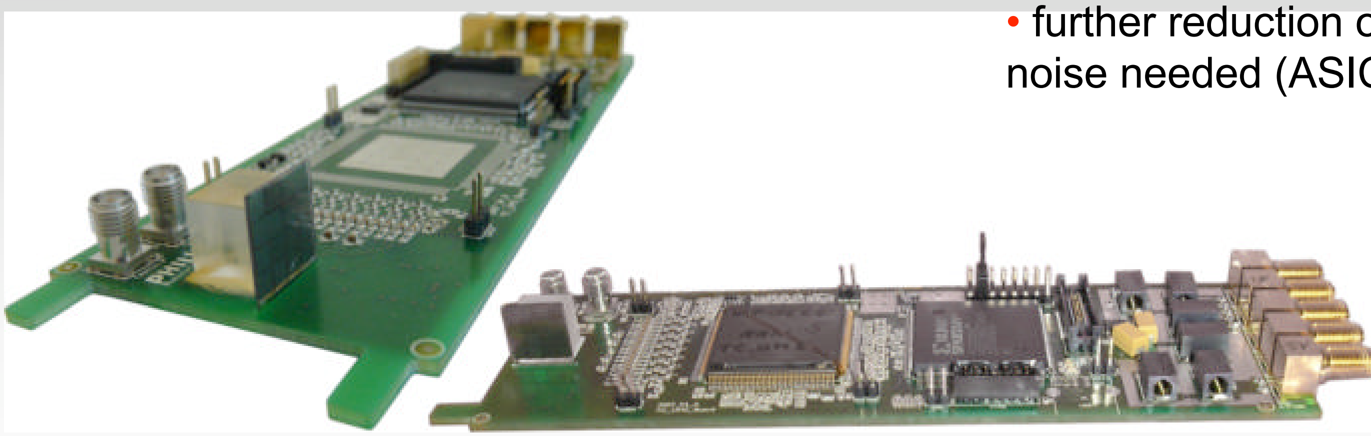
Source / Property	A	B	C	D	E
Cell Size (u)	25, 50, 100	35	50	10	
Pixel Size (mm)	1, 3	3	3.5	3	2
Nb. of cell	400, 3600	7300	4900	90,000	
Fill Factor (%)			36 %		
Timing Res.	270 ps, 1mm 320 ps 3mm	800 ps	460ps	850ps	600 ps
E Res (% FWHM)	20%, 1mm 15%, 3mm	15 %	15 %	25 %	17 %
Dark counts per pixel / per cell	0.5 M ~ 300	> 10 M	> 10 M		~ 10 M
QE @ 420nm	70 % min.	20% now 50% end 07	35 %	75%	
V breakdown	70 +/- 10	30 +/- 10	30 +/- 10	130 +/- 10	

The point is that they vary a lot between vendors, and different versions from the same vendor

From EU PET-MR project web site
FBK SiPM device, Philips ASIC







Measurements:

- crt=660ps @ 35V and 25°C
- crt=600ps @ 36V and 25°C
- crt=500ps @ -10°C

(ref.TDC/QDC w. preamp crt=430ps, 25°C)

Findings:

- further reduction of dark count rate needed (SiPM)
- further reduction of preamp noise needed (ASIC)

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Best the UW group has done

Zecotek Photonics Type N device

Single element

$3x3\ mm^2$

15000 pixels/mm

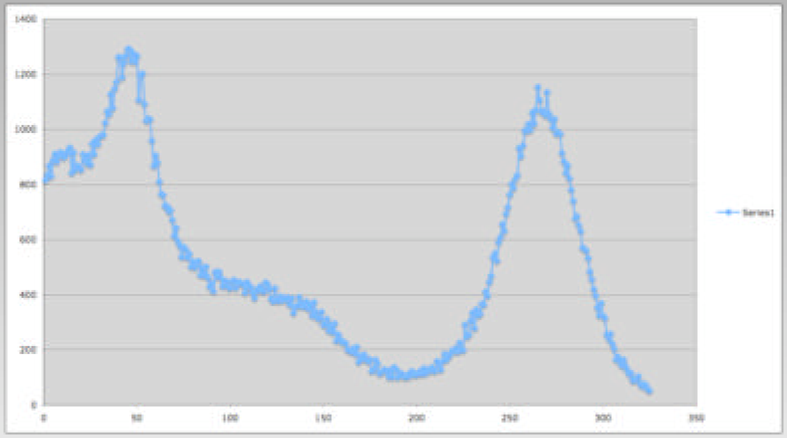
Gain ~ 10^5

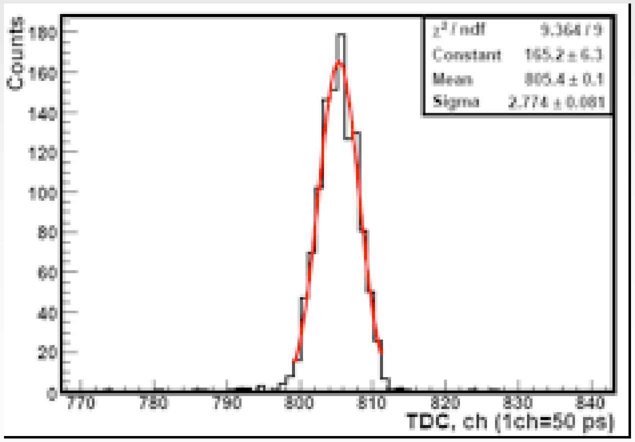
PDE ~ 25%

E res   13%

T res   325 ps (coinc)

Data from 3x3x10 mm LFS-3





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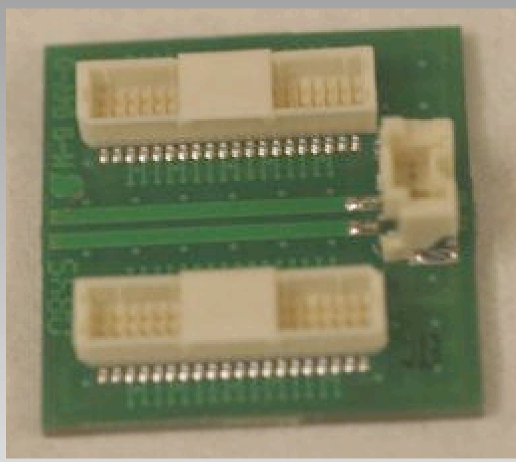
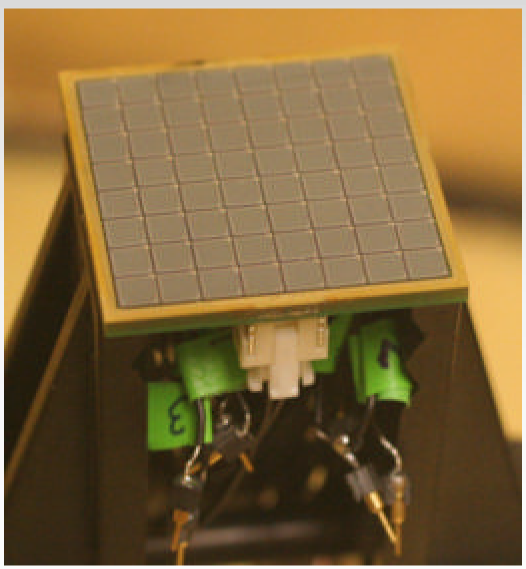
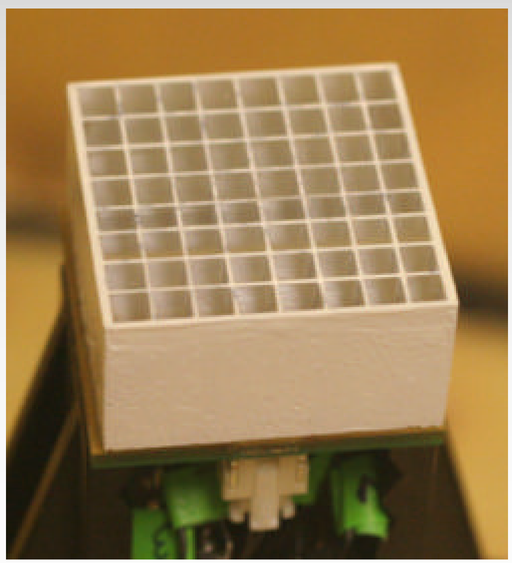
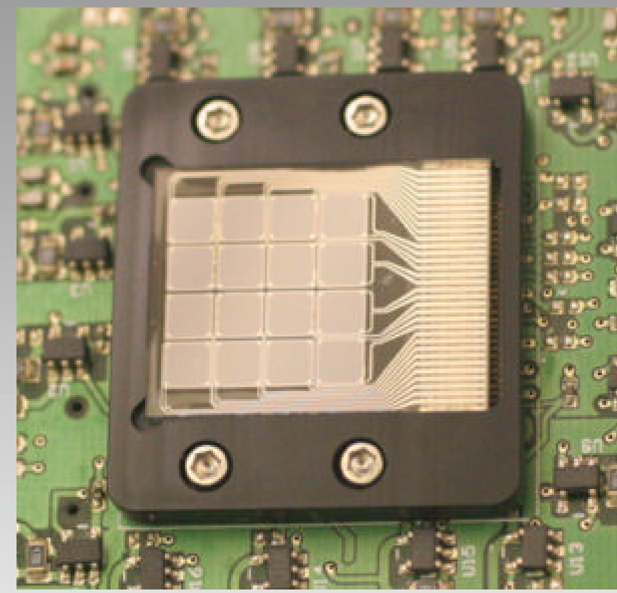
GM-APDs Arrays at the UW



Zecotek Photonics Type 3-N 8x8 array with 3.3 mm square elements



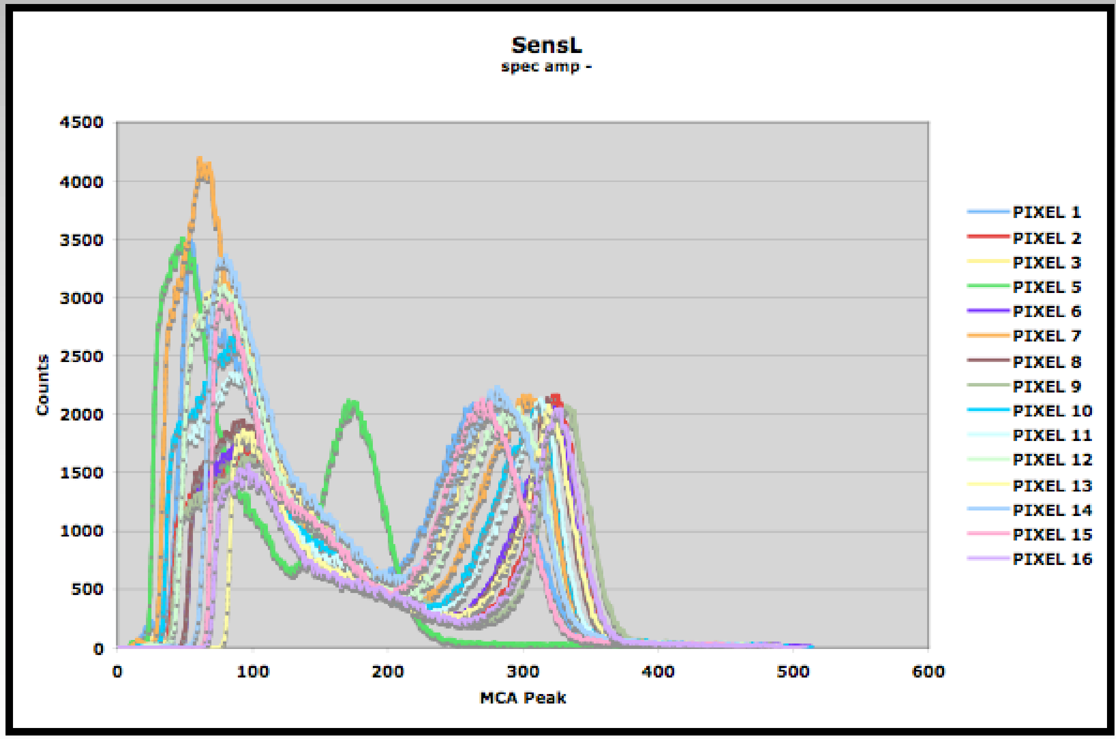




SensL 4x4 array with 3 mm square elements

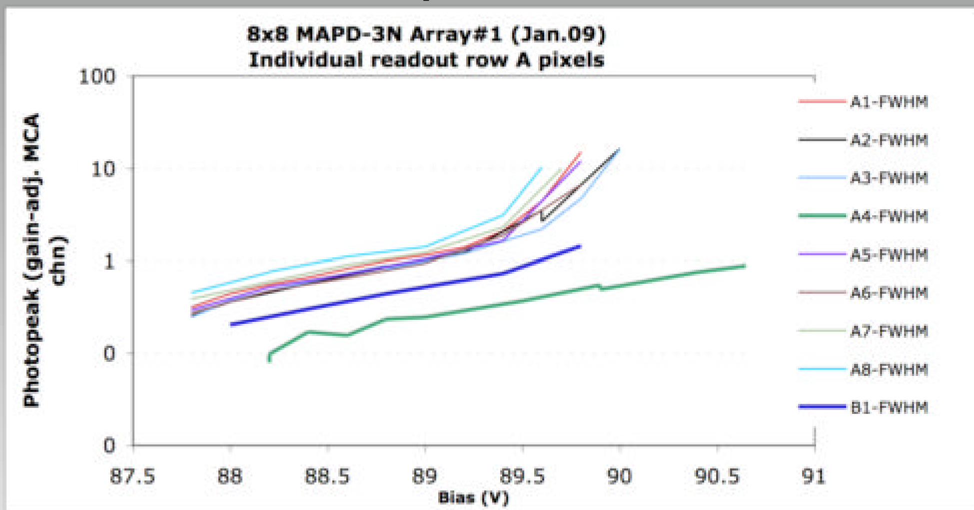
Gain variation an issue

Example from SensL array - same crystal moved to each array element

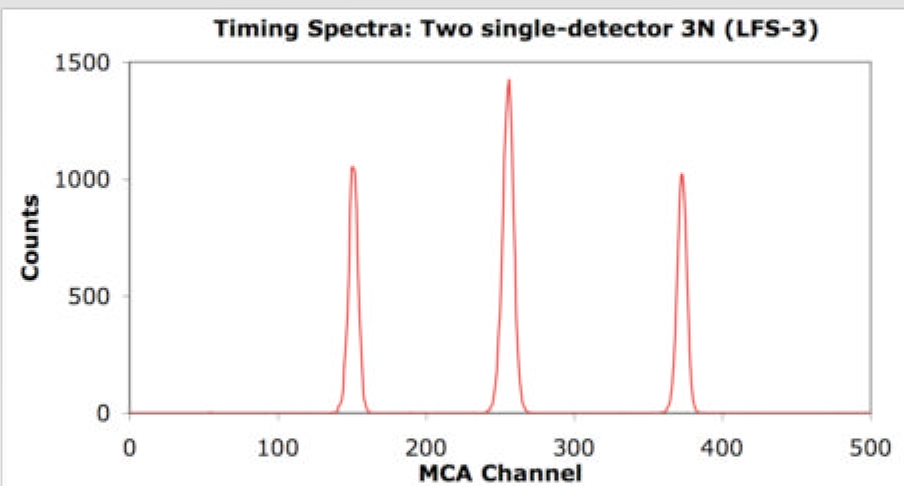


Optima bias V and gain variation

Example from Zecotek MAPD-3N array

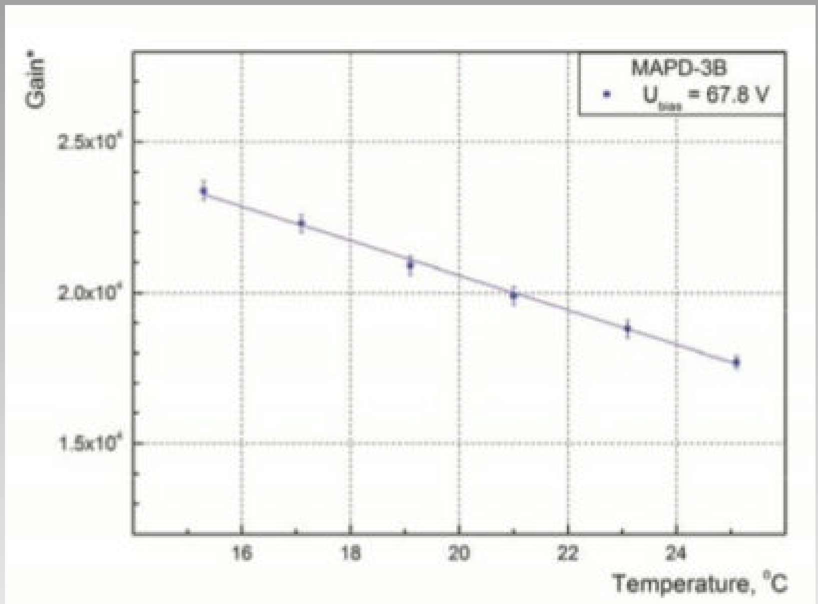


=> Need ASIC with variable gain and bias V per array element



=> 1 ns timing with long leads. Need compact connection to first amplifier -> again suggests ASIC

Temperature dependence



Gain is typically strongly dependent on temperature

Noise is inversely proportional to temperature

Implication is that GM-APDs should be temperature stabilized (i.e., active cooling system)

Most groups working on ASIC readouts

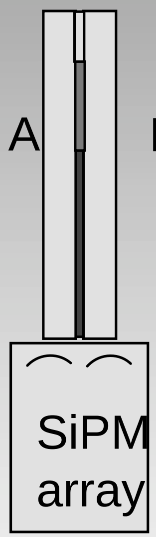
Two basic approaches:

Amplifier and timing circuit for each array element
- Pros: Best SNR for leading edge timing
- Cons: Number of data channels
  Heat generation

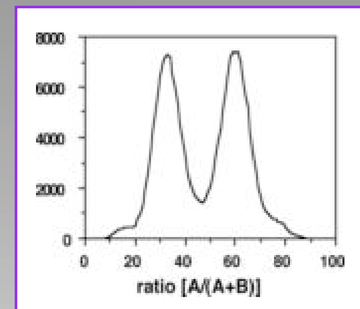
Row/Column summing
- Pros: Number of data channels
  Better control of heat sources
- Cons: Not good for LE timing, need to
  use alternative timing schemes

UW discrete crystal detectors

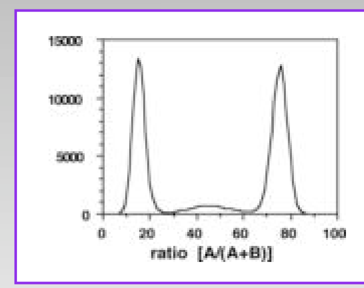
Design interface to ...

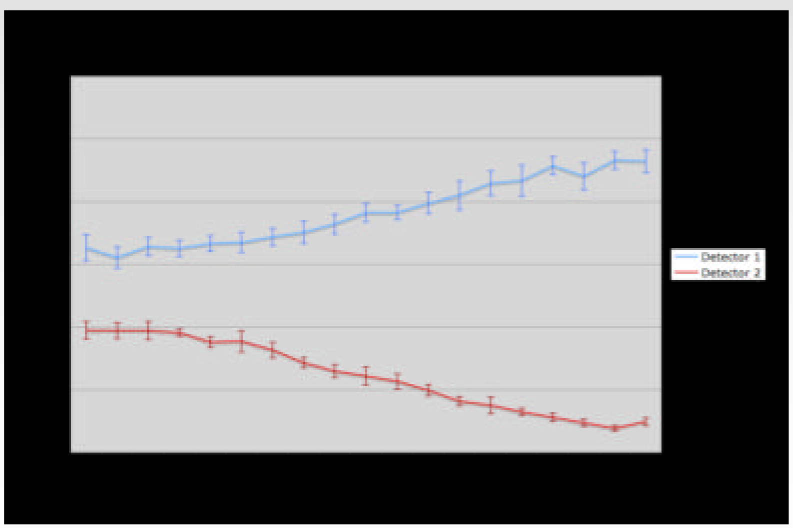


... share large fraction of light



... share very little light





Challenge is scatter in an array of crystals and the number of data channels (>40/detector module and there are 70 to 140 modules in a scanner)

Preliminary data (2004) got 5 mm DOI accuracy. New goal is 2 mm accuracy.

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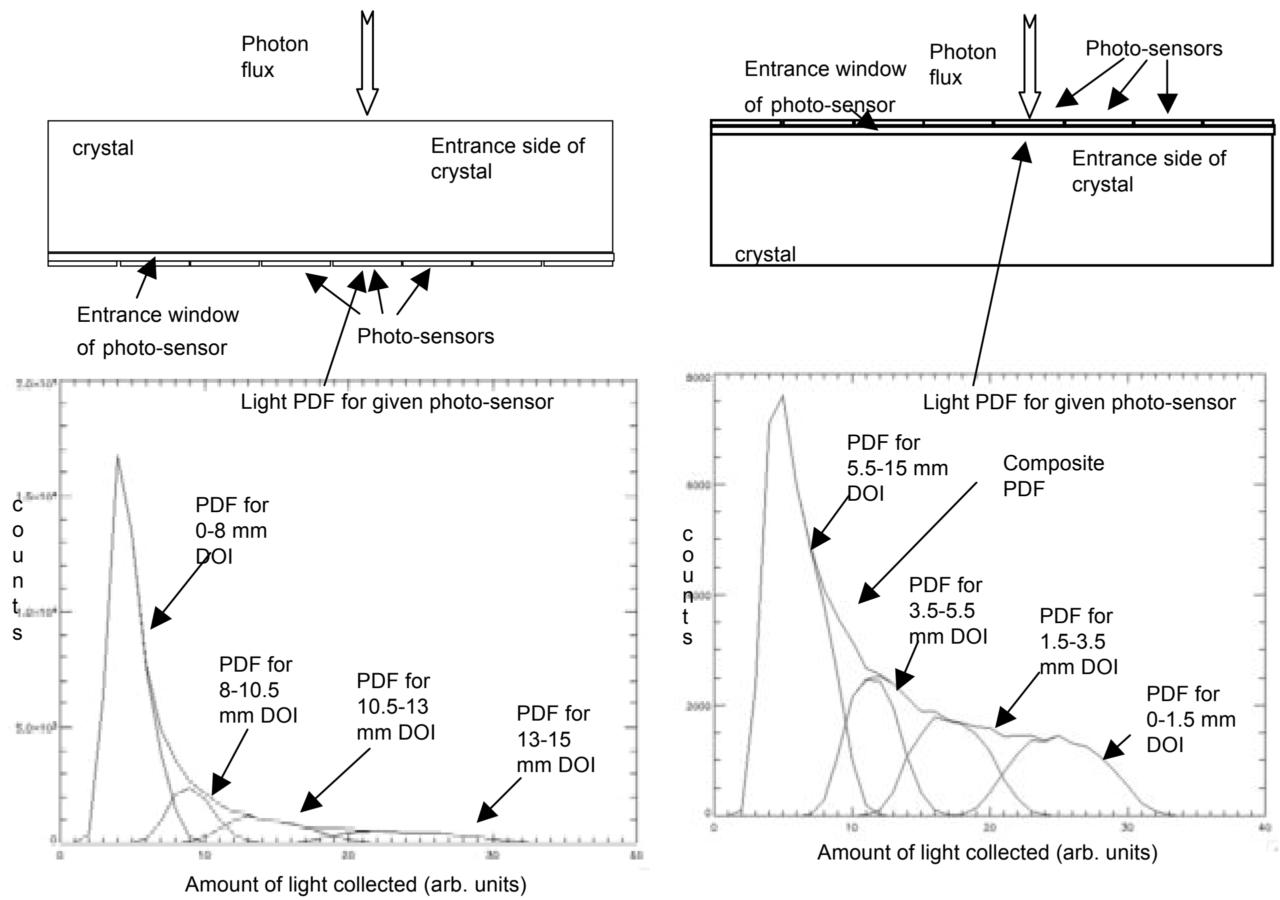
UW monolithic detectors



(a) Diagram illustrating traditional placement of photo-sensors on the back side of the crystal and the associated light PDF for the sensor directly under the photon flux. (b) Diagram illustrated the SEP design and associated light PDF for the sensor directly under the photon flux. In the SEP design a majority of interactions are occurring in the region of the crystal where DOI estimation is the best.

UW approach to FPGA based timing

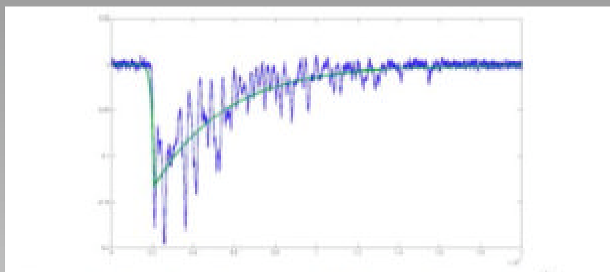


Figure 8: Sample pulse from a PMT coupled to an LSO scintillator, overlaid with the best least squares fit of a curve with exponential rise and fall.

Basic steps

1. Derive reference pulse shape
2. Band limit and digitize
3. Normalize data based on pulse integral to reference pulse
4. Extract pulse start from reference pulse

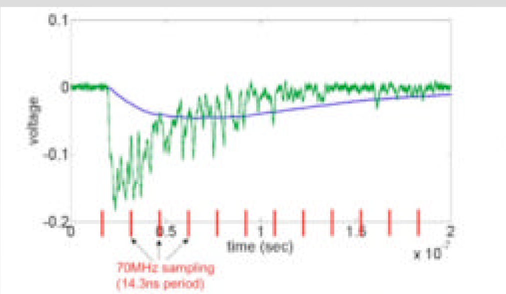
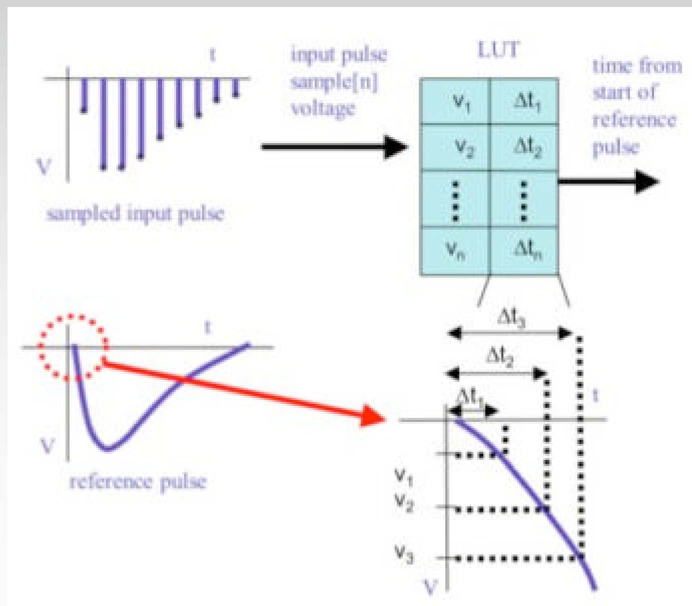


Figure 3. MATLAB plot of a pulse from a LSO scintillator crystal attached to a PMT. A simulated low-pass filter with a 33.3MHz cutoff is also shown. The wide lines on the x-axis indicate the interval at which a 70MHz ADC would sample.



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First test FPGA test results

Experimental data (yellow) taken at 60 and 125 MHz unfiltered with early Zecotek MAPD (slow rise time). Filtered data done by adding a 30 MHz filter in Matlab and then processing with the FPGA.

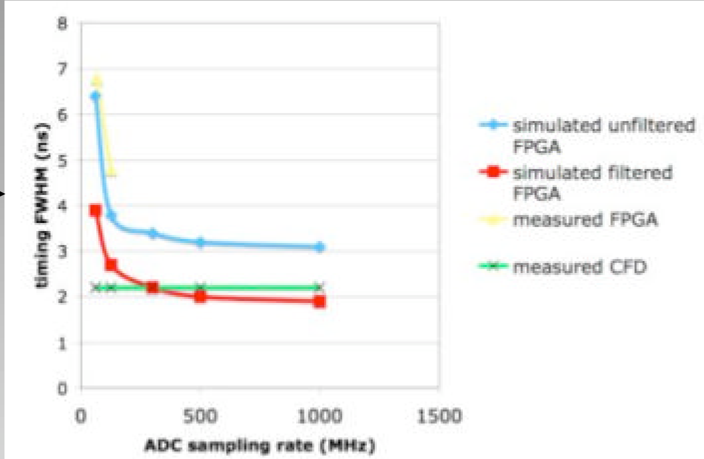


Figure 13. Timing results for simulated and experimental coincidental timing. Note that CFDs do not use ADCs, but the data is included to give a reference.

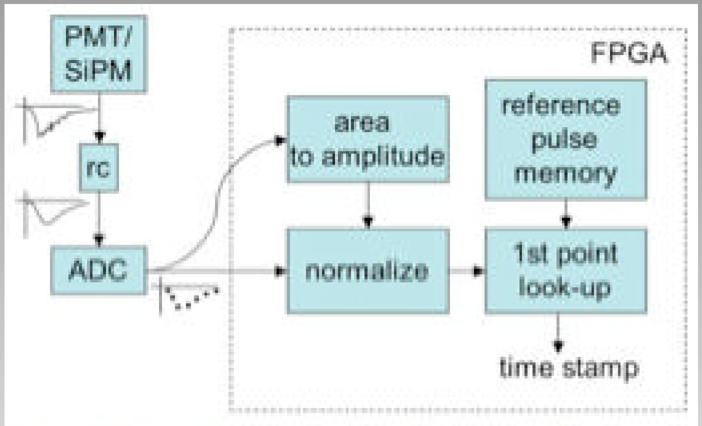
Results from processing signals from a fast MAPD and looking at the SD of time stamp estimates by the FPGA algorithm for different ADC speeds and bandwidth filters.

Table I. Standard deviations (ns) of the distributions of time stamps for different low-pass filter cutoffs and sampling rates.

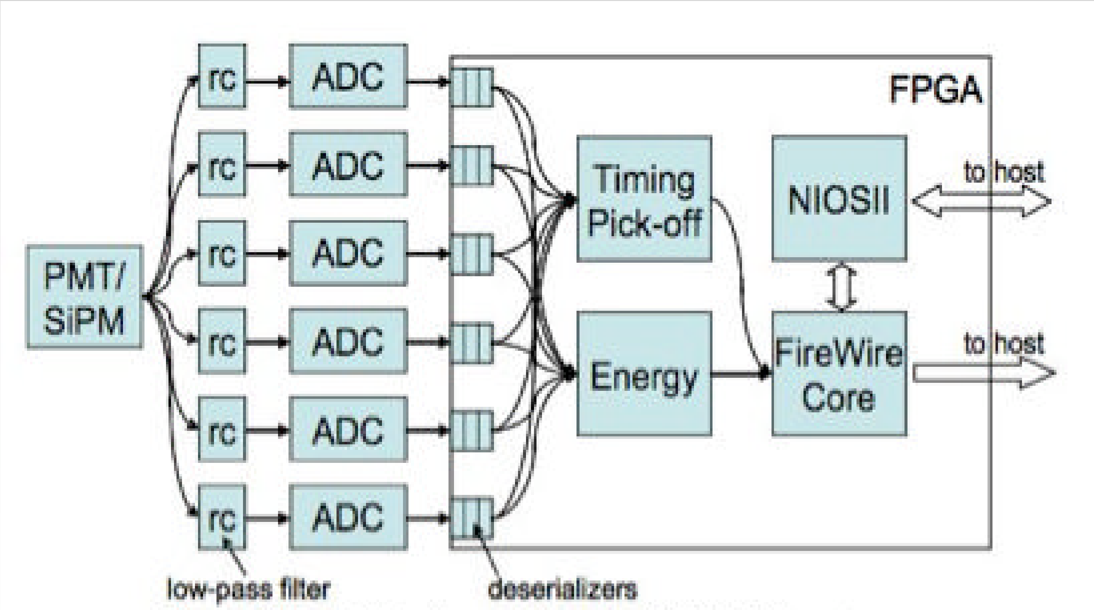
	RC cutoff (MHz)		
ADC rate (MHz)	33.3	16.7	10
70	1.19	1.06	1.03
140	0.78	0.789	0.837
300	0.455	0.543	0.591
500	0.322	0.275	0.409
1000	0.198	0.196	0.198

MiCES phase II electronics

Pulse timing in the FPGA



Up to 48 ADC channels per card, goal is to do it all in one FPGA



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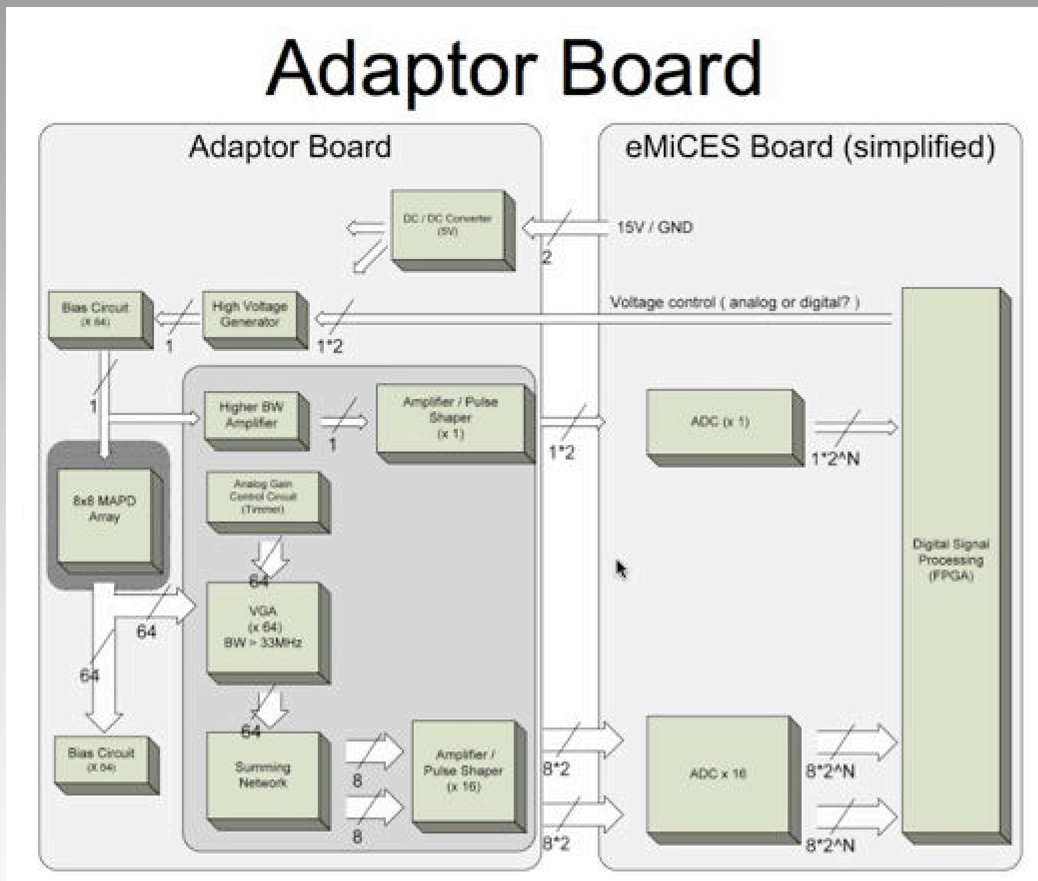
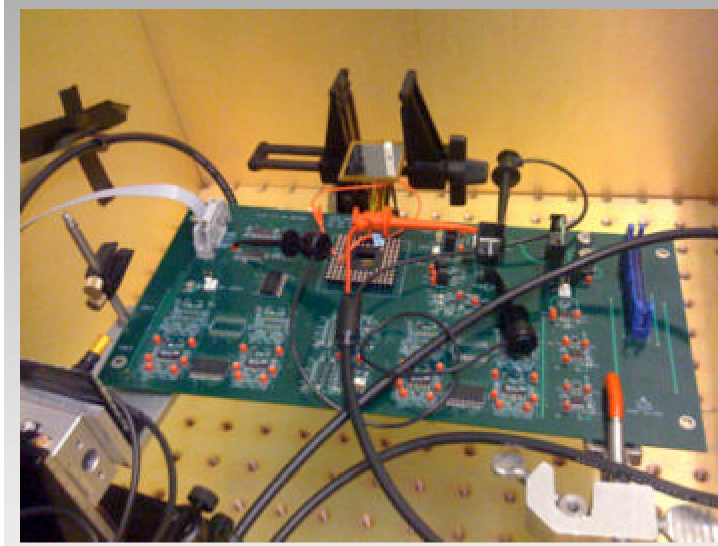
Working on row/column summing





The adapter board will become an ASIC with variable gain and bias for each array element, common anode timing signal, and row/column summing for up to 20x20 arrays

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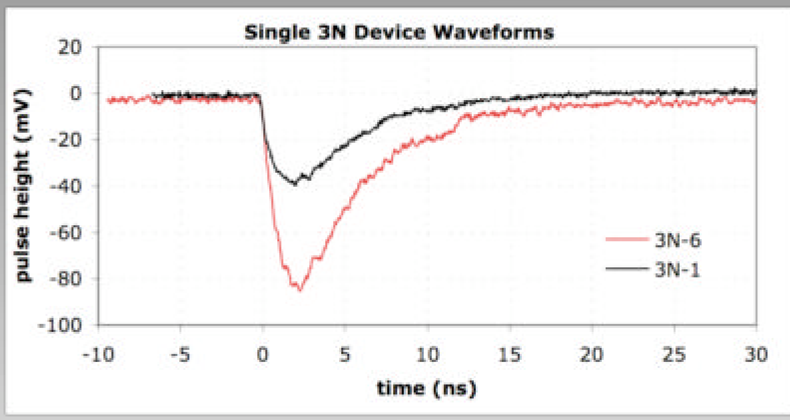
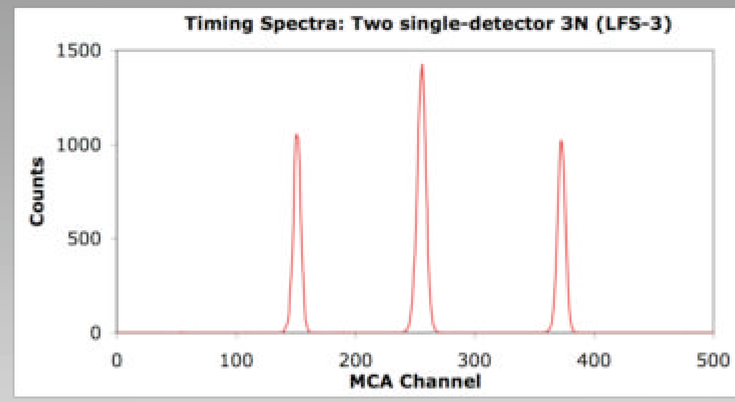
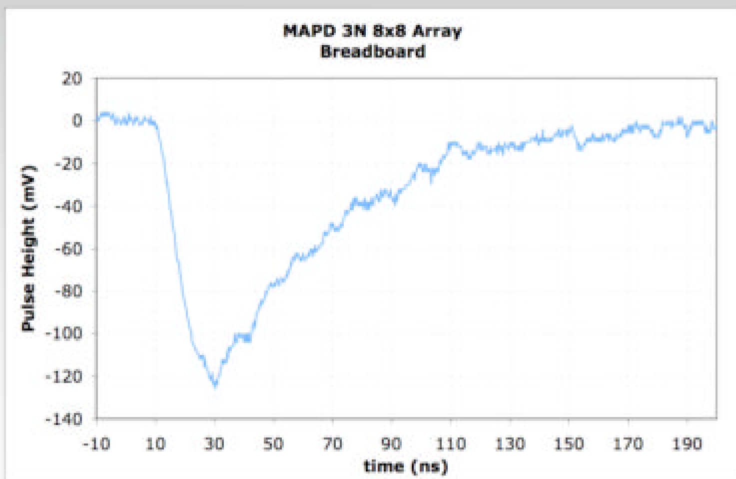
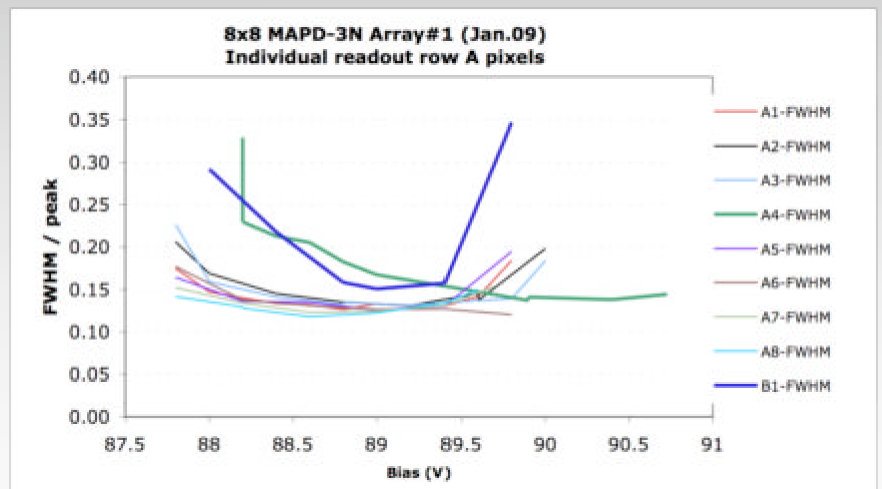
Newest results with Zecotek MAPD and UW row/column prototype board









8x8 board is being assembled and ASIC design will start in March 2009

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That's All Folks!

The best kind of small animal imaging :-)