NUMI Off-Axis Workshop
Argonne Meeting

Electronics for Resistive Plate Chambers

Presented By

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Apr. 25, 2003

Outline of Talk

I. System Architecture

II. Description of System Components

III. Physical Configuration

IV. Cost Estimate

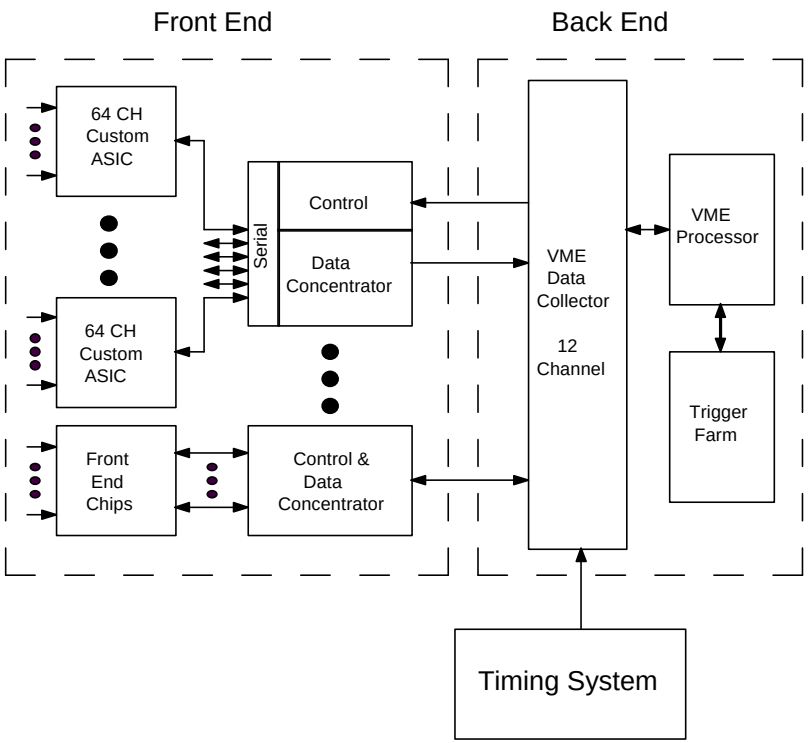
V. Summary

See:

www.anl.gov/drake/numi_off_axis/030425_workshop.pdf

System Architecture

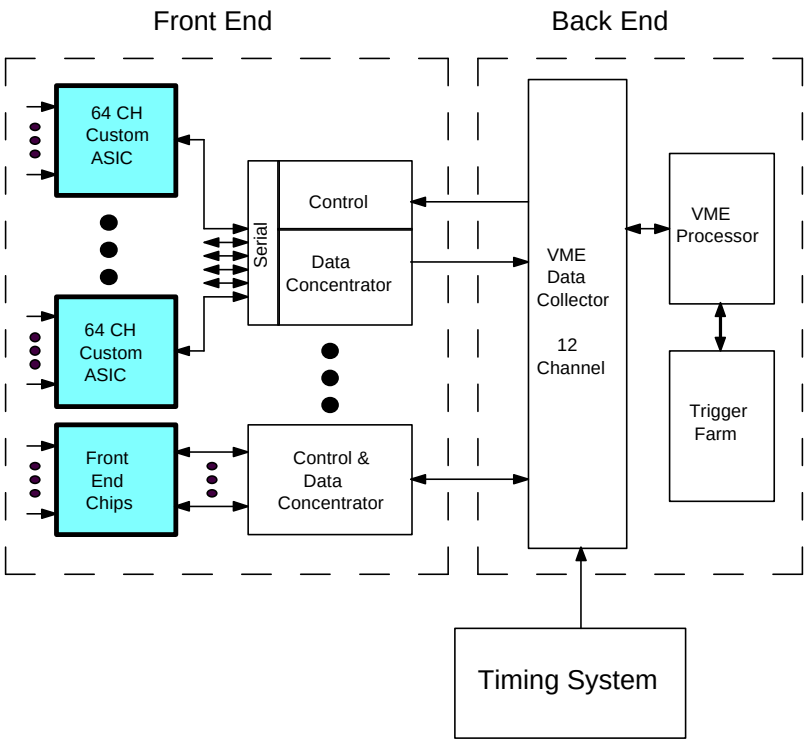
- **System Overview**
  - Discriminate Hits from Detector
  - Timestamp Hits in Front End
  - Store Timestamps in Local Buffers
  - Read Buffers Periodically
  - Use Back End Trigger Processor to Reconstruct Hits



- ➢ *Trigger-less* – Like MINOS
- ➢ Similar to a Parallel Development for the Linear Collider
- ➢ Primary Goal: Cheap Electronics, 1 Bit Dynamic Range

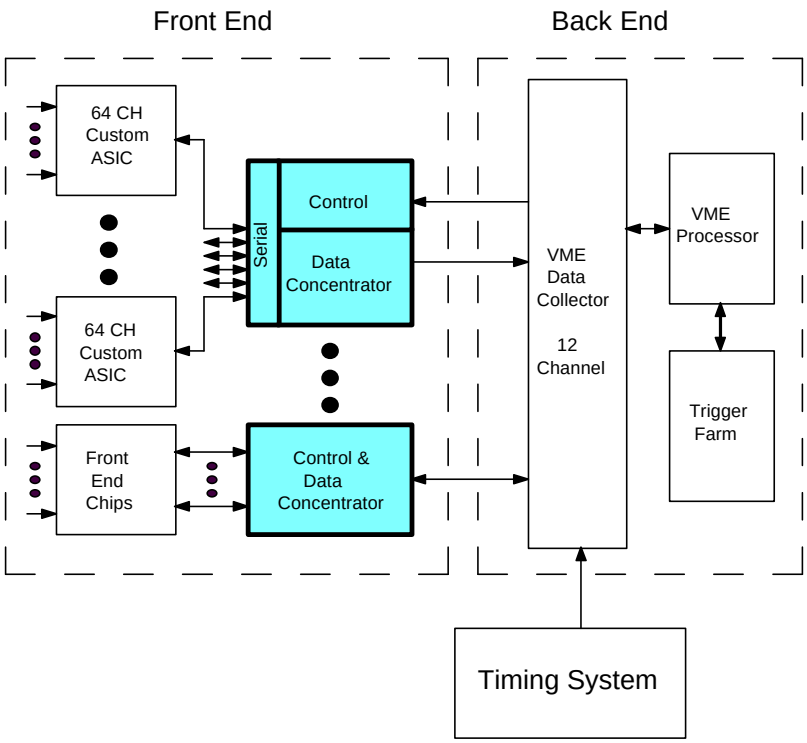
System Architecture

- **Front End**
  - **Custom ASIC**
    - Resides on Chambers
    - Performs Functions:
      - » Receive Detector Signals Differentially
      - » Timestamp Hits
      - » Temporary Data Storage
      - » Serial I/O
    - Services 40 Detector Channels (→ 64)



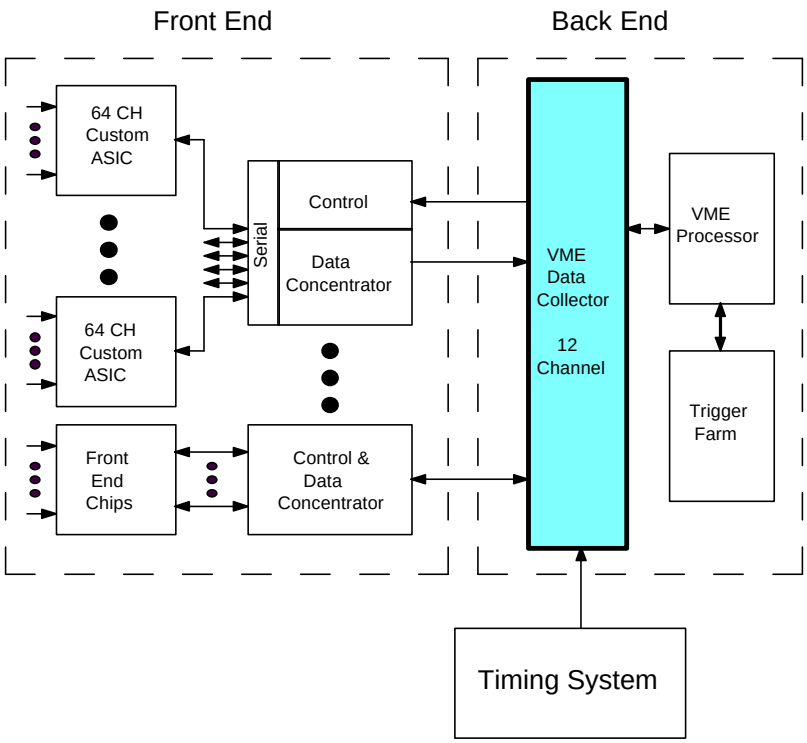
System Architecture

- **Front End (Cont.)**
  - **Data Concentrator:**
    - Concatenate Serial Data Streams from Several Chips
    - Drive Single Serial Line to Back End Read-Out Electronics
    - Handles Control Interface



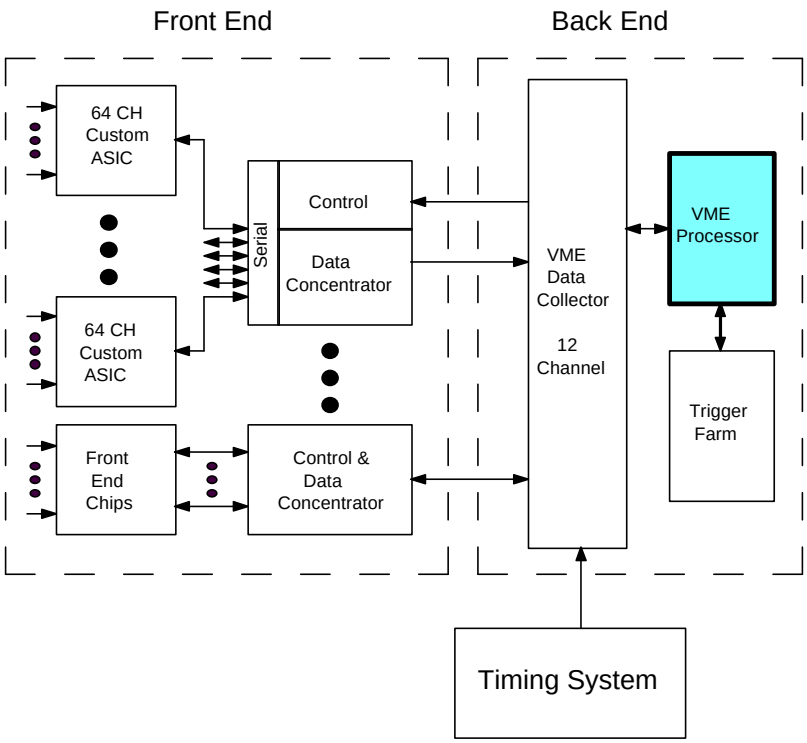
System Architecture

- **Back End**
  - **VME Data Collector:**
    - 9U x 400 mm VME
    - Receives Serial Data Streams from Several Data Concentrators
    - Stores Data in Buffers
    - Buffers Read by VME Processor



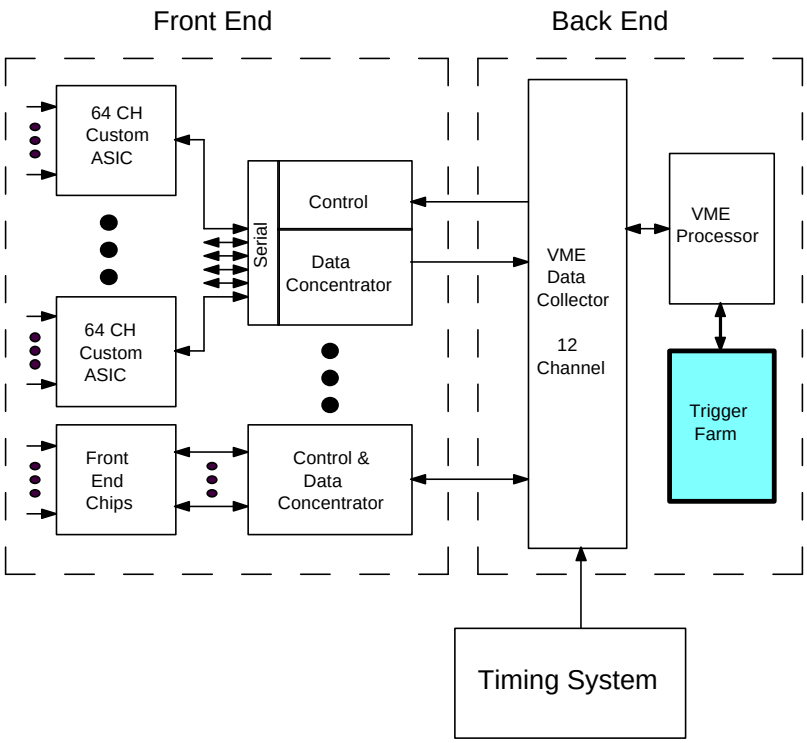
System Architecture

- **Back End (Cont.)**
  - **VME Processor:**
    - Receives Data from All Data Collectors in VME Crate
    - Forms Time Frames from Timestamps (~1 Sec)
    - Sends Time Frames to Trigger Farm for Processing



System Architecture

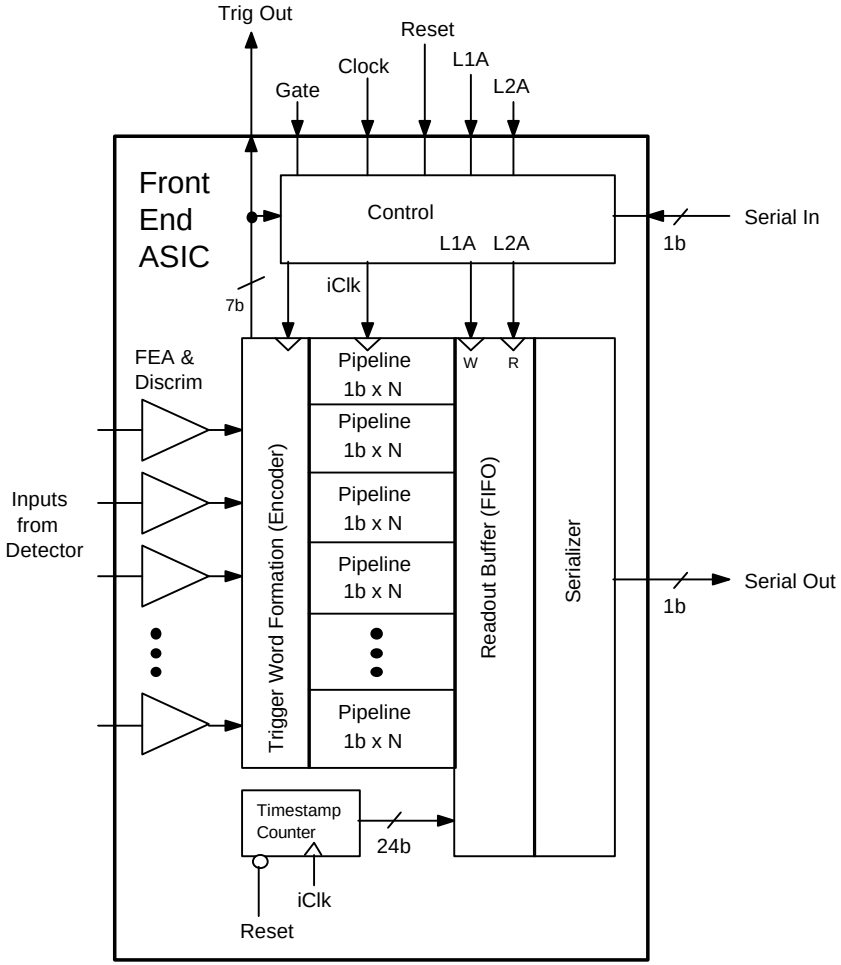
- **Back End (Cont.)**
  - **Trigger Farm:**
    - Receives Time Frames from All VME Processors in System
    - Uses Timestamps in Pattern recognition Algorithm to Find Tracks
    - Write Good Data to Disk
    - Discards Junk



➢ ***Trigger Processing*** **– Like MINOS**

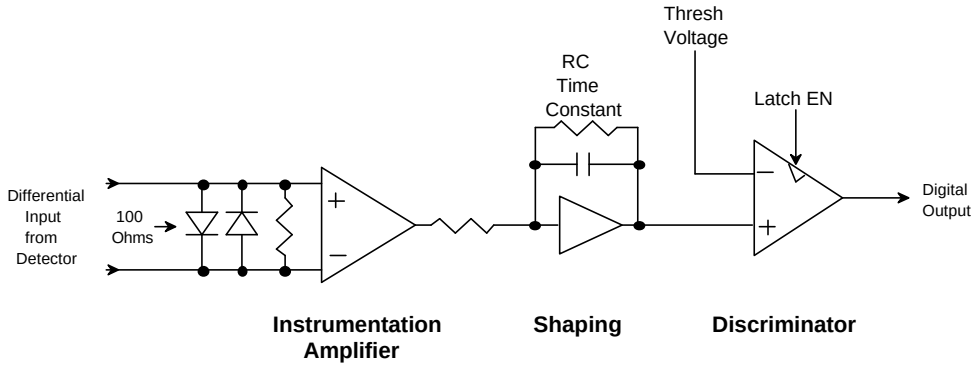
System Components

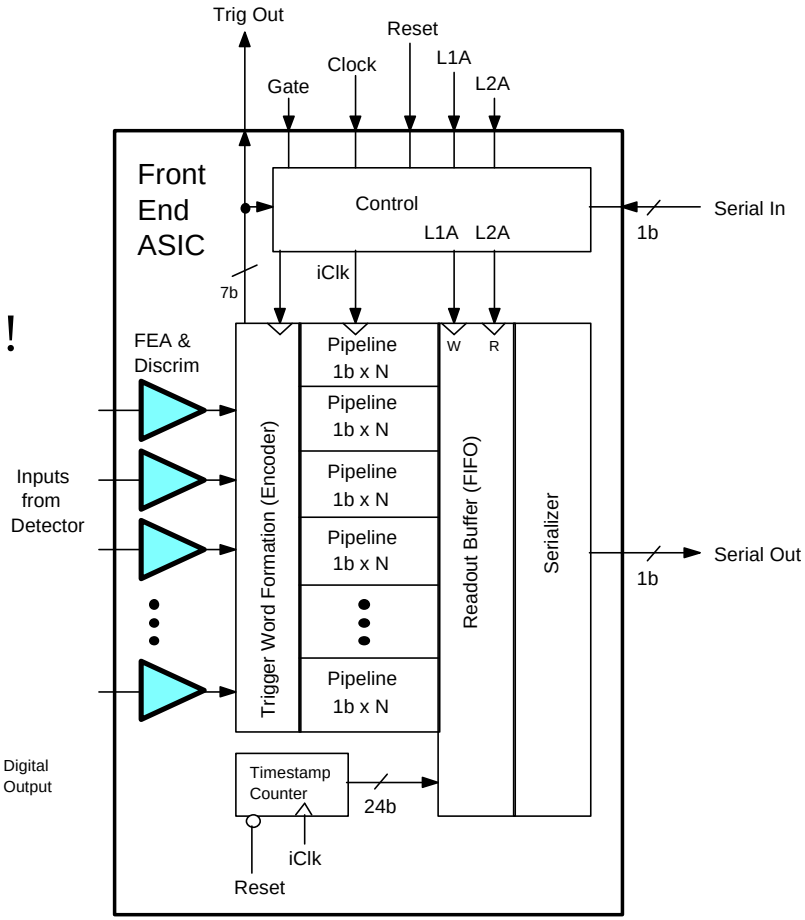
- **Front End ASIC**
  - **Basic Architecture**
    - Front End Amplifier & Discriminator Senses Hits Above Threshold
    - Bits Clocked in Shift Register
    - Save Bits & Timestamp on L1A or Self-Trigger
    - Serial Output – Data Serial Input - Control
    - 24-Bit Timestamp Counter Runs at 10 MHz
    - Services 40 CH (→ 64)



System Components

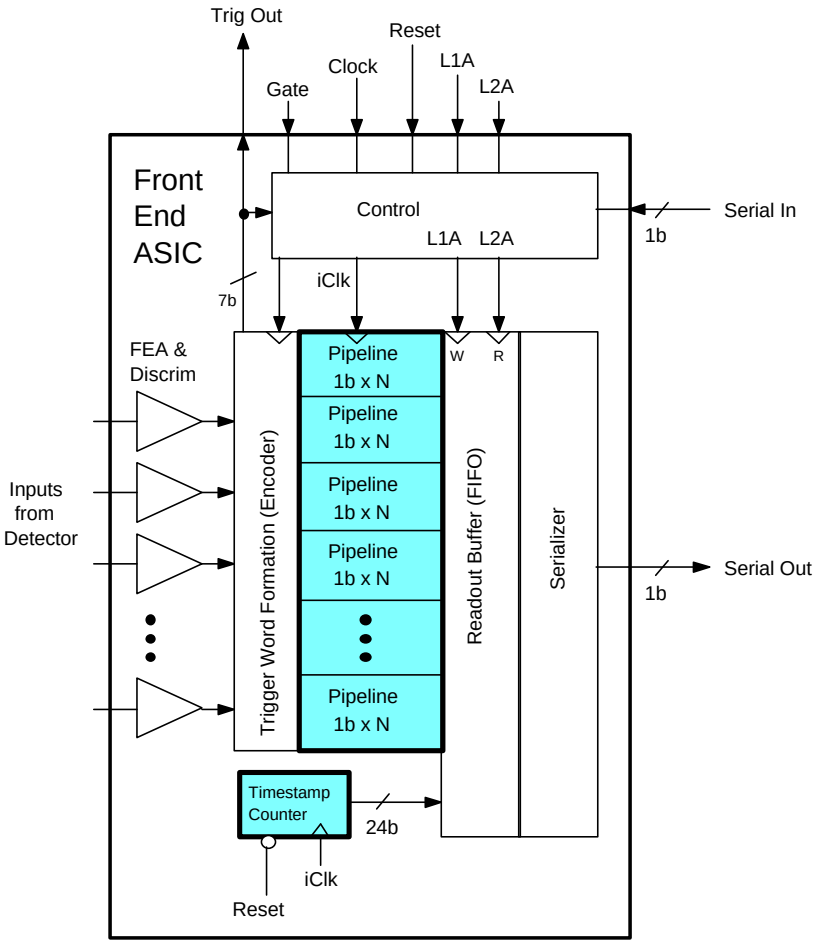
- **Front End ASIC (Cont.)**
  - **Each FEA Channel Has:**
    - Instrumentation Amp Receives Signal Differentially
    - Pulse Shaping
    - A Discriminator - a 1-Bit ADC!
    - Adjustable Threshold Voltage
    - Can Accommodate Positive or Negative Input





System Components

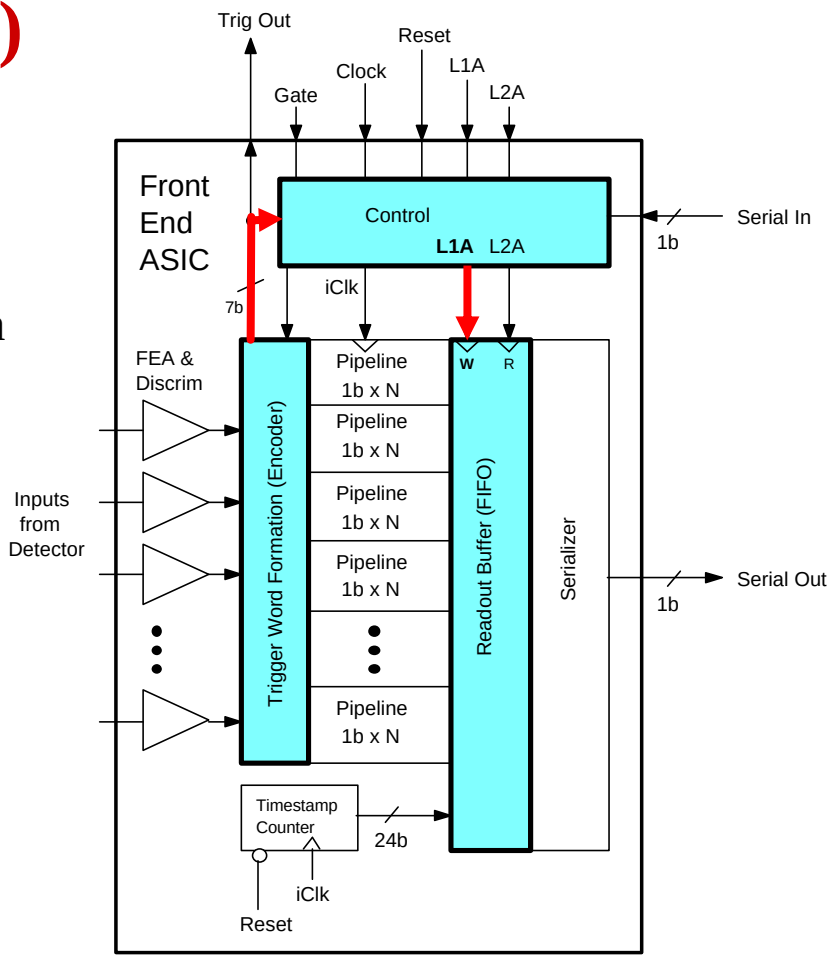
- **Front End ASIC (Cont.)**
  - **Shift Register:**
    - Bit Pattern Shifted Through Pipeline with 10 MHz Clock
    - Store Bits in Read-Out Buffer on L1A
    - Read-Out Buffer Stores Multiple Events
  - **Timestamp:**
    - Timestamp Counter Runs at 10 MHz → 100 nS Resolution
    - Store Timestamps in Read-Out Buffer on L1A
    - Reset Counters Globally 1/Sec → Need 24 Bits



System Components

- **Front End ASIC (Cont.)**
  - **Triggering:**
    - Self-Trigger:
      - » Auto-Generate L1A When Hit, Single or Combination
      - » Timed to Capture Event of Interest at End of Pipeline
      - » Readout Buffer is FIFO, and Can Store Multiple Events

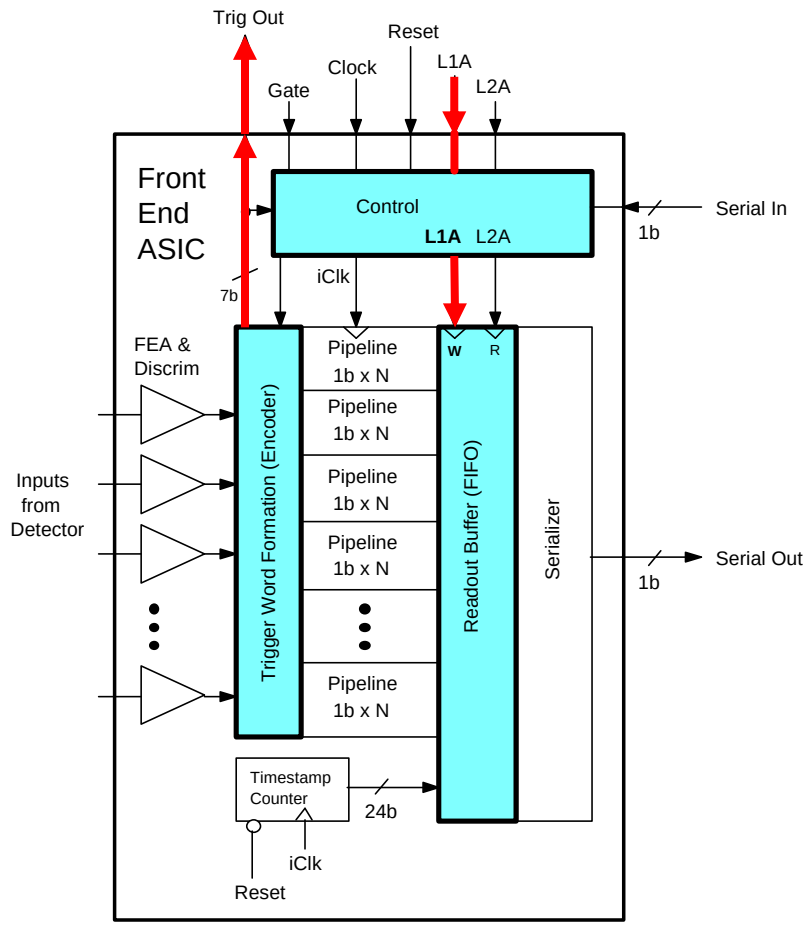
➢ ***Use This Mode for Normal DAQ***



System Components

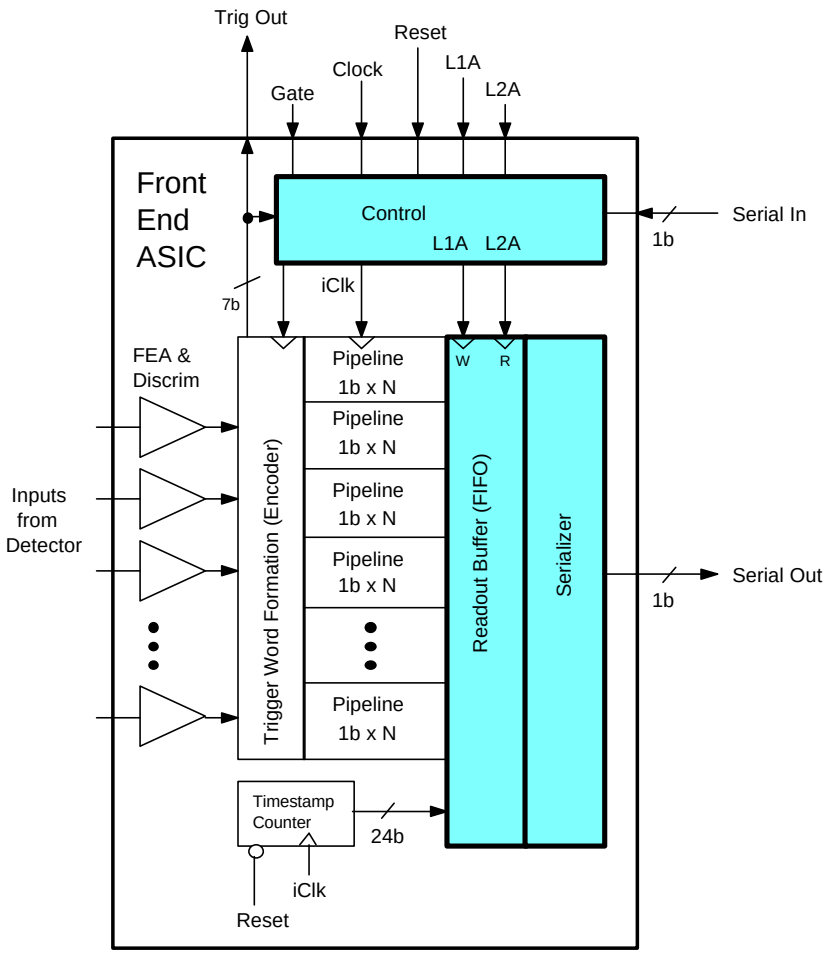
- **Front End ASIC (Cont.)**
  - **Triggering (Cont.):**
    - External Trigger:
      - » Can Send Signal to External Trigger System
      - » Can Receive L1A & L2A from External Trigger System
      - » Pipeline Length Determines Trigger Latency
      - » Can Receive Gate from External Timing System

➢ ***Use This Mode for Test Beams & High-Rate Environments***



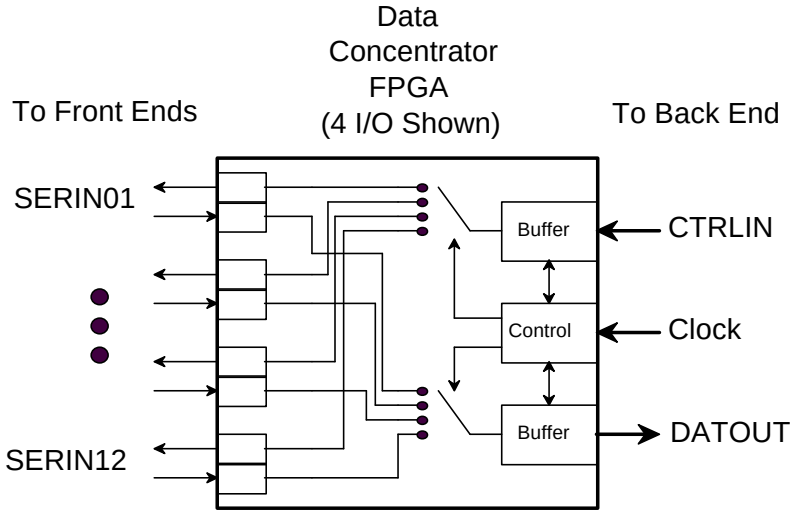
System Components

- **Front End ASIC (Cont.)**
  - **Serial I/O:**
    - Single Serial Line for Data & Control
    - Runs at 100 MHz
    - 88 Bits/Event, + Control → ~1 uS/Event
    - UART Reads FIFO Whenever FIFO Not Empty
    - Use Control For:
      - » Threshold DAC
      - » Charge Injection
      - » Diagnostic Bit Patterns



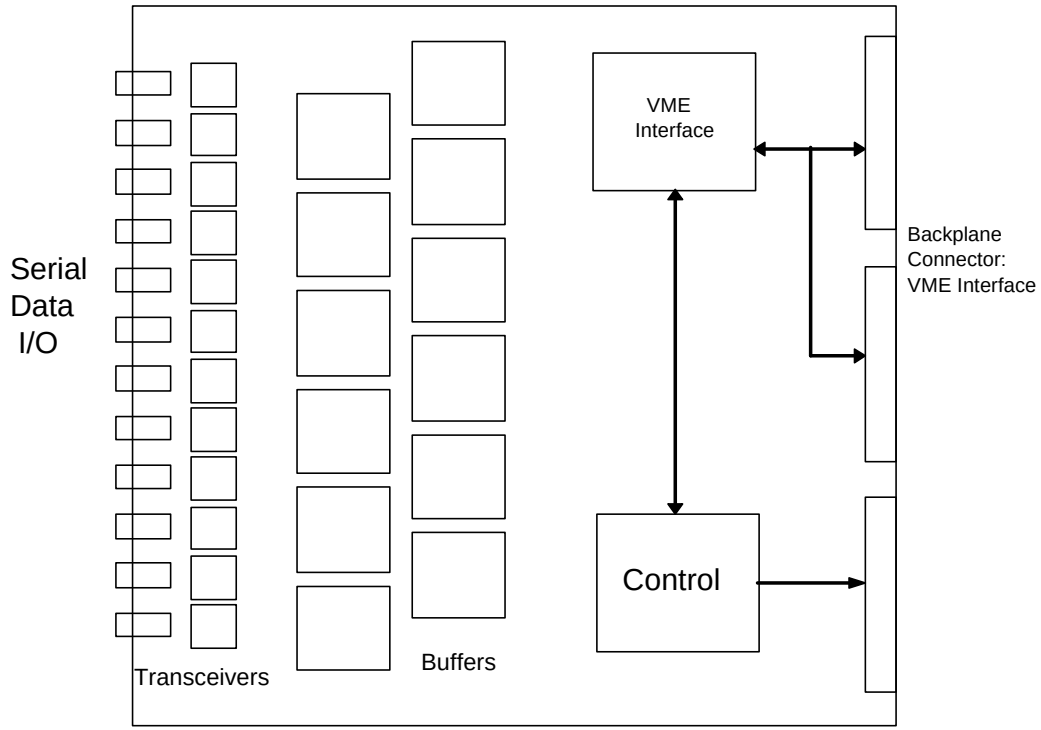
System Components

- **Data Concentrator**
  - **Coalesces Several Serial Data Streams into One**
  - **Needed to Reduce Back-End Costs**
  - **Realize with FPGA**
    - Applies ID to Identify Source
    - Has Buffering
    - Has Flow Control
  - **Similar Device Serves to Coalesce Data Multiple Concentrator Outputs into One Data Stream → "Super" Concentrator**



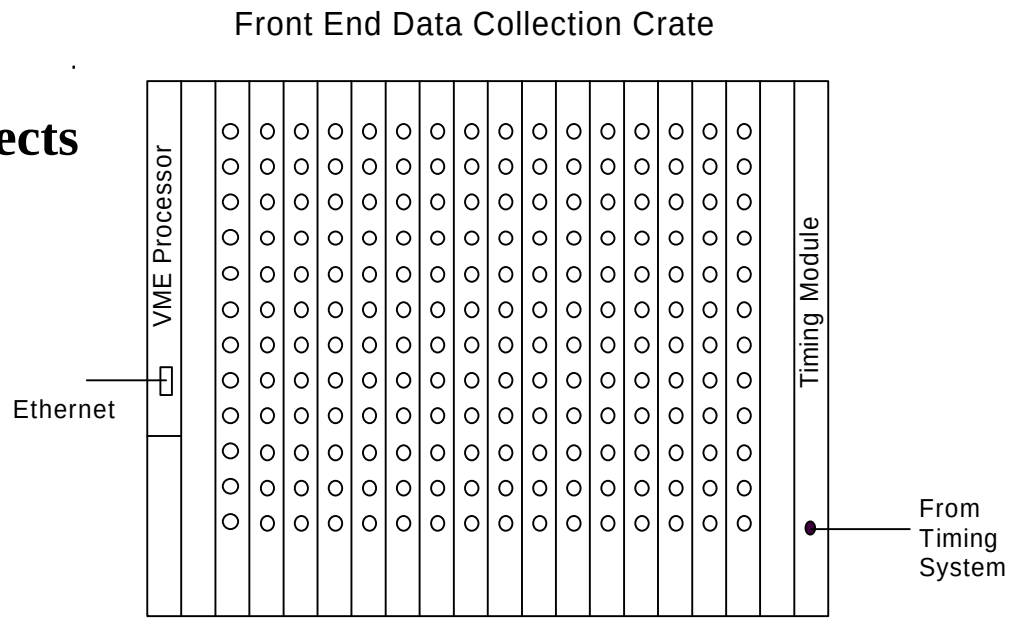
System Components

- **Data Collector**
  - Use VME as Read-Out Infrastructure
  - 9U x 400mm, 12 Inputs
  - Receives Data Streams
  - Saves Data in One of Two Buffers
  - Read Buffers from VME
  - Also Provides Control



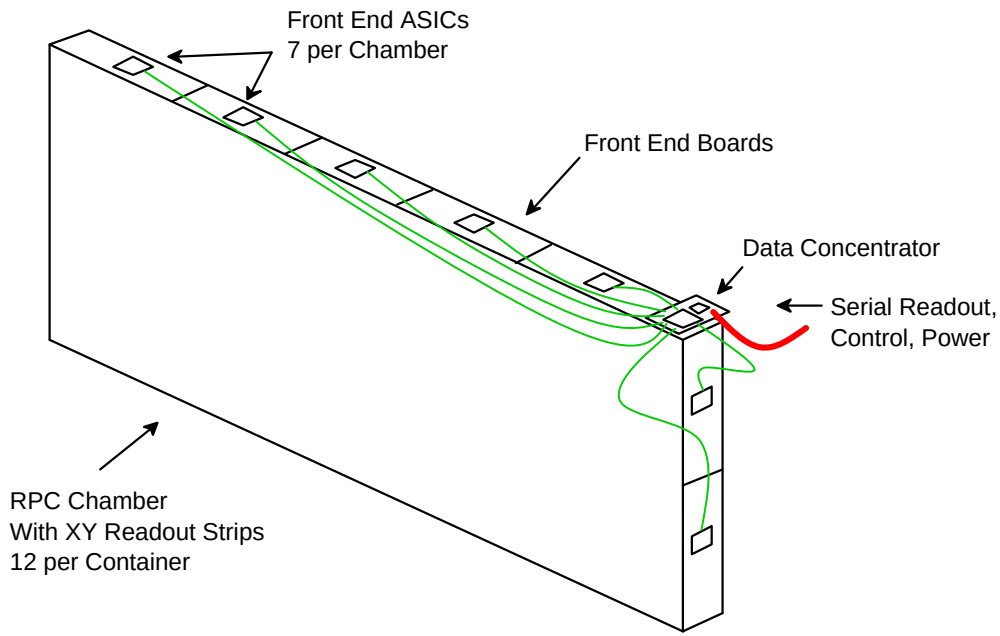
System Components

- **Data Collector Crate**
  - VME Crate Can Hold ~20 Data Collectors
  - VME Processor Connects to Network & Trigger Farm



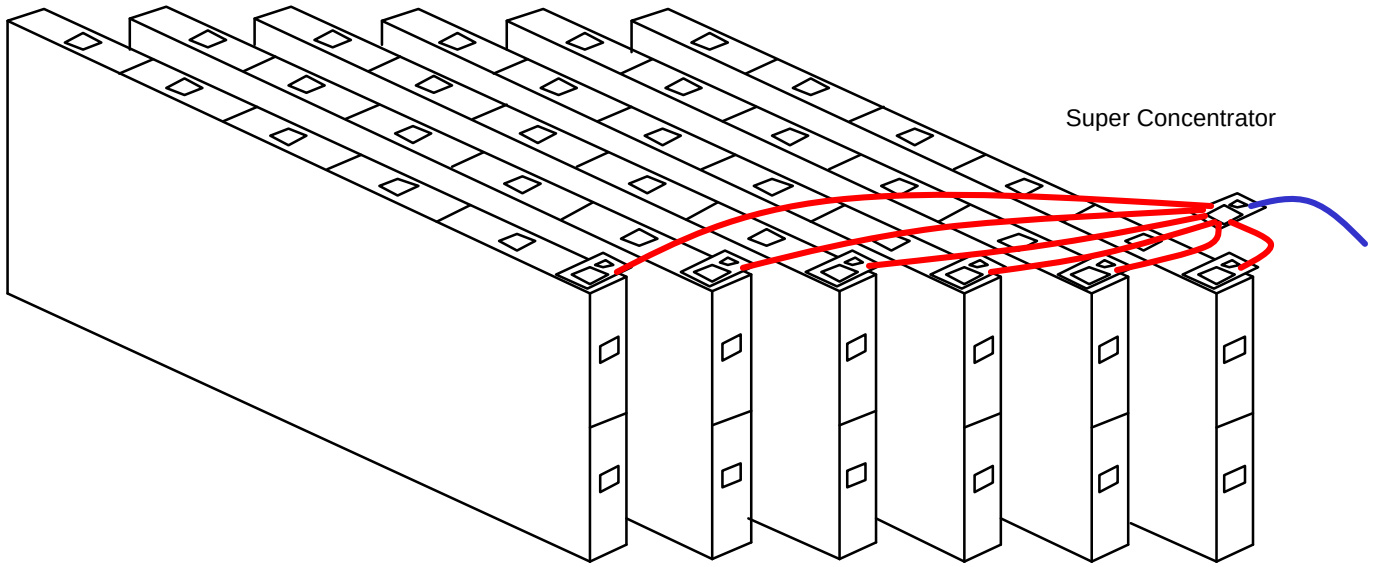
Physical Configuration

- **Electronics on Each Plane**
  - 200 Y Strips/Plane, 80 X Strips/Plane
  - Use 40 Ch/Chip → 7 Chips/Plane
  - Each ASIC Resides on a Printed Circuit Board → 7 FE Boards/Plane
  - 1 Data Concentrator per Plane – Collects Data from 7 Front End Chips
  - Each Data Concentrator Resides on a Separate PCB on Plane



Physical Configuration

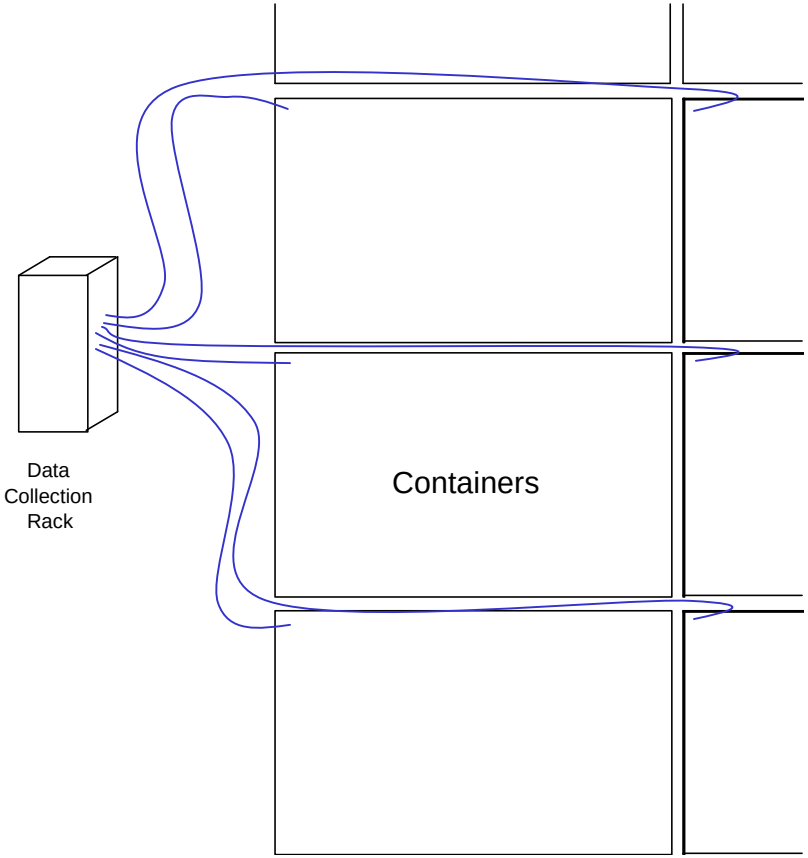
- **Planes in Container**
  - 12 Planes/Container
  - 1 "Super" Concentrator per Container
  - Use VECSEL Optical Drivers w/Fiber for Output



(6 of 12 Planes Shown)

Physical Configuration

- **Connections to Container**
  - One Group of Cables per Container
  - Cable Bundle Includes Serial Data, LV Power, HV Control
  - 1 VME Crate Services ~200 Containers, But Need Space for LV Power Supplies…



Physical Configuration

- **Bandwidth Considerations**
  - **Per ASIC Output (Data Concentrator Input)**

    (15 m^2/plane * 1 KHz/m^2) / 7 Chips/Plane = ~2 KHz = 1 Event/500 uSec

    88 b/event * **100 nS/b** = ~10 uS/event << 500 uSec → **OK**
  - **Per Data Concentrator Output (Super Concentrator Input)**

    15 KHz/plane → 1 Event Every 66 uSec

    (91b/event * **100 nS/b**) = ~10 uS/event < 66 uSec

    → **OK w/Buffering & Flow Control** (Can Run This Link Faster…)
  - **Per Super Concentrator Output (Data Collector Input)**

    12 planes * 15 KHz/plane = 180 KHz → 1 Event Every 5.6 uSec

    (~100b/event * **10 nS/b**) = ~1 uS/event < 5.6 uSec

    → **OK w/Buffering & Flow Control**

    → **Probably Need Fiber for Long Cable Runs @ 100 Mbps**

Physical Configuration

- **Power Considerations**
  - **Per ASIC *(10 MHz Operation)***

    ~15 mW/CH * 64 CH = ~ 1 Watt/Chip → 84 Watts/Container
  - **Per Data Concentrator *(10 MHz Operation)***

    ~ 0.25 Watt/Device → 6 Watts/Container
  - **Per Super Concentrator *(100 MHz Operation)***

    ~2 Watts/Device → 2 Watts/Container
  - **Per Container**

    → ~100 Watts

Costs

• Assumptions

Component	Needed for Detector	Number to Produce **REQUIRED**
Basis of Counts:		
Number Channels/Plane	280	
Number Planes/Container	12	
Number Containers	2,000	**2,000**
Total Number of Planes	24,000	**24,000**
Total Number of Channels	6,720,000	**6,720,000**
Number Channels/ASIC	40	
Number ASICs/Plane	7	
Number ASICs/DatConc	7	
Number DatConc/SupConc	12	
Number SupConc/Data Collector	12	
Number Slots/VME Crate	17	

Costs

Component	Needed for Detector	Number to Produce **REQUIRED**	Total Cost M&S	Total Labor Cost	Total Cost w/Labor	Overall Average Unit Cost Total
Items to Produce:						
Data Collectors	167	**183**	$595,013	$30,140.00	**$625,153**	$3,422.37
Front End Boards	168,000	**184,800**	$7,585,300	$620,928.00	**$8,206,228**	$44.41
Data Concentrator Boards	24,000	**26,400**	$4,108,200	$279,180.00	**$4,387,380**	$166.19
Super Concentrator Boards	2,000	**2,200**	$493,600	$31,350.00	**$524,950**	$238.61
VME Timing Modules	10	**12**	$12,250	$396.00	**$12,646**	$1,053.83
Items to Purchase:						
ASICs	168,000	**200,000**	$3,721,000	$0.00	**$3,721,000**	$20.14
VME Crates	10	**15**	$51,750	$450.00	**$52,200**	$3,480.00
VME Power Supplies	10	**13**	$52,000	$429.00	**$52,429**	$4,033.00
Front End Power Supplies	2,000	**2,201**	$440,200	$72,633.00	**$512,833**	$233.00
FE-DatConc Cables	168,000	**168,500**	$168,500	$0.00	**$168,500**	$1.00
DatConc-SupConc Cables	24,000	**24,200**	$48,400	$0.00	**$48,400**	$2.00
SupConc-Data Collector Cables	2,000	**2,200**	$22,000	$0.00	**$22,000**	$10.00
Power Cables	2,000	**2,200**	$22,000	$0.00	**$22,000**	$10.00
Timing System Cables	10	**12**	$480	$0.00	**$480**	$40.00
Total Costs			$17,320,693	$1,035,506	**$18,356,199**	**$2.73**

Avg. Cost/Ch

Summary

- **Primary Goal of Electronics for RPCs:** ***CHEAP***
  - Low Event Rate (Mostly Noise)
  - Low Dynamic Range (1 Bit)
  - Low Clock Speed
  - Funnel Many Channels into a Read-Out Board (VME Real Estate is Expensive)
- **Requires ASIC to Achieve Low Cost & Desired Performance**
  - Not a Big Deal These Days, But Does Take A While
  - Chip Has Many Blocks, But Each Block is Straight-Forward
- **ASIC Development to Begin Soon (→ Linear Collider)**