

# Evaluation of Prototype RoI Builder in Integration with Level 1 RODs

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## 1.0 Introduction

This note discusses an evaluation of the performance of the RoI Builder, the interface between the Level 1 and Level 2 trigger, in a phase 1 integration with both the muon readout driver (MIROD) [1] and calorimeter readout driver (CPROD) [2]. The RoI Builder collects ROD records in the standard Atlas format from the muon, calorimeter and central trigger processor and combines these records from an event into a single record which is sent to a Level 2 supervisor processor. S-Link [3] interfaces are used for both the input and output of the RoI Builder.

## 2.0 Goals of the Integration

In the phase 1 integration, the MIROD and CPROD were integrated with the RoI Builder separately. Integration of the two systems together is planned for a later phase. The goals of these studies was to test the basic compatibility of the RODs and RoI Builder in three areas: interfaces, performance and robustness [4].

### 2.1 Interfaces

S-Link interfaces are used between the RODs and RoI Builder. For the phase 1 tests, it was agreed to use copper interfaces built at ANL, mainly due to the availability of these cards. Issues to be addressed included:

- timing of electrical signals
- synchronization of control and data signals
- data format compatibility
- data correctness

### 2.2 Performance

The issues to be studied in the area of performance were the following:

- what is the maximum Level 1 accept rate that can be sustained
- what is the latency of the RoI Builder and ROD from the Level 1 accept to the delivery of the assembled event to the Level 2 supervisor

## 2.3 Robustness

The issues to be studied in the area of fault tolerance and robustness are the following:

- does the flow control mechanism work correctly
- if data is lost or corrupted does the RoI builder recover correctly

## 3.0 Test Procedures and Results

The major goals of the phase 1 integration was to study compatibility of the hardware components. Custom software solutions were developed to control the components and validate the integrate of the data records. The RODs and RoI Builder were controlled with separate programs run by experts of each component. Use of the On-line Software environment, where all components could be controlled from a central location is planned for a later phase of the integration.

Sets of test events were prepared in an ASCII format. The test events were preloaded into the memory of the ROD as well as the Level 2 supervisor processor. The RODs then delivered events to the RoI Builder which sent them on to the supervisor where a byte by byte comparison was made. In the case of the CPROD, the L1ID and BCID were overwritten by values derived from the TTC system, so these words were not compared by the supervisor. For the MIROD, a set of one or two events was loaded and cycled over, while for the CPROD, larger sets of events (127 to 1024) were used.

### 3.1 MIROD Results

The first problem occurred in the MIROD integration and was traced to the timing of the clock signal with respect to the data and control signals. The clock allowed insufficient time to latch the data in the RoI Builder logic which ORed the clock and link write enable signals to produce a FIFO write enable signal. The delay caused by this logic gate was enough to miss the data and control signals. The phase was shifted first by adding additional cable to the clock signal and later by adding circuitry to the RoI Builder input to time the clock. This provided a system which worked well enough to allow study of rates, latency and flow control behavior.

After making this clock phase adjustment, the MIROD integration proceeded smoothly. The system was run at rates between 20 kHz and 80 kHz where the data comparison running on the supervisor limited the rate. At this point, flow control signals were sent back to the MIROD which correctly handled the condition and stopped sending event records in time to avoid data loss.

### 3.2 CPROD Results

Timing in the CPROD was not so tight as in the MIROD. Adjustment of the clock phase was not necessary. However, flow control was not handled properly between the two systems. After receiving a link full signal, the CPROD continued to send until the current

record was completely sent. This caused the RoI Builder to lose data since it asserted link full for about 2 microseconds each time it shifted a record out of its input FIFO. Any data transmitted during this period was lost. Furthermore, the logic on the input card of the RoI Builder would lock up and accept no more data if start and stop control words were received out of order.

Several iterations were done on the firmware of the CPROD to solve these problems, but data corruption was not eliminated within the CPROD if flow control was needed. Due to these problems, only very low rates could be sustained (around 1 kHz). Even though the average rate that the supervisor could read and compare event records was much higher (60-70 kHz), fluctuations in this rate could temporarily cause back pressure in the system which was not handled properly.

### **3.3 Latency Measurements**

If the cables to the S-Link interfaces on the output of the RoI Builder were disconnected, the RoI Builder operated in a mode where flow control is never asserted. This mode could be used to measure the latency of the hardware components in the RoI Builder by measuring the timing of signals that indicate start and stop times to process a record. Latencies were measured by observing timing of the following signals

- Level 1 Accept
- S-Link control signals at input to RoI Builder
- S-Link control signals at output of the RoI Builder.

These signals give the latency within the ROD, within the S-Link interfaces and within the RoI Builder.

## **4.0 Recommendations**

As a result of the integration tests with the MIROD and CPROD, the following points should be addressed in the design of the RoI Builder.

### **4.1 S-Link Interface**

#### **4.1.1 Input Buffer**

The Input card on the RoI Builder should be designed to buffer sufficient words after setting link full to allow the signal to reach the source ROD and also for the ROD to react to the link full condition. The former depends on the physical layer implementation while the latter depends on the ROD design. Having a large input buffer would help eliminate flow control signals being asserted during fluctuations in the readout time of the RoI Builder.

### **4.1.2 S-Link Reset**

The S-Link interfaces on both the Input and Output cards should have the capability to reset the link and should do so upon detection of an error and also be able to be reset under software control. Most S-Link implementations power on in a link down state and a reset is necessary on at least end to make the link operational. The ODIN G-Link implementation could not be tested in this integration since neither the ROD nor the RoI Builder had the ability to reset the interface.

## **4.2 Robustness**

### **4.2.1 Error handling**

The error recovery procedure of discarding entire events as a result of a time-out on a single channel should be rethought. When a time-out occurs it would be better to transfer the data which has been collected and indicate an incomplete event condition in a status word (see next section).

A check of the LIID should be done to ensure that each fragment has the same id. If not an error flag should be set.

### **4.2.2 Monitoring**

Both the input card and RoI processor cards should have status registers addressed from VME that indicate their state. Examples of states on the input card would be waiting for header, waiting for trailer and sending fragment to RoI processor. The RoI processors should tag similar states as well maintain a count of the fragments processed from each channel since the last clear operation.

## **4.3 Output record format**

The S-Link start and stop words delivered with each fragment should be stripped off before sending the assembled event record to the Level 2 supervisor. A header should be added which complies with the Atlas DAQ format. Status words should be added which indicate any errors detected in the event and also provide pointers to each of the fragments.

## **4.4 Hardware diagnostic aids.**

Test headers should be available to monitor important S-Link signals as well as signals which synchronize flow between the cards within the RoI Builder.

## 5.0 References

1. **C.Schwick**, *The MIROD documentation page*, <http://home.cern.ch/schwick/muctpi/mirod/mirod.html>
2. *Atlas First Level Trigger Prototype readout Driver*, <http://hepwww.rl.ac.uk/Atlas-L1/Modules/ROD/rod-spec-1-1.pdf>
3. *CERN S-Link Homepage*, <http://hsi.web.cern.ch/HSI/s-link/>
4. *Proposal for Integration of Level 1 with Dataflow* [http://edms02.cern.ch/tmpfiles/edms\\_tmp\\_893406\\_11proposal.pdf](http://edms02.cern.ch/tmpfiles/edms_tmp_893406_11proposal.pdf)