

Report on the Dataflow Integration Test of the Muon-CTP-Interface and the RoI Builder

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Abstract

This document reports on the integration test of the Muon-CTP-Interface and the RoI Builder carried out in the week of 29 January to 2 February 2001.

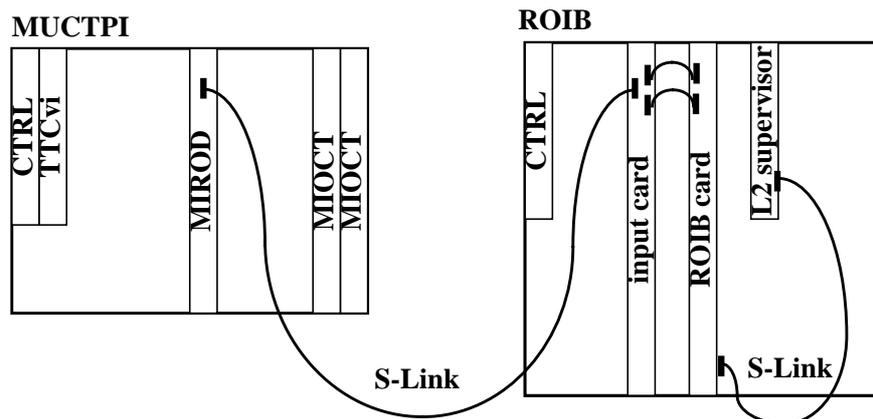
1 Introduction

Following the integration plans laid out in the Level-1 dataflow integration document [1] which has been presented in the ATLAS TDAQ week November 2000, the Muon-CTP-Interface (MUCTPI) [2] and the RoI Builder (ROIB) [3] system were integrated at CERN in the week of 29 January to 2 February 2001. The aim of the tests was to send RoI information from the MIROD module of the MUCTPI to the input card of the ROIB, through the ROIB card, and to a Level-2 supervisor. Understanding of the interface between the two systems, which is using S-Link [4], and testing of the performance and of the data integrity were the principle goals. The two systems were controlled and monitored by their respective test and diagnostic software. At this stage, no attempt was made at integrating the two systems with a common online software.

2 Test Setup

The setup which is schematically shown in figure 1 consists of the MUCTPI, the ROIB system, and some auxiliary equipment, including a TTCvi [5] module for timing and trigger signal generation, and a digital oscilloscope.

Figure 1: Schematic View of the Setup



The MUCTPI consists of the following modules:

- the 9U VME MUCTPI crate with a dedicated backplane (MIBAK);
- one MIROD [6] module which on each L1A receives data from the MICTP and all MIOCT modules, formats them to the ATLAS event format [7] and sends event data and RoI fragments to the data acquisition and the ROIB, respectively; the MIROD module can also generate data internally;
- two MIOCT [8] modules which receive data from the muon trigger sector logics.; in absence of the sector logics data can be generated internally; one of the MIOCT modules can be programmed to emulate the data that in the final system would be sent by the MICTP module; the MICTP module is currently under design;
- dummy MICTP cards for timing signal distribution and dummy MIOCT cards to charge the MIBAK backplane correctly;
- a VME single-board computer from CES [9], a RIO2 8061, which controls and monitors the MUCTPI.

The ROIB system consists of the following modules:

- the 12U VME ROIB crate;
- an input card; two types of input cards exist: the old input card does not have external input but can generate data internally; the new input card can use S-Link inputs or generate data internally;
- one ROIB card which receives the data from the input card, forms complete RoIs and sends them to the Level-2 supervisor(s);
- a VME single-board computer from CES [9], a RIO2 8062, which acts as Level-2 supervisor;
- a VME single-board computer from CES [9], a RIO2 8062, which controls and monitors the ROIB system.

The MIROD's Level-2 S-Link output is connected to an S-Link input on the input card. The two identical outputs of the input card are connected to the ROIB card. The ROIB card needs at least two RoI fragments in order to work correctly. Since the RoI fragments and thus the Level-1 identifiers are identical, the building of the RoI is straightforward. The output of the ROIB card is connected by S-Link to the Level-2 processor. All S-Links use the implementation on cable developed at Argonne National Laboratory.

Both systems are controlled and monitored by test and diagnostic software which runs on the VME single-board computers. These computers run the LynxOS operating system and are connected to a TCP/IP local area network.

3 Results

3.1 Stand-alone Tests MUCTPI & ROIB

After installing the equipment in building 594, stand-alone functional tests of the MUCTPI and of the ROIB system were carried out.

The MUCTPI was tested in stand-alone mode with RoI fragments generated from data in internal memory of the MIROD module. The RoI fragments were read out directly at the FPGA driving the S-Link output. Fixed RoI fragments can be sent this way at a frequency which can be tuned between 2 Hz and about 1 MHz. Alternatively, data can be generated in the MIOCT modules. One of the MIOCTs, in this case, has to emulate the data which in the final system will come from the MICTP module. The MICTP module is currently under design. The data generation in the MIOCT modules is triggered by an L1A signal which is generated in a TTCvi module. The TTCvi generates exponentially distributed L1As with a few selectable rates ranging from 1 Hz up to 100 kHz. Due to the emulation of a MICTP module, the RoI fragment sent to the ROIB has the Level-1 identifier and BC identifier mismatch error flags set.

For the ROIB system's stand-alone tests, RoI fragments were sent from memory in the old input card to the ROIB card using two identical inputs, and from there to the Level-2 supervisor. The maximum frequency the ROIB system can sustain was measured to be 100 kHz. This rate was reduced to 60 kHz when the Level-2 supervisor verified the data. The same results were obtained using the new input card and a RIO2 with an S-Link output as source of the RoI fragments. In the last test it was found that one bit (bit 21) of the data was stuck at zero but this did not prevent the RoI fragments from being passed through the ROIB system correctly.

3.2 Single-RoI Tests MIROD → ROIB

When the S-Link output of the MIROD was connected to an S-Link input of the input card, no data arrived at the ROIB card at first. The problem was tracked down to a timing problem on the FIFOs on the input card which receive the S-Link data. The problem was documented in several timing diagrams and discussed with the experts at Argonne National Laboratory. A short-term work around was found: the continuously running clock on the S-Link can be delayed by a cable loop. This allows the RoI fragments sent by the MIROD to be received correctly at the input card.

With this work-around RoI fragments were sent by the MIROD and verified by the Level-2 processor. The data verification was done with a test program running on the Level-2 supervisor. It took as input a dump from the MIROD Level-2 output and compared it to the data coming from the ROIB card. Two bits seem to be stuck on the input card: bit 21 and bit 25. They were masked out for these tests, as they are not vital for the functioning of the protocol. Apart from the two bits stuck at zero the data verification showed no other problem.

3.3 Continuous Tests MIROD → ROIB

RoI fragments were sent continuously from the MIROD to the ROIB at increasing frequency. The data integrity and the correct functioning of the flow control were checked. Settings from about 2 Hz to a maximum speed of about 1 MHz can be chosen on the MIROD. For these test the flow control was taken into account by the MIROD. The results of the data verification with RoI fragments from the MIROD are summarized in table 1.

Table 1: Continuous tests MIROD → ROIB

Attempted Rate [kHz]	Data Verification
10	ok
20	ok
30	ok
40	ok
80	ok
100	ok

At 80 kHz the Level-2 S-Link busy signal came on already quite frequently on the MIROD, indicating that the RoI fragments were not picked up fast enough by the ROIB. The bottleneck, however, was the program running on the Level-2 supervisor performing the data verification before polling the next RoI. After switching off the verification, the Level-2 supervisor could poll RoIs every 8 us, allowing the MIROD to send RoI fragments at a rate of up to 125 kHz.

Also important was the check of the flow control. Stopping the readout of the ROIB card resulted in the Level-2 S-Link busy signal to become active and stop the MIROD, as expected. After starting the readout again, the MIROD resumed sending RoI fragments without any problem. In cases when the S-Link was saturated, the MIROD stopped and resumed immediately when the S-Link was free again. Since no problems were observed with the control words in the case the busy signal went on and off, the conclusion is that no words are lost. As all RoI

fragments sent from the MIROD have the same Level-1 identifier, entire fragments to be lost cannot not be noticed. However, this is considered to be an unlikely coincidence, especially since the RoI fragment size was also varied in other tests and no fragments were lost.

3.4 Continuous Tests MIOCT → ROIB

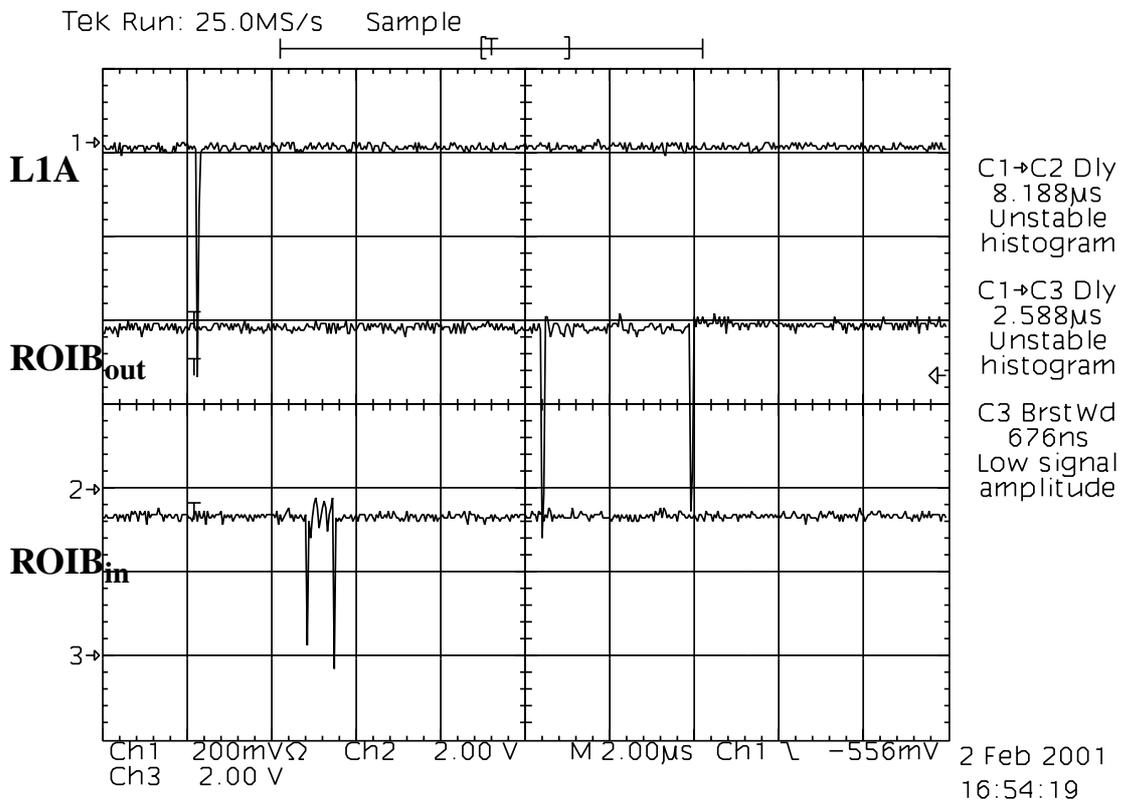
Data was generated internally in the MIOCT modules, collected by the MIROD and RoI fragments send to the ROIB. The L1A signal was generated using the random trigger of the TTCvi module. After setting up this configuration it was verified that the RoI fragments arrive correctly at the Level-2 supervisor. The tests described in section 3.3 were not repeated in detail, as from the point of view of the ROIB nothing actually changed.

3.5 Latency Measurements

Using the configuration described in section 3.4 the latency of the system was measured as a function of the L1A frequency and the RoI fragment size. The following three points in the system were monitored by one channel each of the digital oscilloscope:

1. the L1A signal from the output of the TTCvi trigger;
2. the S-Link control bit (#LCTRL, pin 19) on the S-Link input of the input card (ROIB_{in});
3. the S-Link control bit (#UCTRL, pin 19) on the S-Link output of the ROIB card (ROIB_{out}).

Figure 2: Latency Measurement



The latency was first measured for 12 candidates in the RoI fragment with L1A frequencies ranging from 1 kHz to about 50 kHz. No significant changes in the latency were observed (see below). Figure 2 shows a dump of the scope. In the dump the upper line (first in time) shows

the L1A signal, the second line (last in time) shows the ROIB_{out}, and the lower line shows the ROIB_{in}. The latter two have two signals each, representing the begin-of-block and the end-of-block control signal of the S-Link protocol. The two signals are closer for the ROIB_{in} than for the ROIB_{out}, since the first contains only one RoI fragment and is clocked with the 40 MHz clock from the MIROD, while the latter contains two (identical) RoI fragments and runs with the slower 15 MHz (???) clock of the ROIB.

Secondly, the latencies for RoI fragments with 12, 6, 1 and 0 candidates were measured. Results are summarized in table 2. The latencies given are averages read from the scope. Actual values were usually fluctuating by a few tenths of μs .

Table 2: Latency Measurements

# Candidates	# Data Words	L1A \rightarrow ROIB _{in} [μs]	L1A \rightarrow ROIB _{out} [μs]
12	27	2.6	8.2
6	21	2.6	8.0
1	16	2.6	7.9
0	15	2.6	7.9

4 Conclusion

The goals of the integration of MUCTPI and ROIB were achieved. All participants thought that the integration test was very useful and that a much better understanding of the interface between the Level-1 and the Level-2 system was achieved. Rates of RoI fragments sent from the MUCTPI to the ROIB up to 100 kHz could be sustained. The flow control on the interface works correctly. The data were verified to be correct at the Level-2 supervisor. The latency from an L1A to the RoI fragment being sent to the ROIB input card is about 2.6 μs . The latency from an L1A to the complete RoI containing two identical RoI fragments being sent to the Level-2 supervisor is about 8 μs .

A timing problem on the ROIB input card was identified and temporarily fixed. The input card is now back at Argonne National Laboratory where the experts are looking into the possibility of a permanent fix of the timing problem. The ROIB crate stays for the time being in building 594. It is possible that the modified input card will come back at a later time and that the tests will be continued.

References

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