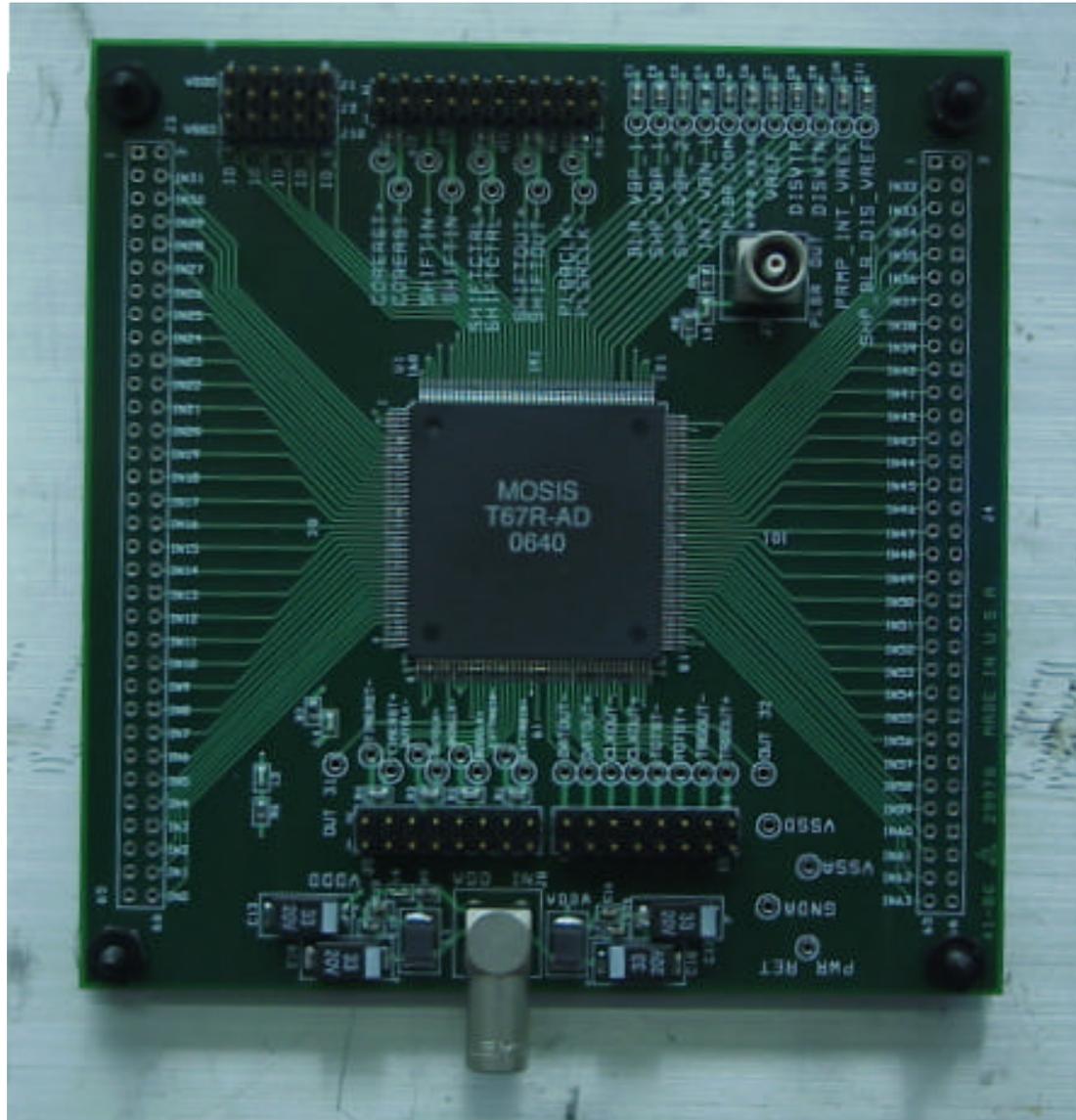


Testing & Status of DCAL2

**Gary Drake & Jose Repond
Dec. 20, 2006**

DCAL2 Test Board



Tests Done So Far:

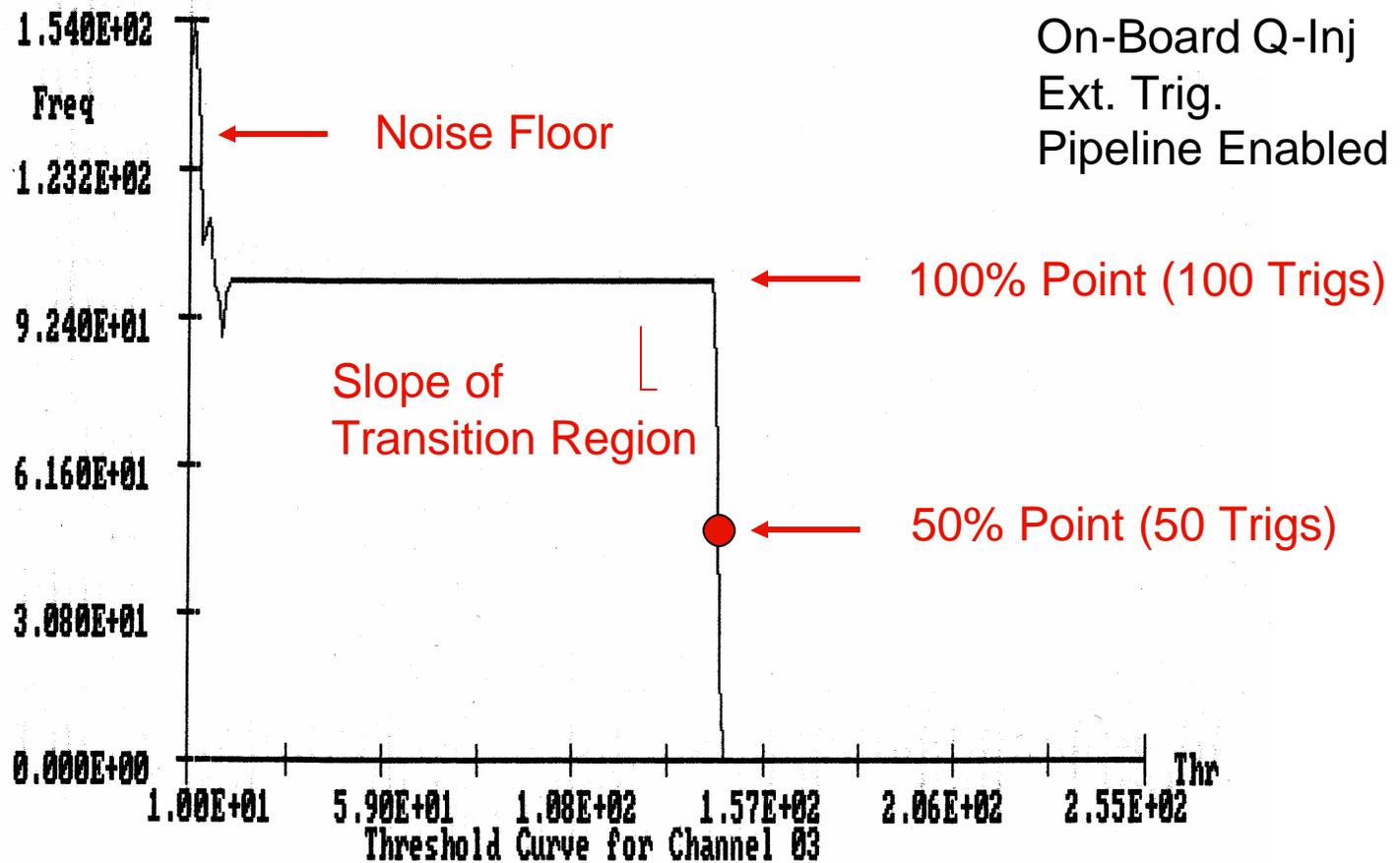
- Register Read/Write Tests
- Test of Pipeline w/ Ext. Trigger
- Threshold Tests using On-Board Q-Inj – High-Gain Channel
- Threshold Tests using On-Board Q-Inj – Low-Gain Channel
- Tests of Noise Floor

Register Tests:

- Check Address: R/W to All Addresses,
Read Correct Data for Selected Address
No Response for All Other Addresses
- R/W 1's thru field of 0's: 00000001
00000010...
- R/W 0's thru field of 1's: 11111110
11111101...
- R/W Marching 1's: 00000001
00000011...
- R/W Marching 0's: 11111110
11111100...

→ **Results: Chip Works Perfectly when Address Lines left Floating (ADR=0)
Having Problems for Other Addresses
May be Problem on Test Board...**

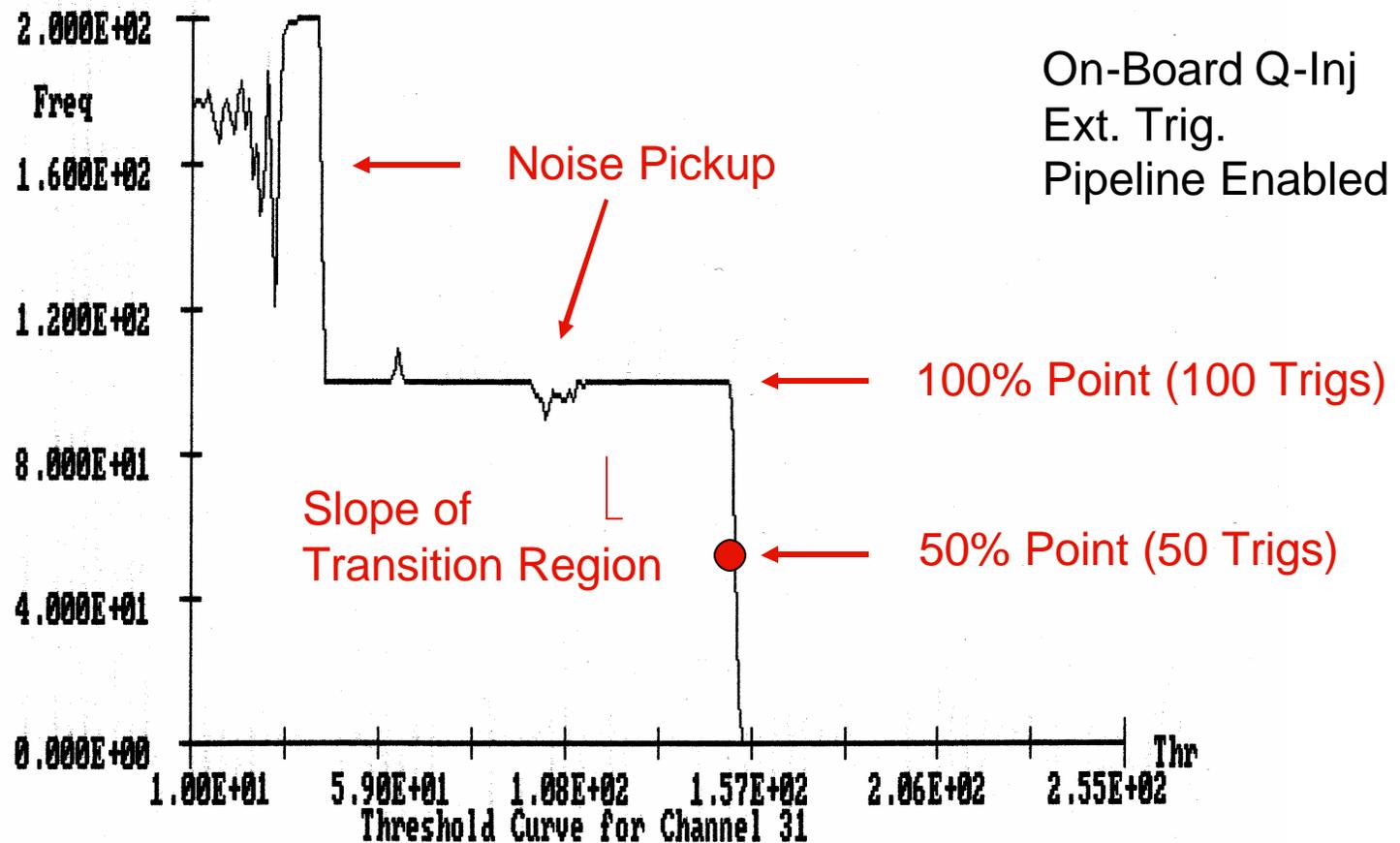
Threshold Response Tests Typical Channel (DAC=192, High-Gain)



Threshold Response Tests

Channel with Issues (Ch31 & Ch32)

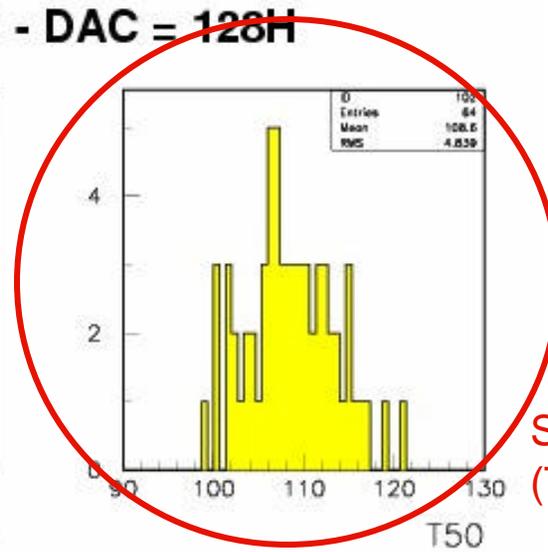
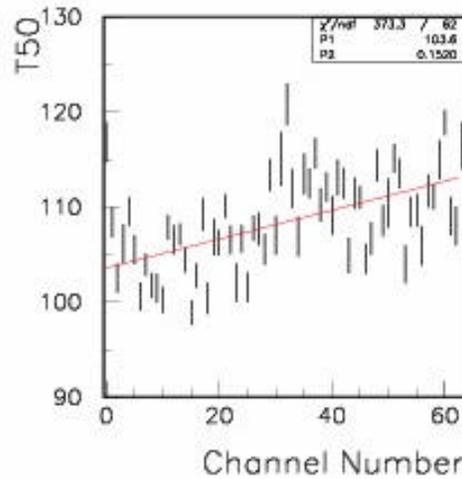
(DAC=192, High-Gain)



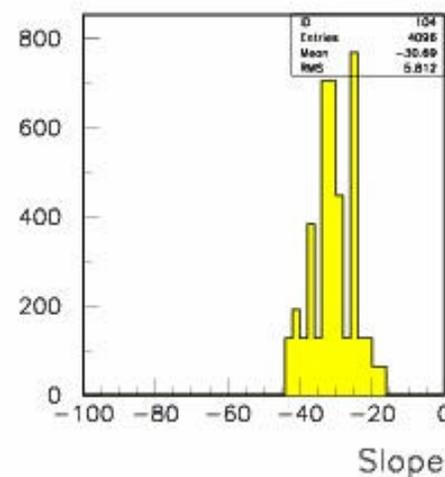
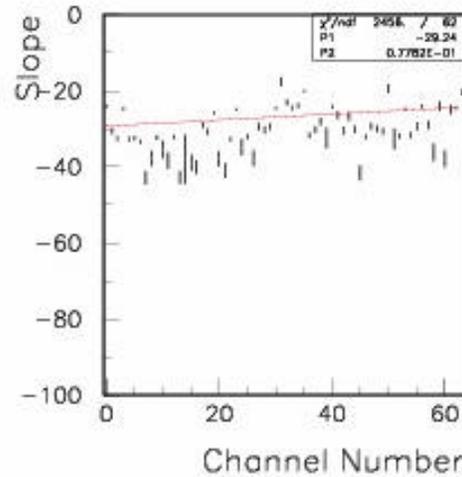
→ Ch 31 & 32 Have Test Points
Brought to External Pins of Chip
Which May Be the Cause...

Threshold Response Tests Summary for All Channels (DAC=128, High-Gain)

DCAL 2.1 - DAC = 128H

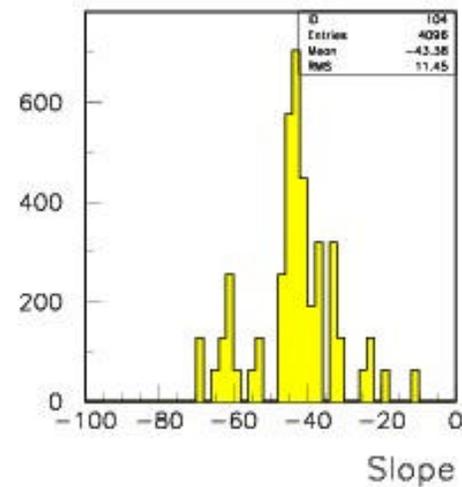
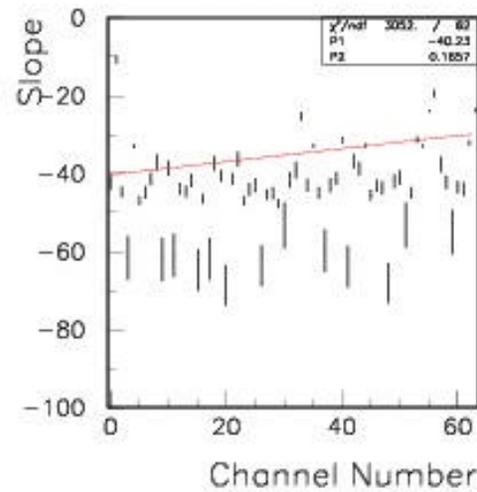
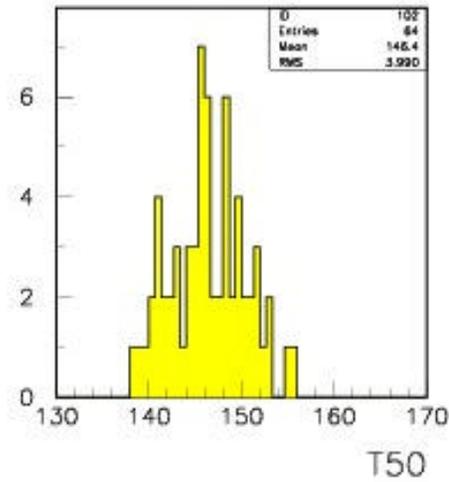
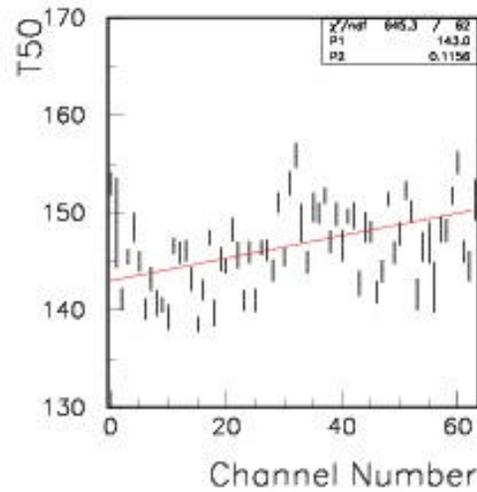


Spread ~20 DAC Cnts
(Typically ~10-15 Cnts)



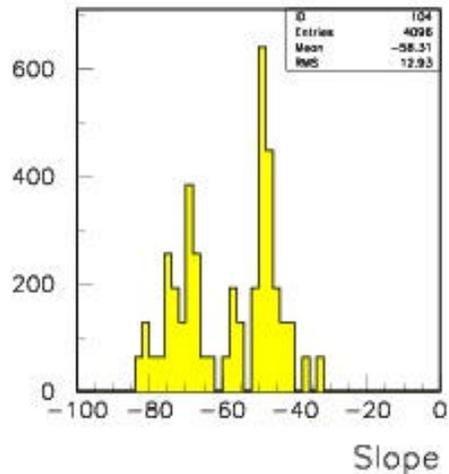
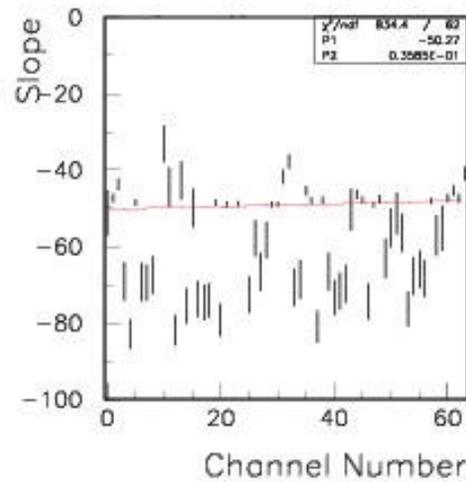
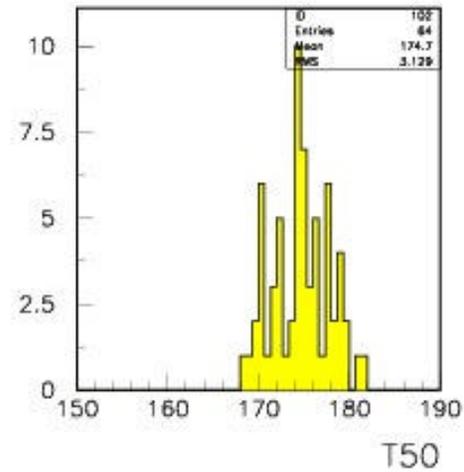
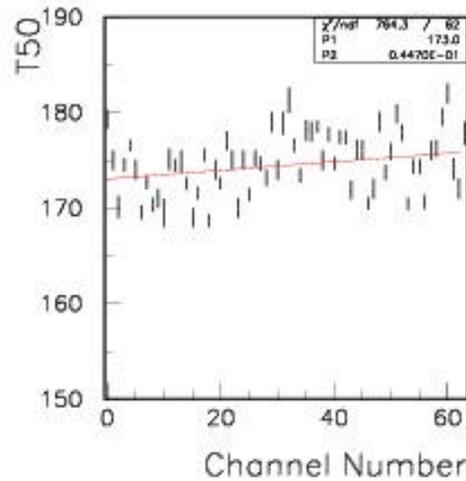
Threshold Response Tests Summary for All Channels (DAC=192, High-Gain)

DCAL 2.1 - DAC = 192H



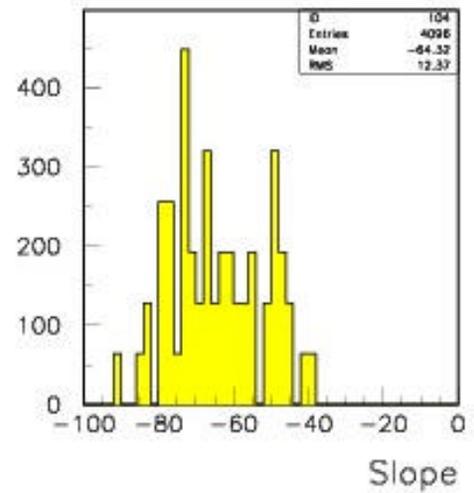
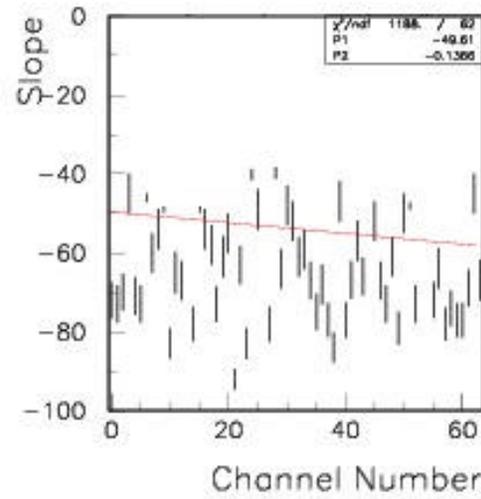
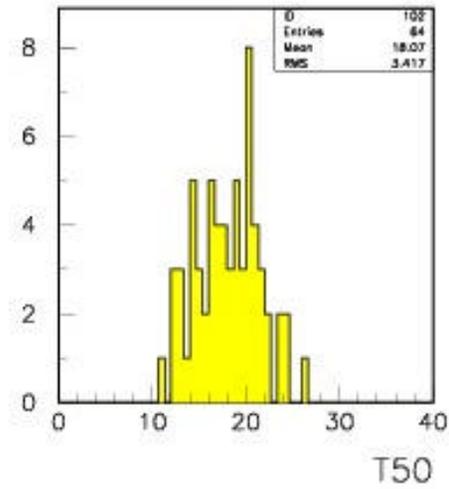
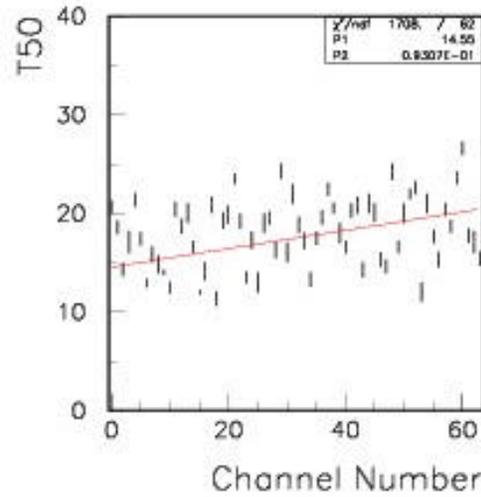
Threshold Response Tests Summary for All Channels (DAC=255 (FS), High-Gain)

DCAL 2.1 - DAC = 255H



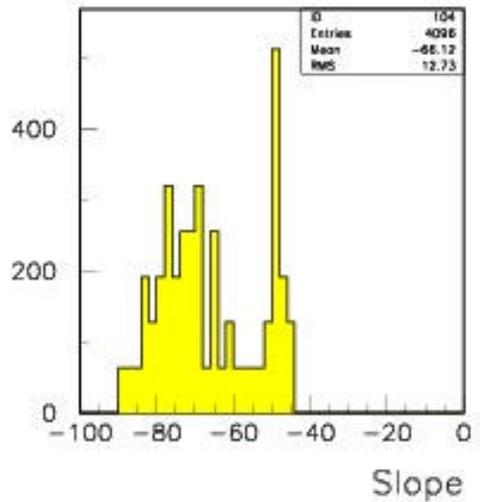
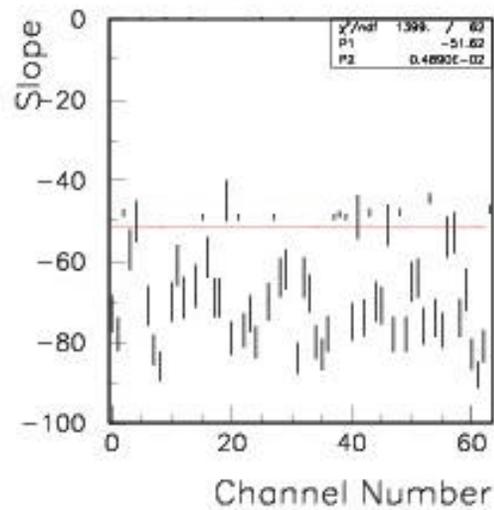
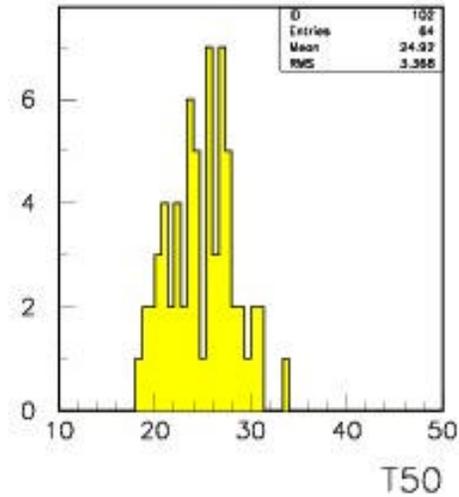
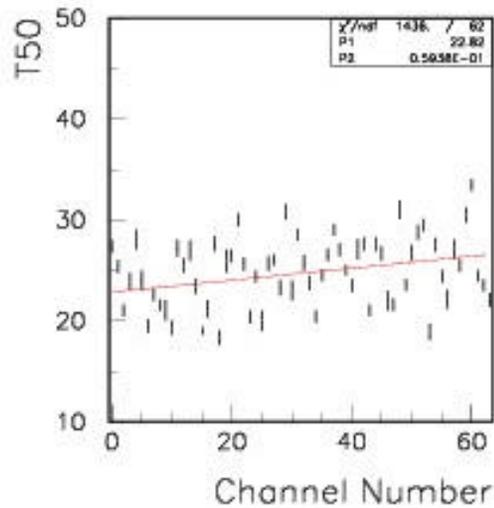
Threshold Response Tests Summary for All Channels (DAC=128, Low-Gain)

DCAL 2.1 - DAC = 128L



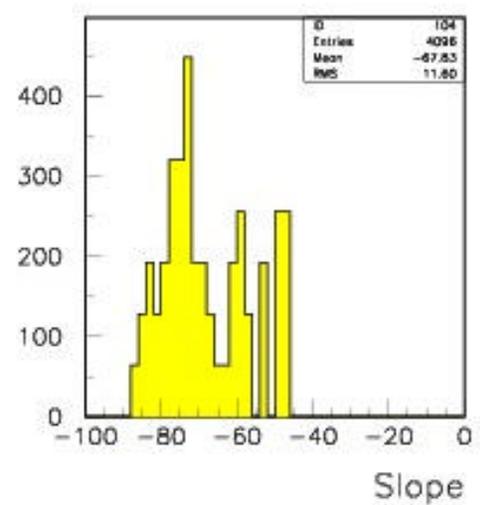
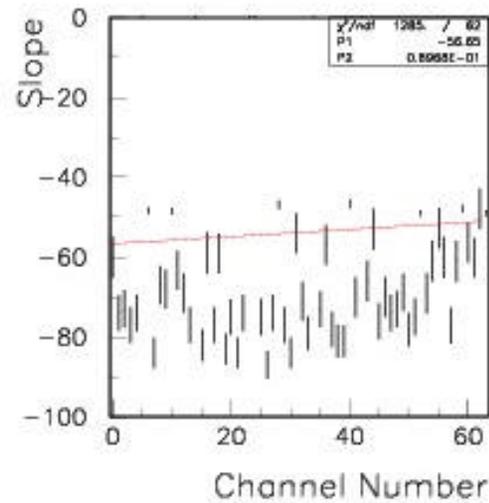
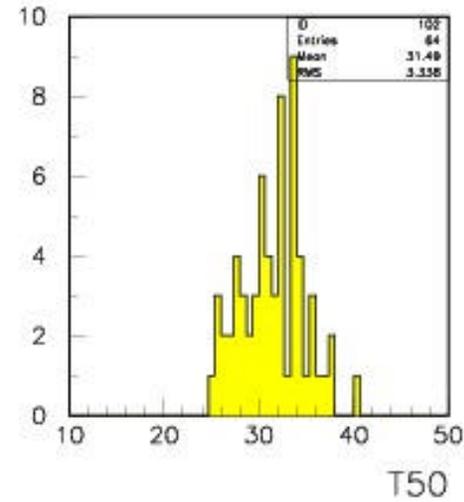
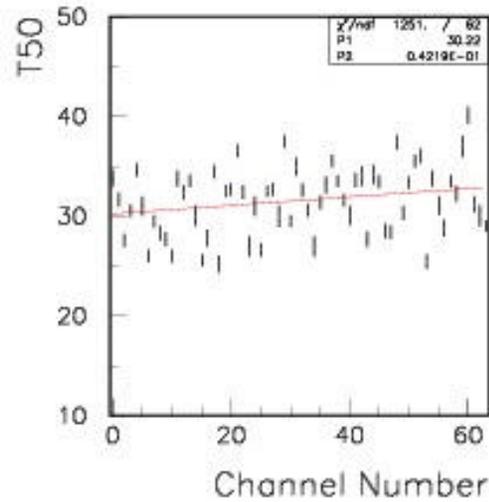
Threshold Response Tests Summary for All Channels (DAC=192, Low-Gain)

DCAL 2.1 - DAC = 192L



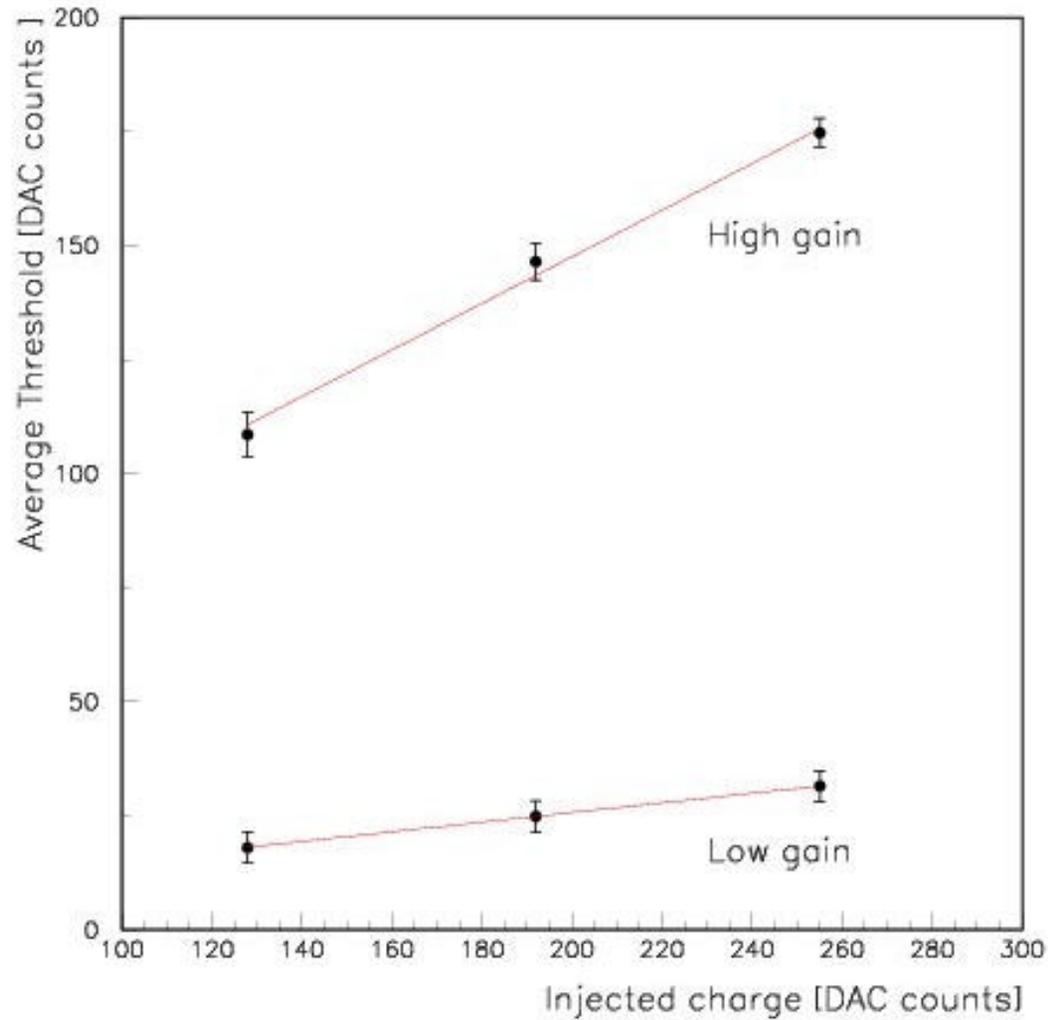
Threshold Response Tests Summary for All Channels (DAC=255 (FS), Low-Gain)

DCAL 2.1 - DAC = 255L



Threshold Response Tests Summary for All Channels

DCAL 2.1



Slope Ratios:

~ 5.5

Expected:

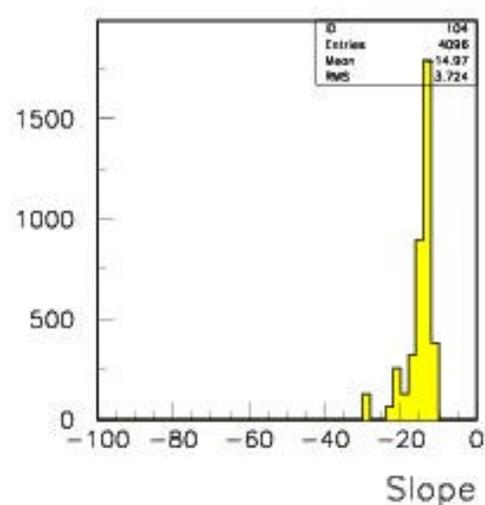
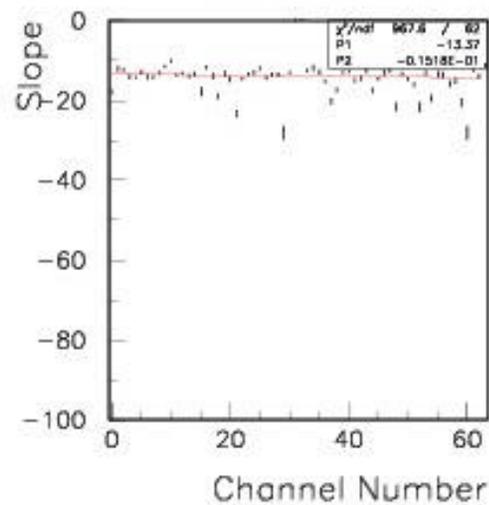
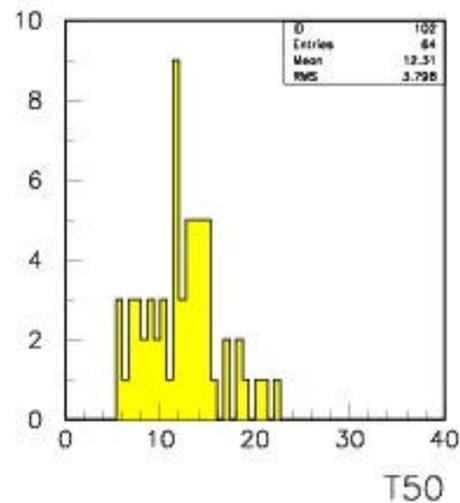
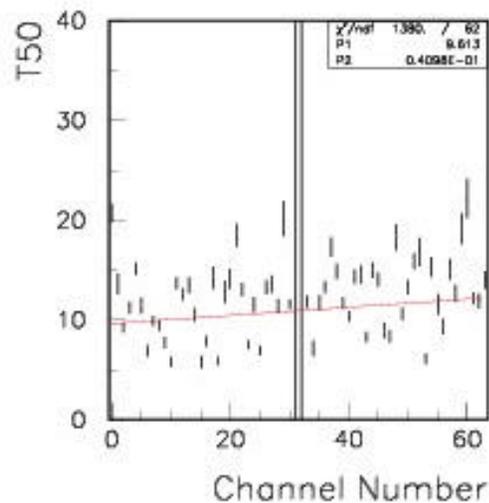
~ 8.4 pF / 1.5 pF

= 5.6

$C_{QINJ} = 160$ fF

Noise Floor Tests Summary for All Channels (High-Gain)

DCAL 2.1 - Noise floor



Summary

- Chip is Mostly Working!
- 2 Minor Problems Remain:
 - Chip Addressing Not Understood
 - Noise Pickup on Ch31 & CH32
- Tests Yet to Do:
 - Low-Gain Noise Floor
 - External Charge Injection
 - Tests with Self Trigger
 - Look for Digital Noise Pickup