



# *DHCAL Back-End*

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# DCOL Status



- PCB Design underway. Wu estimates can send out for fabrication in < 3 weeks.
- Several minor specification issues under discussion:
  - Data to front-end as spec'd (width encoded)
  - Return data should be un-encoded binary
- Hit sorting will be done in DCOL
  - DCAL chips must be read in consistent order by Data Concentrator
  - A distinctive indicator must be sent when all DCAL chips are empty (can be “link idle”)



## DCOL Status (cont.)



- 5V will be sent to FE to power links via local 3.3V regulator
- Test pulse will be synchronized to start of 100ns frame on front-end link
- Open Issues:
  - Trigger module interface has some open questions... but we don't have a designer for this yet. Probably don't need it for the vertical slice test.



# Software Issues



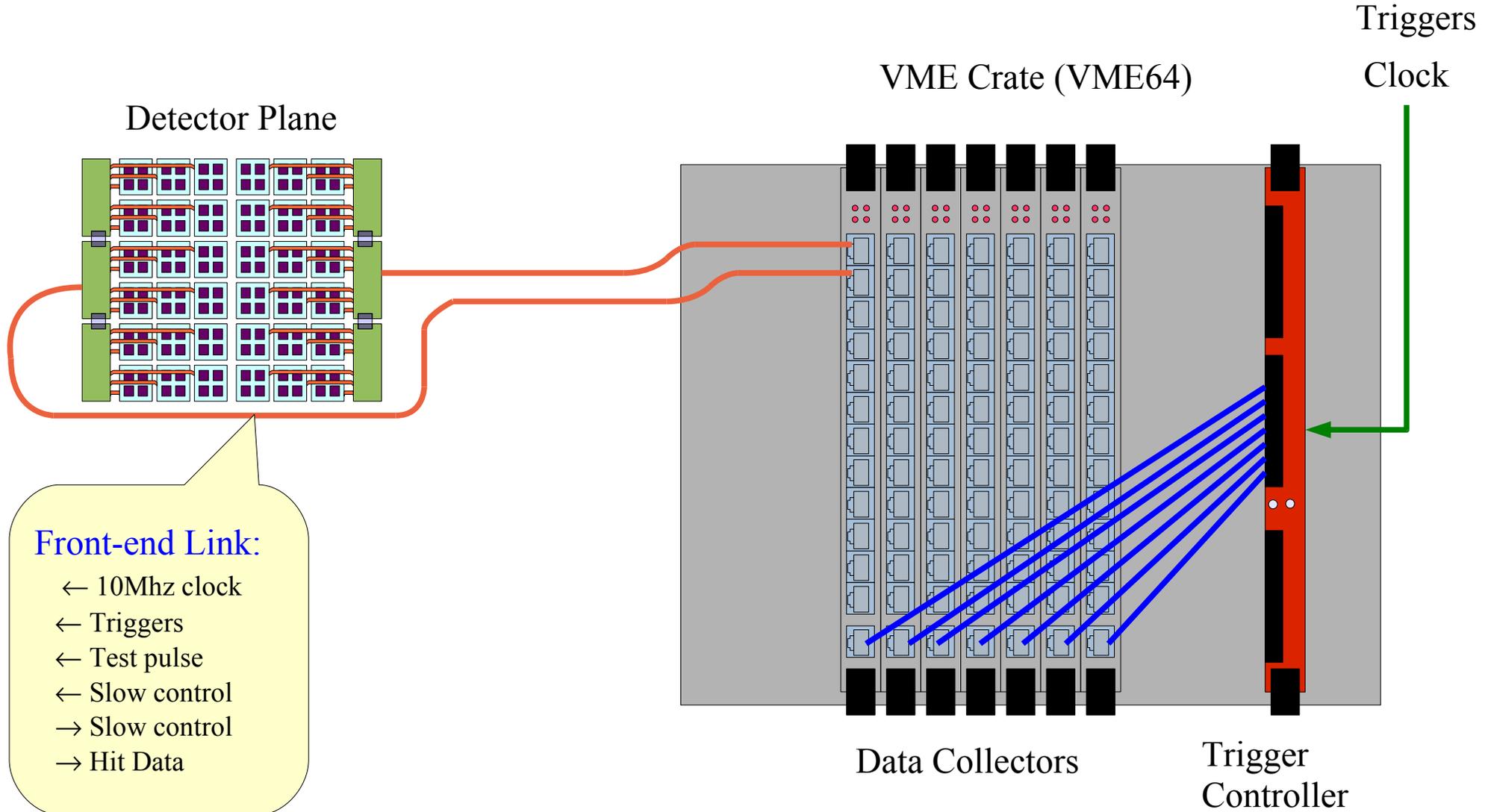
- BU “spare” PCI/VME bridge re-claimed by our CMS colleagues :(
  - We have one for our own use, but no extra
- Have requested register map from Wu for DCOL... hope to have it “soon”!
- I'm happy to participate in discussions about using HAL, etc when a system is set up at ANL



## Backup Slides



# Readout Overview

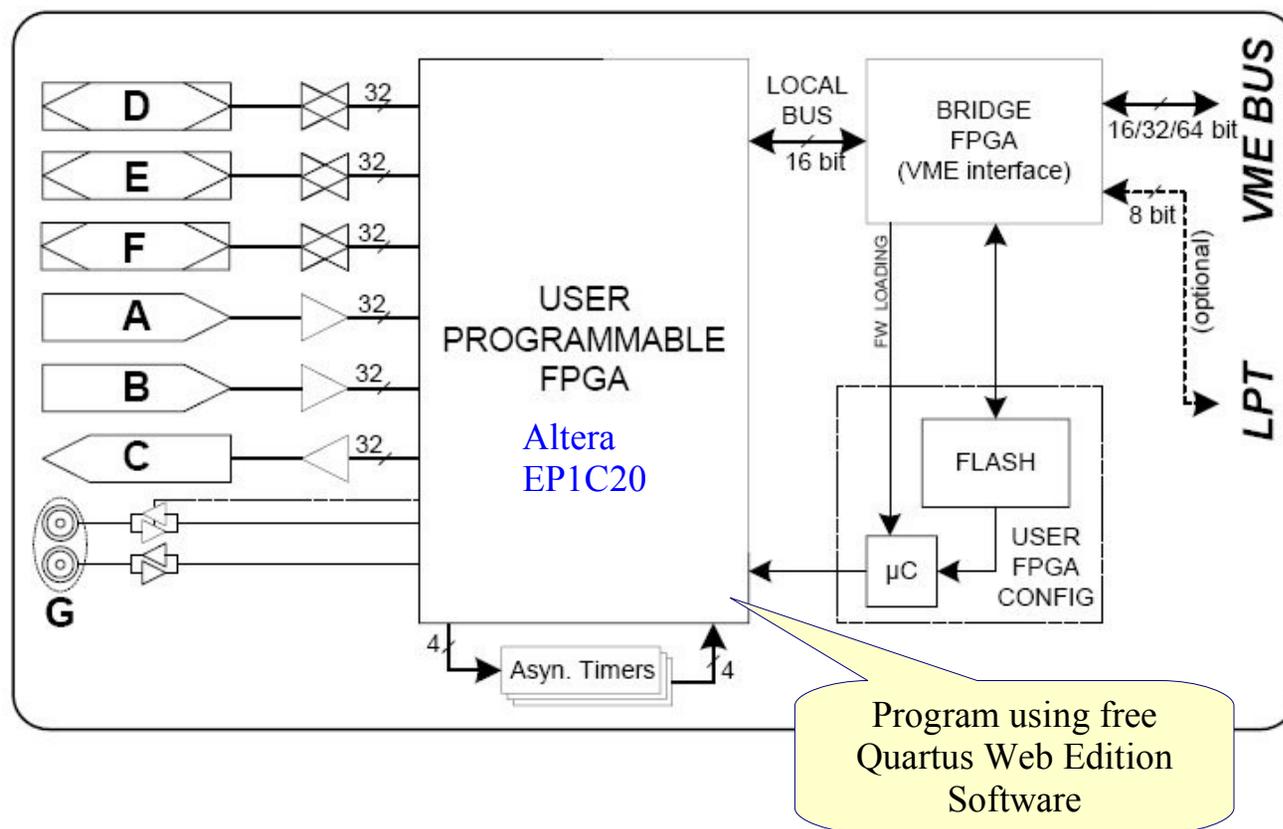
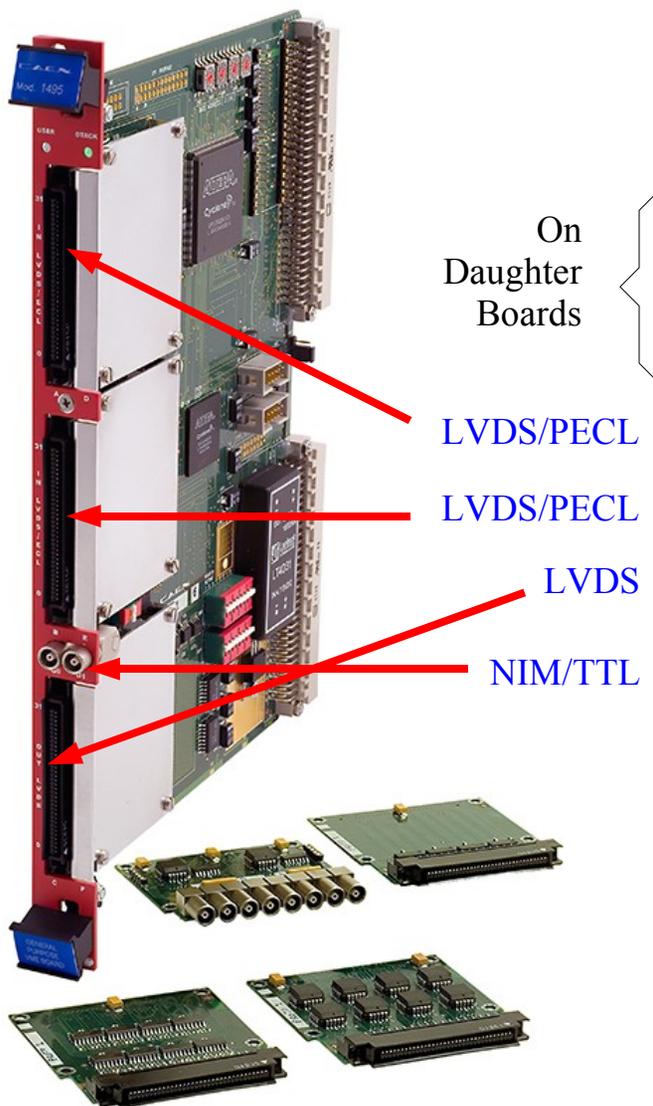




# Trigger Module - Candidate Hardware



- CAEN V1495 General-Purpose VME Module



This thing is in production  
One unit could be obtained for evaluation quickly  
Price: \$3400 (cheaper than custom design)