



DHCAL Back-End

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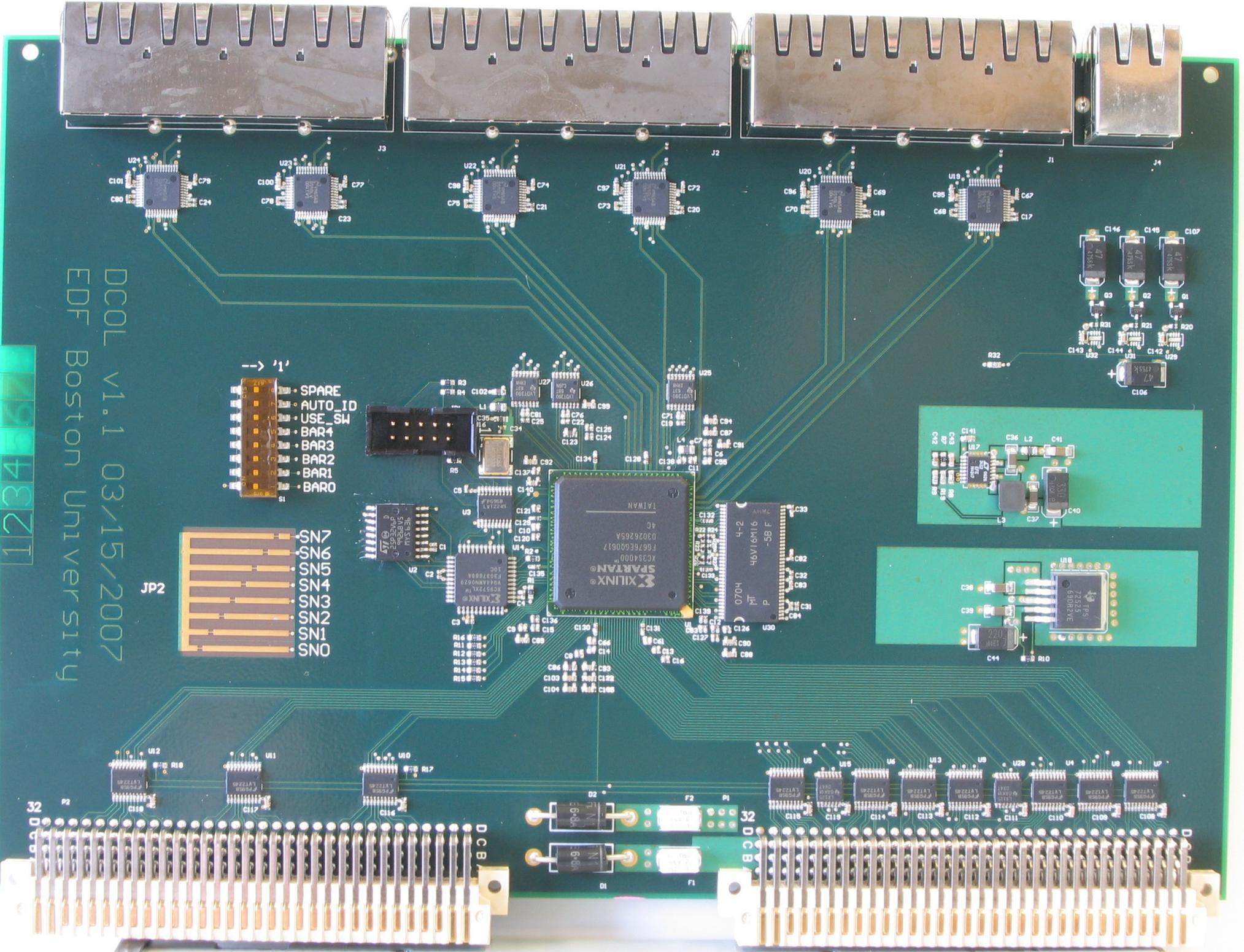
DCOL Status



- 3 Boards Stuffed - hardware tested and working
- Preliminary firmware released
- Testing underway at ANL and Boston
- Still missing:
 - Current-limiting chips for front-end links
 - Front panels

1234567

DCOL V1.1 03/15/2007
EDF Boston University



- SPARE
- AUTO_ID
- USE_SW
- BAR4
- BAR3
- BAR2
- BAR1
- BAR0

- SN7
- SN6
- SN5
- SN4
- SN3
- SN2
- SN1
- SNO



Firmware Status



- What is still missing
 - Only “Circular buffer mode” implemented
 - No sorting by timestamp
 - No monitoring counters
 - We should specify what we want!
- What has been tested (superficially)
 - SDRAM memory test
 - Flash programming from VME
 - Front-end link
 - Slow control write/read
 - Hit data read



Next Steps - Hardware



- Reproduce BU link tests at ANL
- Further link tests with Xilinx board
- Integrate DCOL with DCON
- Integrate DCOL with TTM
- Update/fix DCOL firmware as needed