DHCAL Readout Back End

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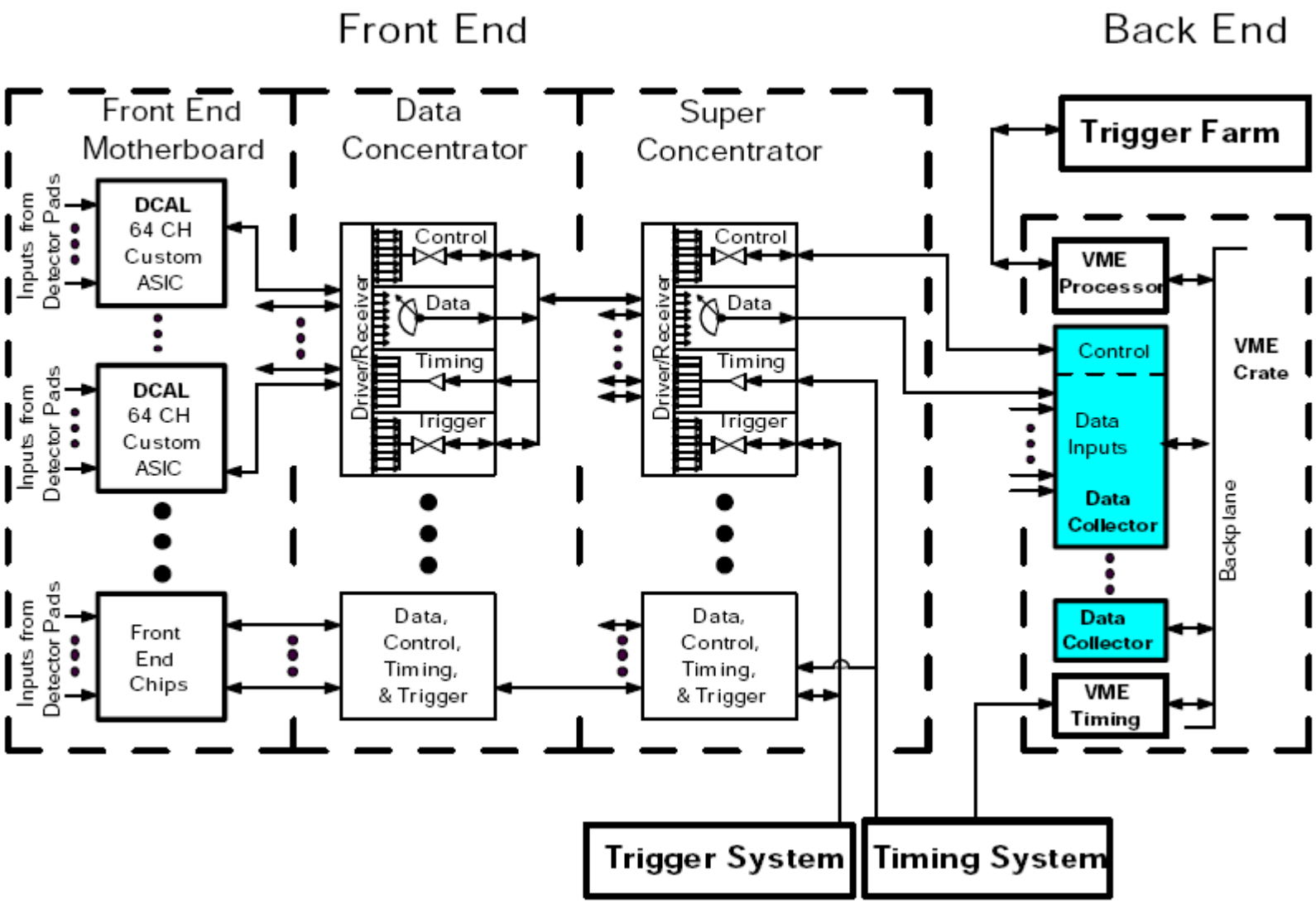
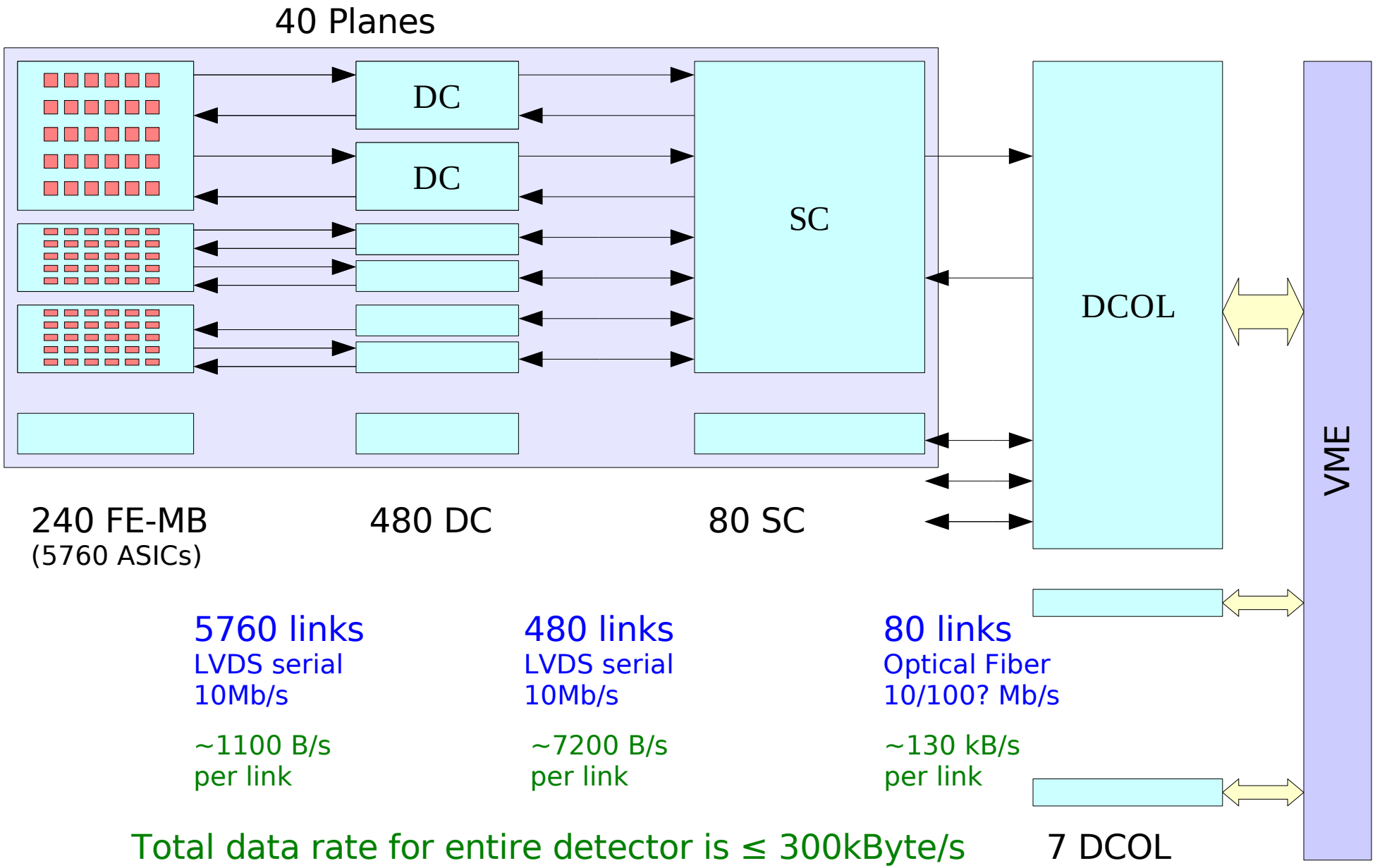
DHCAL Readout

Diagram from Proposal



DHCAL Data Paths

From Proposal



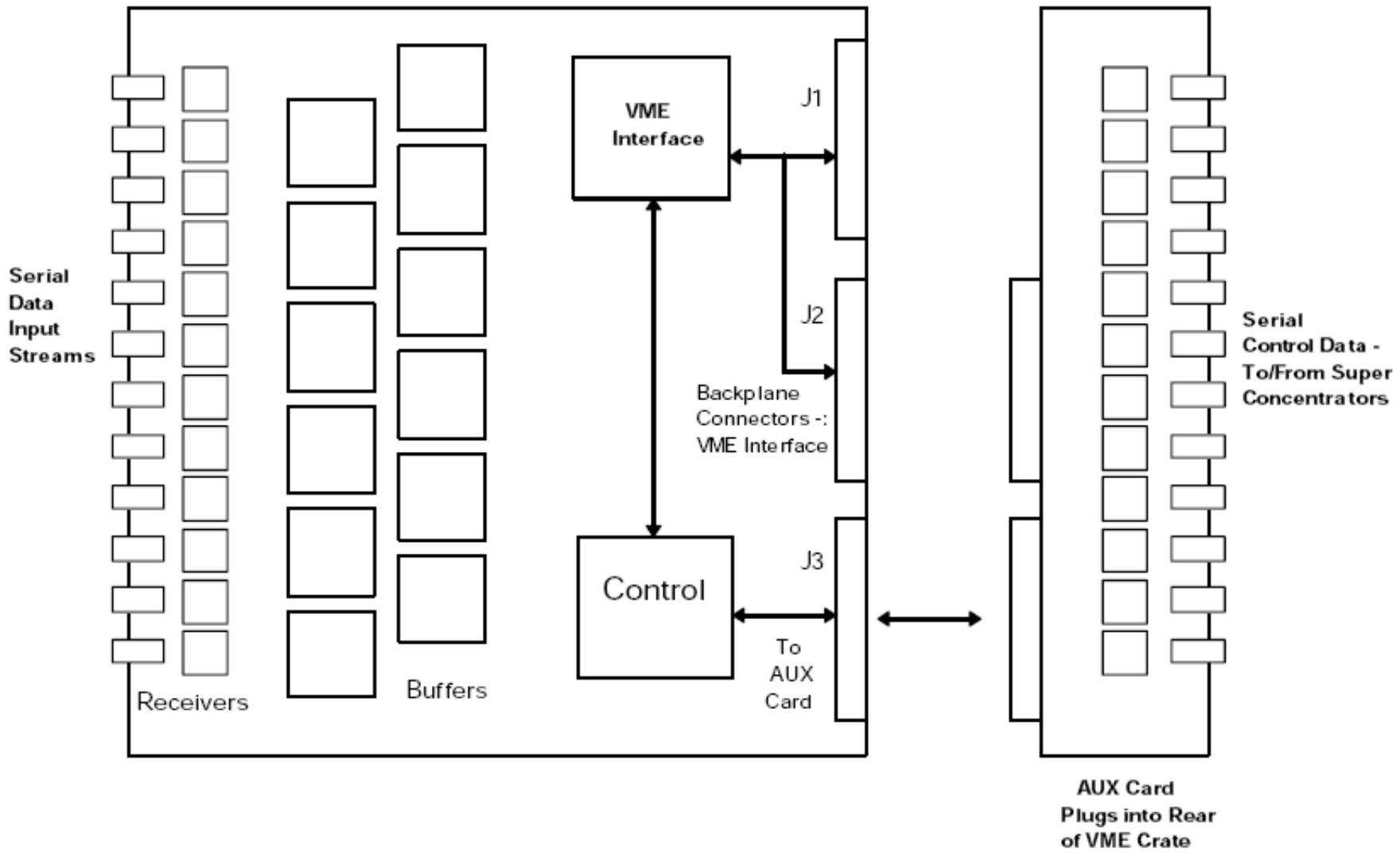
Total data rate for entire detector is ≤ 300kByte/s

DHCAL Data Collector

- Requirements (as I understand them!):
  - Receive 12 optical links from SC at (10 or 100?) Mbit/sec each
  - Transmit/fanout clock, timing, trigger signals to 12 SC and read back control/monitor data
  - Build events and (double) buffer for VME readout
- This seems at first glance a straightforward digital design which would be very similar to our work for CMS, DØ and other projects

Data Collector

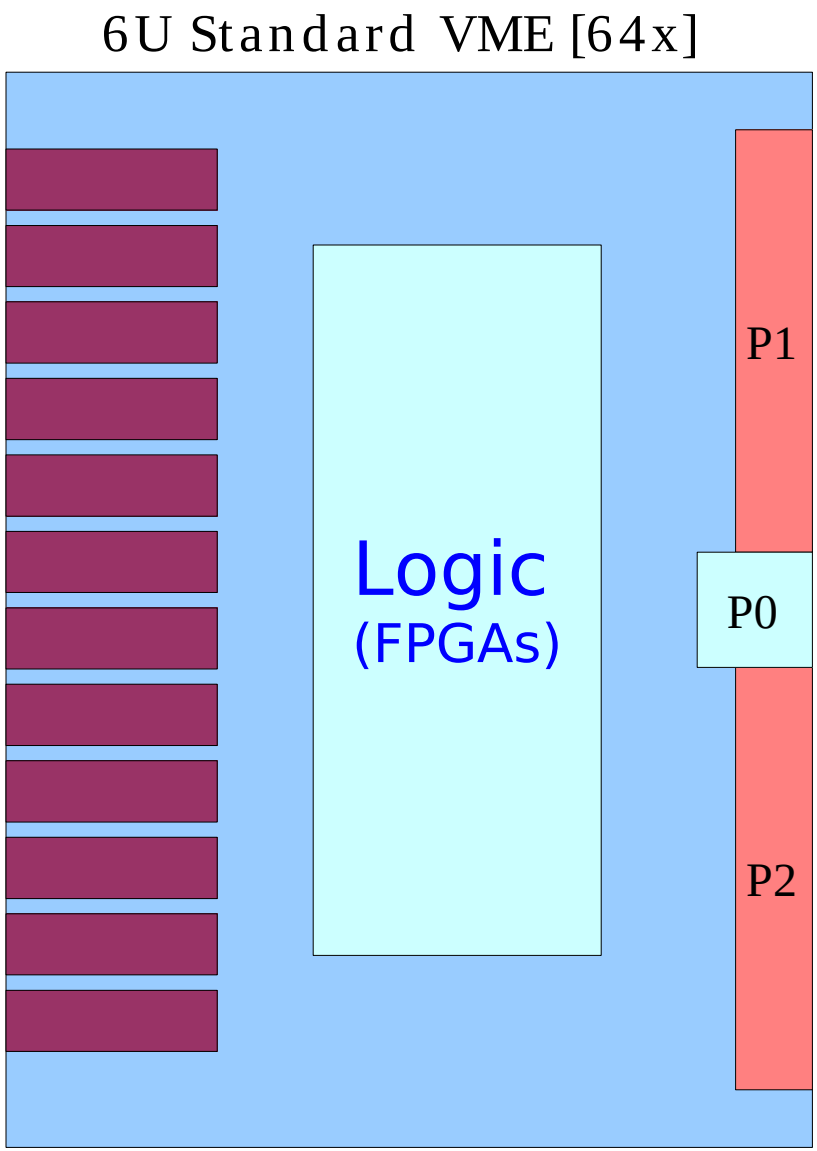
Diagram from Proposal



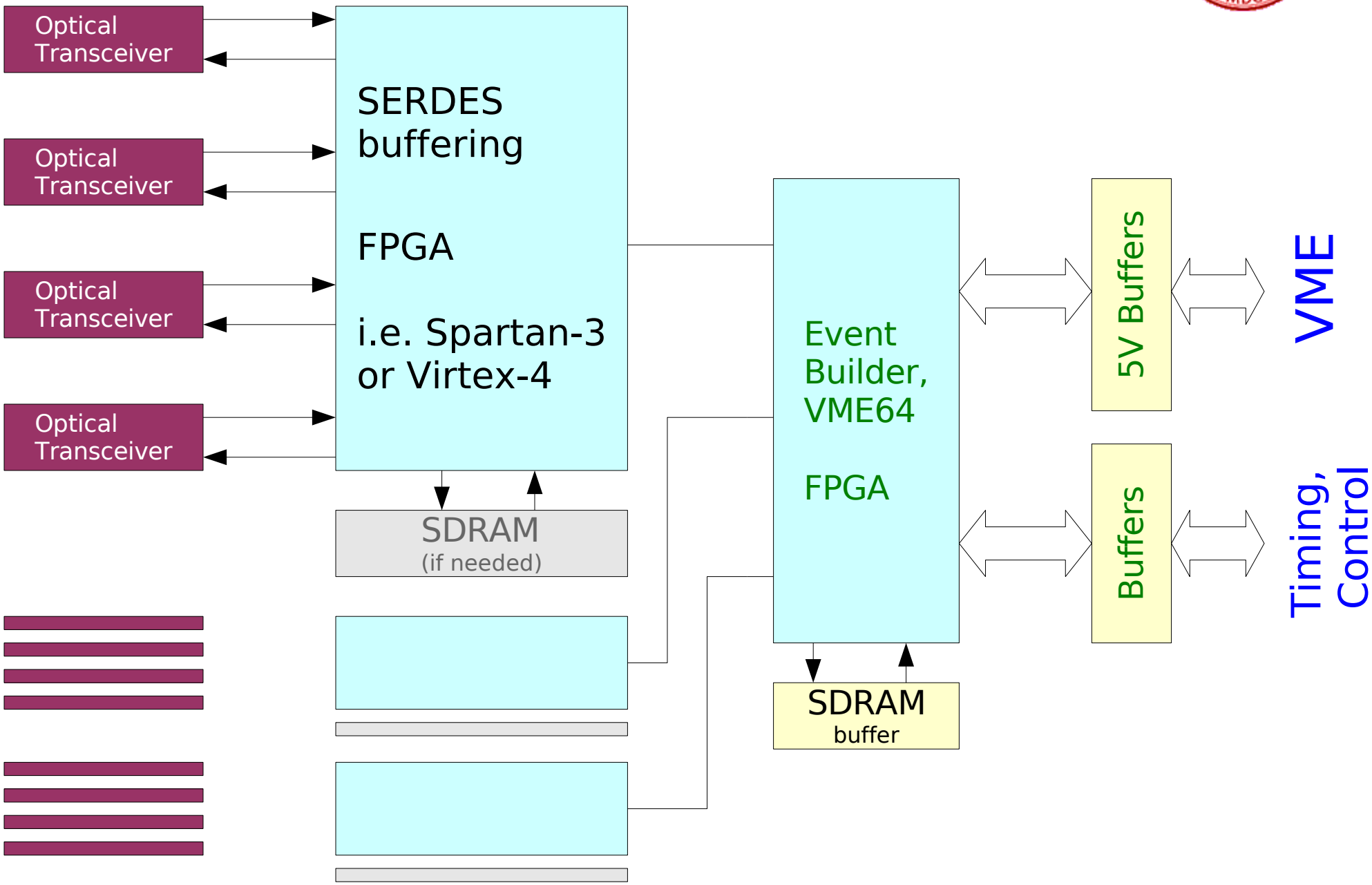
DCOL Alternative 1

6U VME, no transition module

- 12 SFF (dual LC) optical transceivers fit on FP
- Rx for data; Tx for ctrl: could use one duplex LC fiber to each SC
- Plenty of room for other stuff if done in FPGAs



DCOL Alternative 1

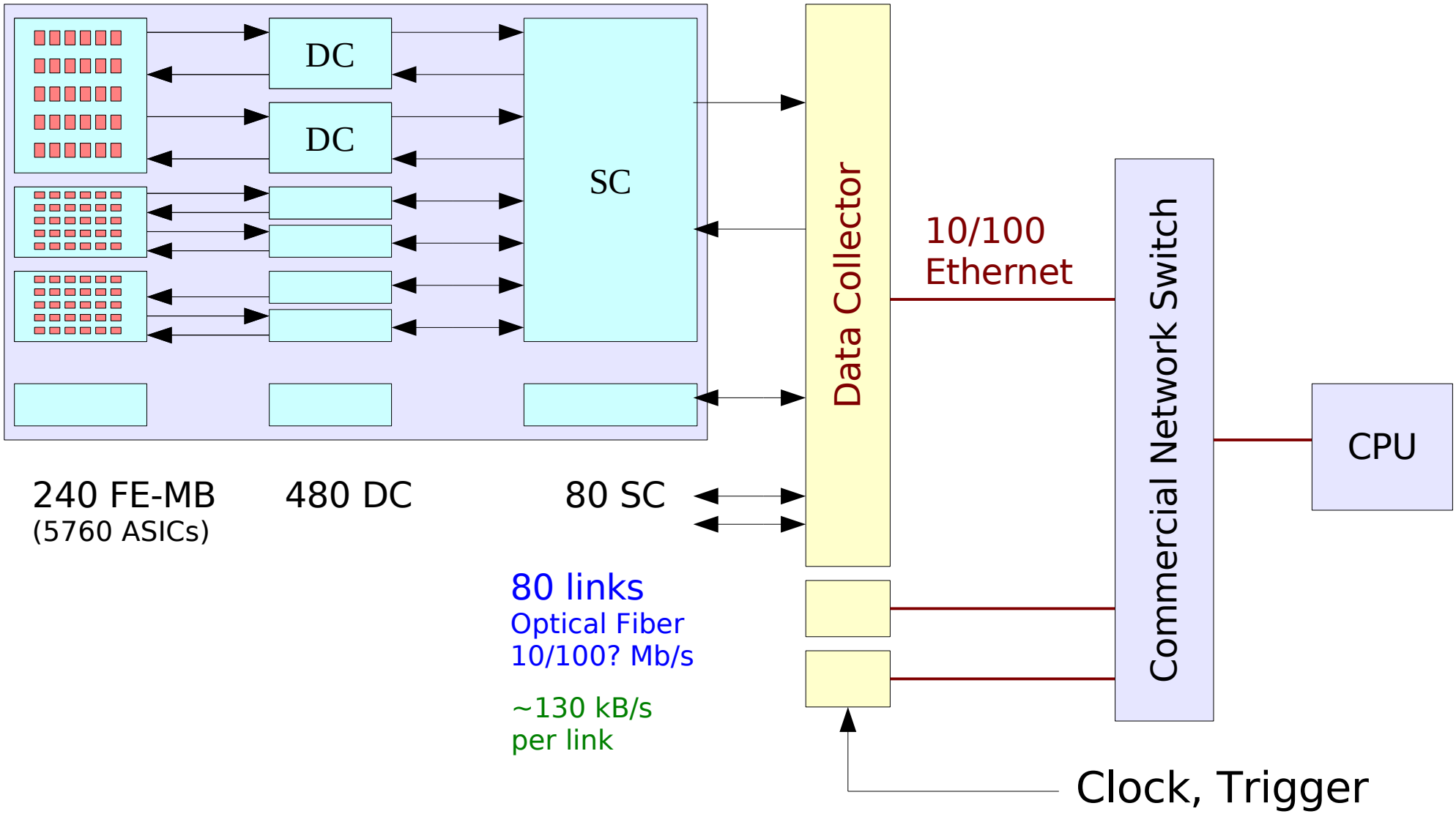


DCOL Technology

- 10 or 100 MB/s serializer/deserializer can be implemented in Virtex 2 or newer Xilinx FPGA
  - tested implementation in our lab at 280MB/s
- Candidate FPGAs have ~200k Bytes RAM
  - perhaps no additional RAM needed for input buffering
- Timing/Control can be sent on transmitter side of optical transceiver
  - one duplex fiber to each SC

DCOL Alternative 2

Ethernet Readout, no VME



Total data rate for entire detector is ≤ 300kByte/s

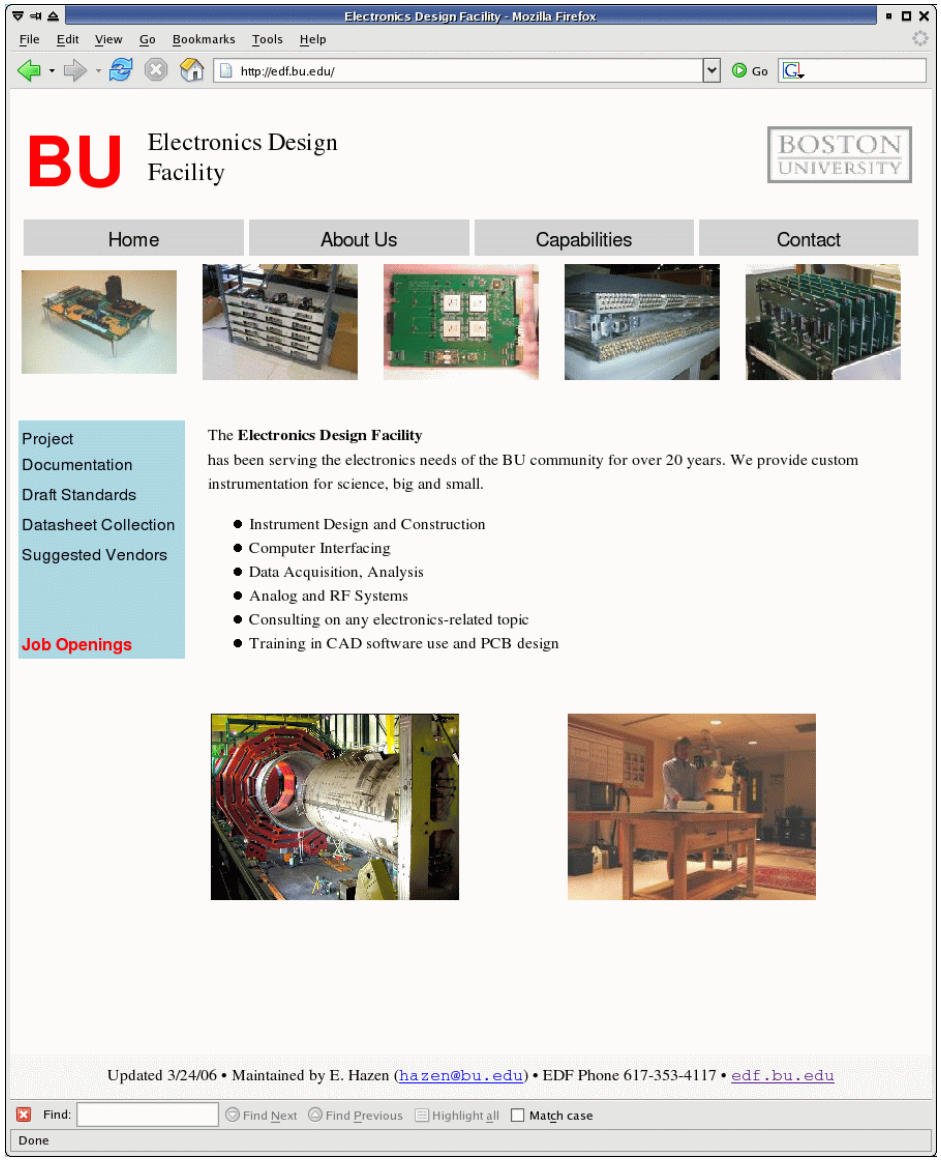
Ethernet Readout

- Pros
  - Eliminate VME crate - direct to CPU (save $$)
  - Easy to scale up
  - Significant experience in other experiments
    - ATLAS TDAQ, KEK (SiTCP), SuperK*
- Cons
  - Final event building stage in software
    - At our slow rate, should not be a problem
  - “New” technology, requires new tools

Cost and Schedule

- No details known yet, but generally...
  - M&S:
    - $5k for PCB prototype run (fab & assembly)
    - Parts cost ~$2k each in very small qty
      - (maybe half that in large qty, plus FPGAs may be free)
  - Engineering
    - 2–6 man-months depending on firmware complexity
    - BU rate is $50/hour so $15k–$50k development
  - Schedule
    - Could start in September with 1 FTE

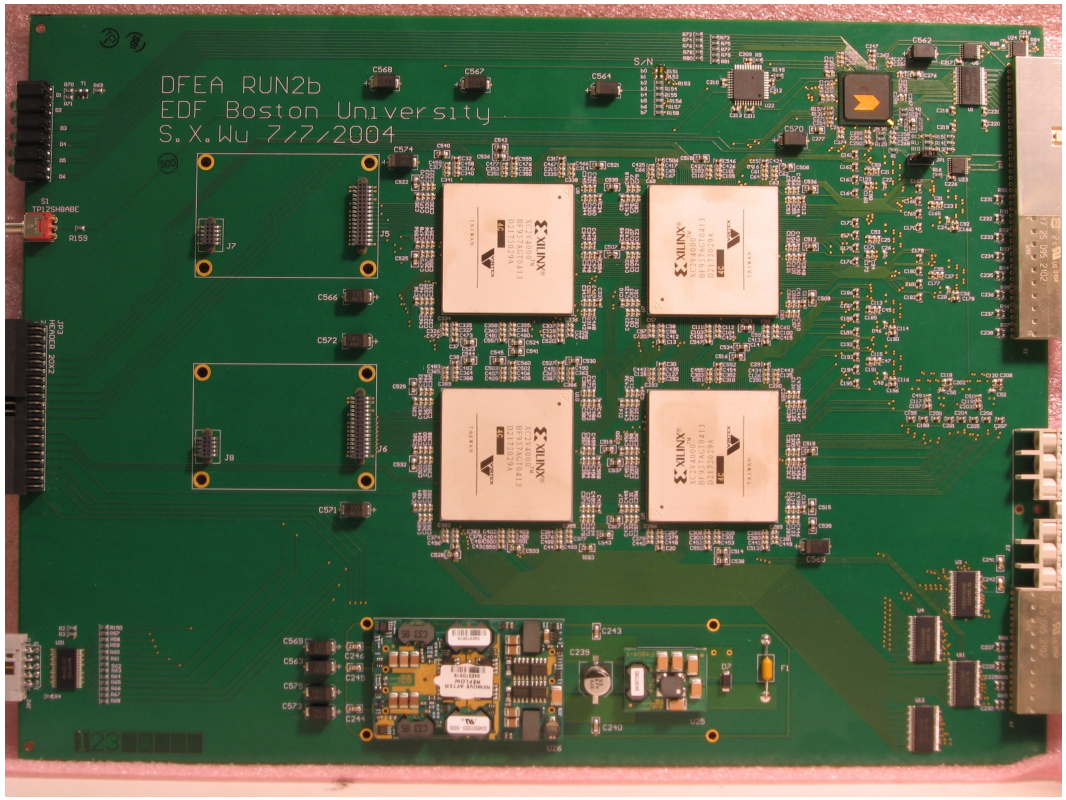
Similar Recent Projects



- D0 L1CTT trigger upgrade
- CMS HCAL data concentrator
- Super-K Ethernet interface
- CMS RPC optical link board

DFEA2 Board for D0/L1CTT

(M. Narain)



- 2nd Generation Level 1 Central Track Trigger processor board
- 8 in, 4 out LVDS serial links (370Mbit/s)
- 24M gates in 4 FPGAs plus VME-like interface
- 48V power
- 60 boards produced

$2M worth of FPGAs donated by Xilinx
(this is our typical experience)

CMS Data Concentrator

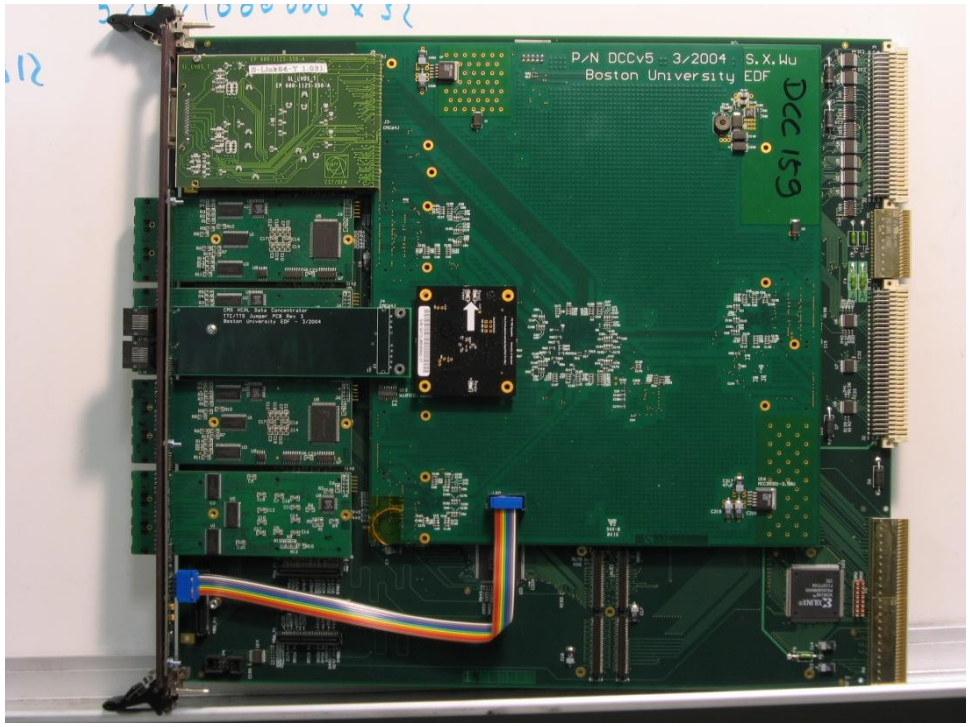
(J. Rohlf)

9U x 400mm VME module with up to 18 inputs
Throughput 200MBytes/sec with fiber output
VME motherboard with PCI bus daughterboard sites
(PC-MIP and PMC)
Can be configured for up to 18 inputs, each 40MHz
Channel Link over RJ-48 (5 pair) cable (>1Gbit/sec each)

40 boards installed in CMS/HCAL at CERN

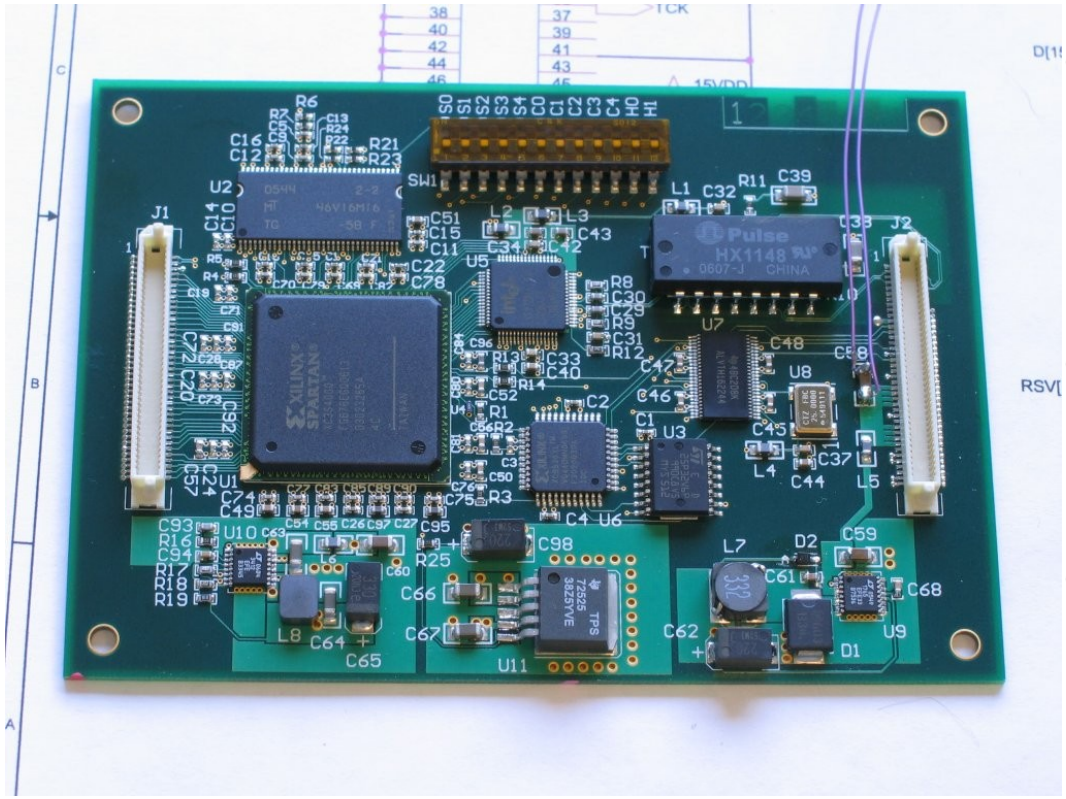
Proven design, but uses somewhat obsolete technology.

Cost about $3500 to produce (2004)



Super-K Ethernet Board

(E. Kearns)

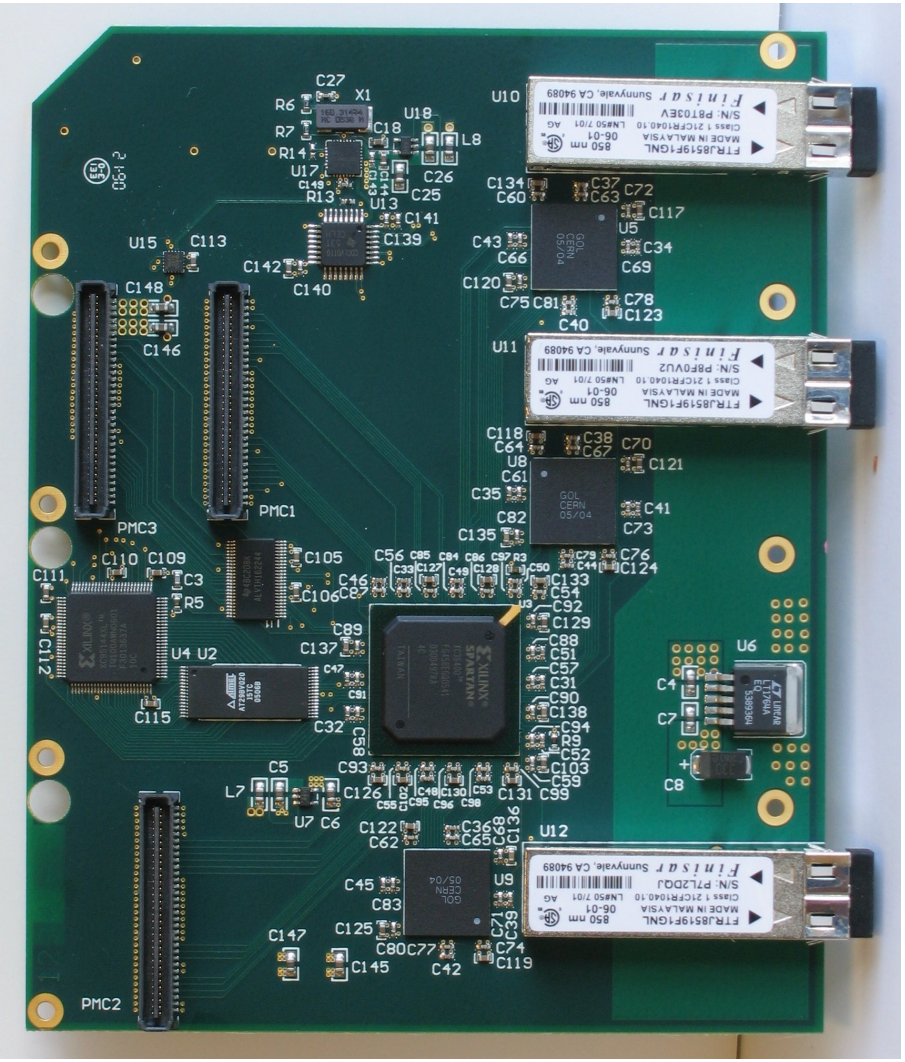


- Ethernet interface between front-end ADC/TDC and DAQ
- Will replace traditional (TKO bus) readout
- Features:
  - Full TCP/IP stack in Verilog (KEK-developed SiTCP)
  - Ethernet firmware updates
  - 15V (only) power
  - DDR SDRAM memory

Working prototypes now; 500 pc production in 2007

CMS RPC Optical Link

(J. Rohlf)



- Connect outer layer of HCAL to muon trigger
- (3) 1.6 Gbaud optical links
  - Finisar transceiver
- On-board PLL for low-jitter link clocks
- FPGA firmware download over local bus
- Working prototypes; 50 pc production in 2007