

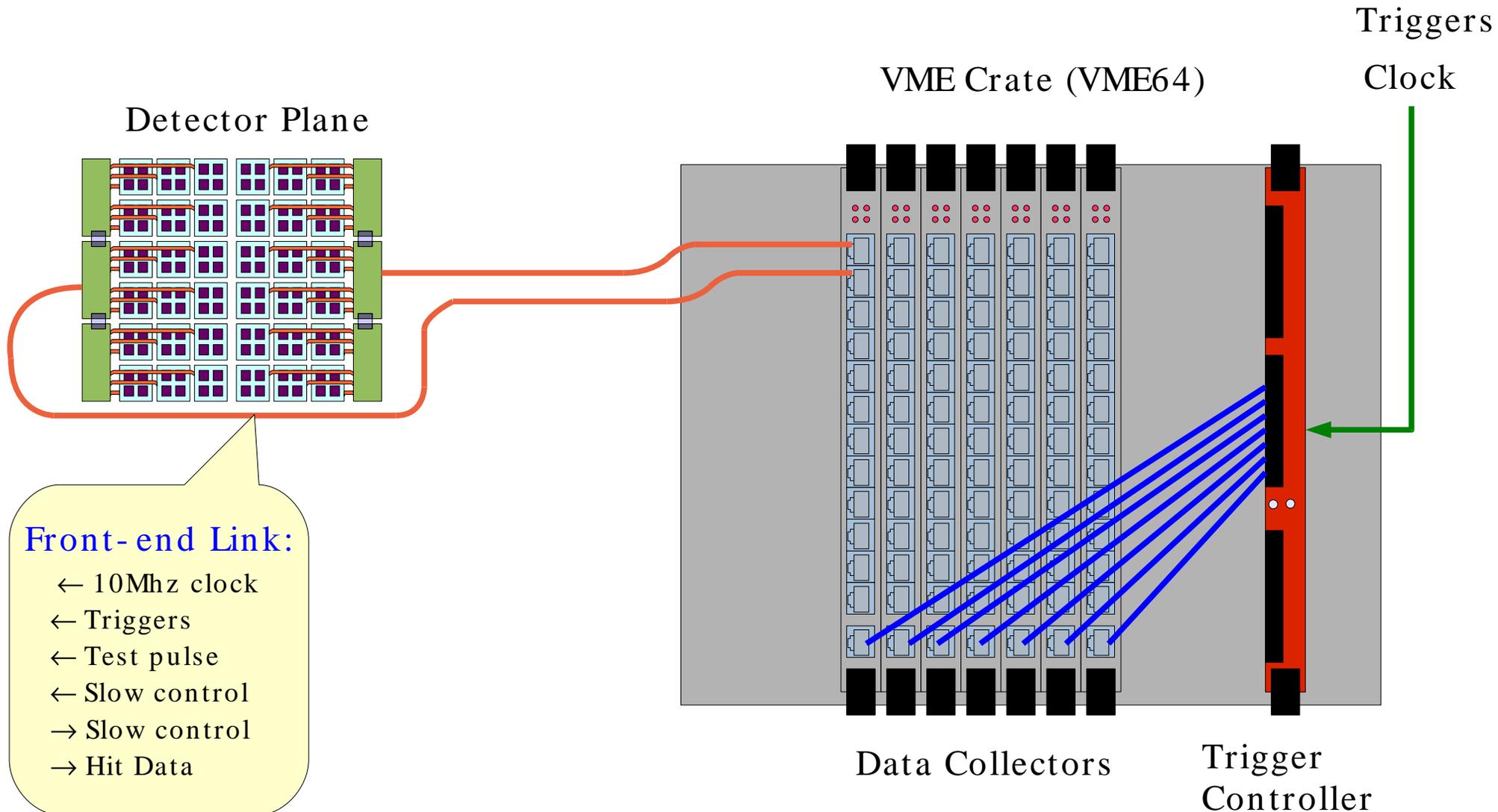
DHCAL Back-End

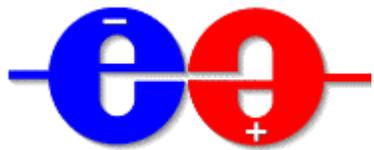
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Readout Overview





Discussion Items



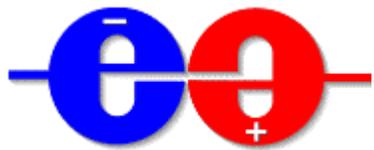
- Are Front-End hits in Time Order?
 - Need to settle this before detailed design of DCOL can start!
- Data/Super Concentrator should send one packet each timestamp wrap
- Permissible trigger delay?
 - Trigger from scintillator or ECAL CRC
 - Receive by trigger module, timestamp
 - Transmit to DCOL
 - Transmit to Data Concentrator
 - Transmit to Front-end board
 - Transmit to DCAL chip
 - Each stage has a delay... what total can be tolerated by DCAL chip?



Discussion Items (2)



- How to handle front-end links detector end
 - Daughter-board designed by BU
 - Built-in circuit designed by ANL to BU specs



Data Collector Status



- Spec online
 - <http://edf.bu.edu/Proj/DHCAL>
- Detailed design started
 - Spartan-3e front-ends
 - Spartan-3 event builder
 - SDRAM buffer
- T.B.D.
 - Front-end link details
 - Buffer size needed



Trigger Module Specs



- **Inputs:**
 - 10MHz system clock
 - External trigger (from logic or ECAL)
 - Logic inputs for coincidence trigger
 - Test pulse
- **Outputs**
 - (12) Encoded trigger/clock to Data Collectors
- **LEDs for power, VME activity, triggers, clock present, other general purpose**



Trigger Module Specs (2)



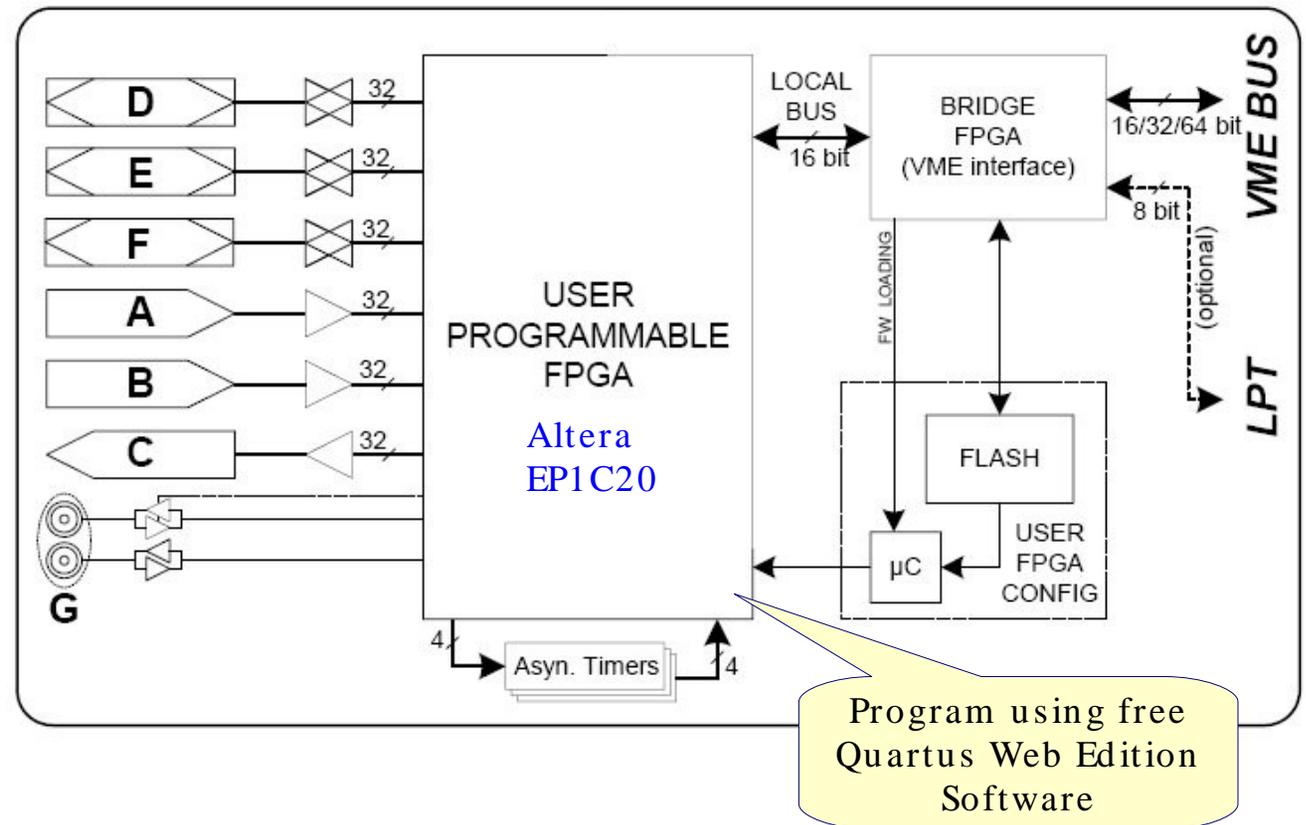
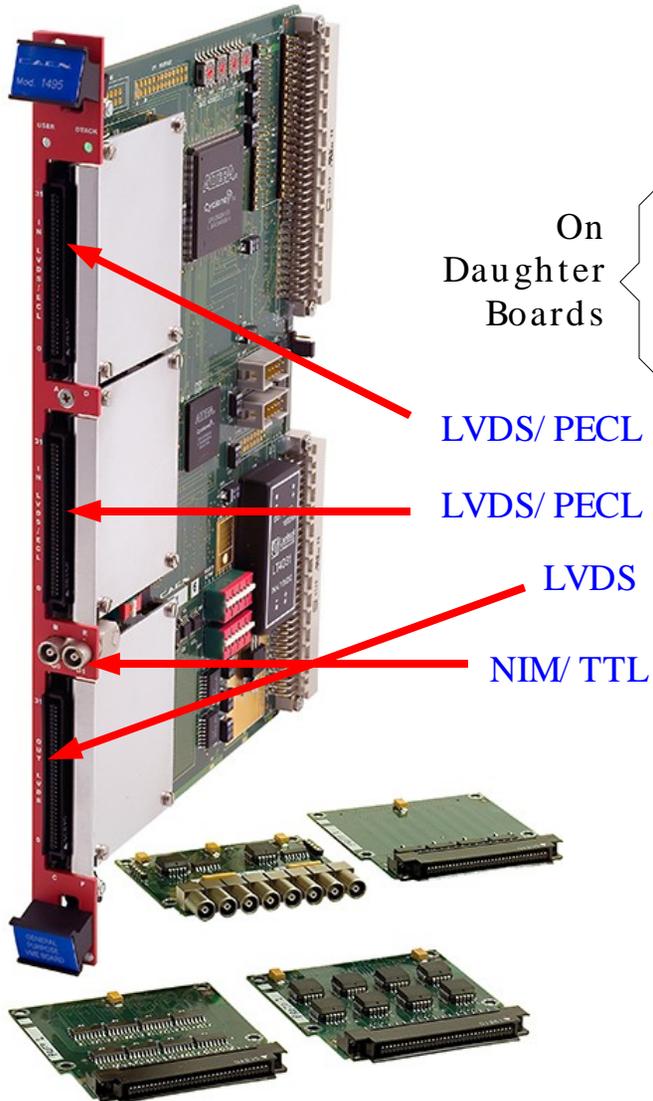
- **Functionality:**
 - Timestamp each trigger, store trigger time and event number in FIFO
 - Trigger modes:
 - External
 - Coincidence logic using multiple (i.e. PMT) inputs
 - Periodic (timer)
 - VME (software forced)
 - **VME Interface**
 - Access to trigger FIFO
 - Current status (current event #, trigger counters, etc)



Candidate Hardware



- CAEN V1495 General-Purpose VME Module



This thing is in production
One unit could be obtained for evaluation quickly
Price: \$3400 (cheaper than custom design)



Action Items



- Settle hardware discussion items today
- Obtain a CAEN module and assign someone the task of programming it to perform simple trigger tasks (or make some other plan for trigger)
- Get started on DAQ software
 - Understand CALICE DAQ requirements
 - Write HAL address tables (DCOL, trigger)
 - Write C++ classes to control modules
 - Write “toy” DAQ for testing