

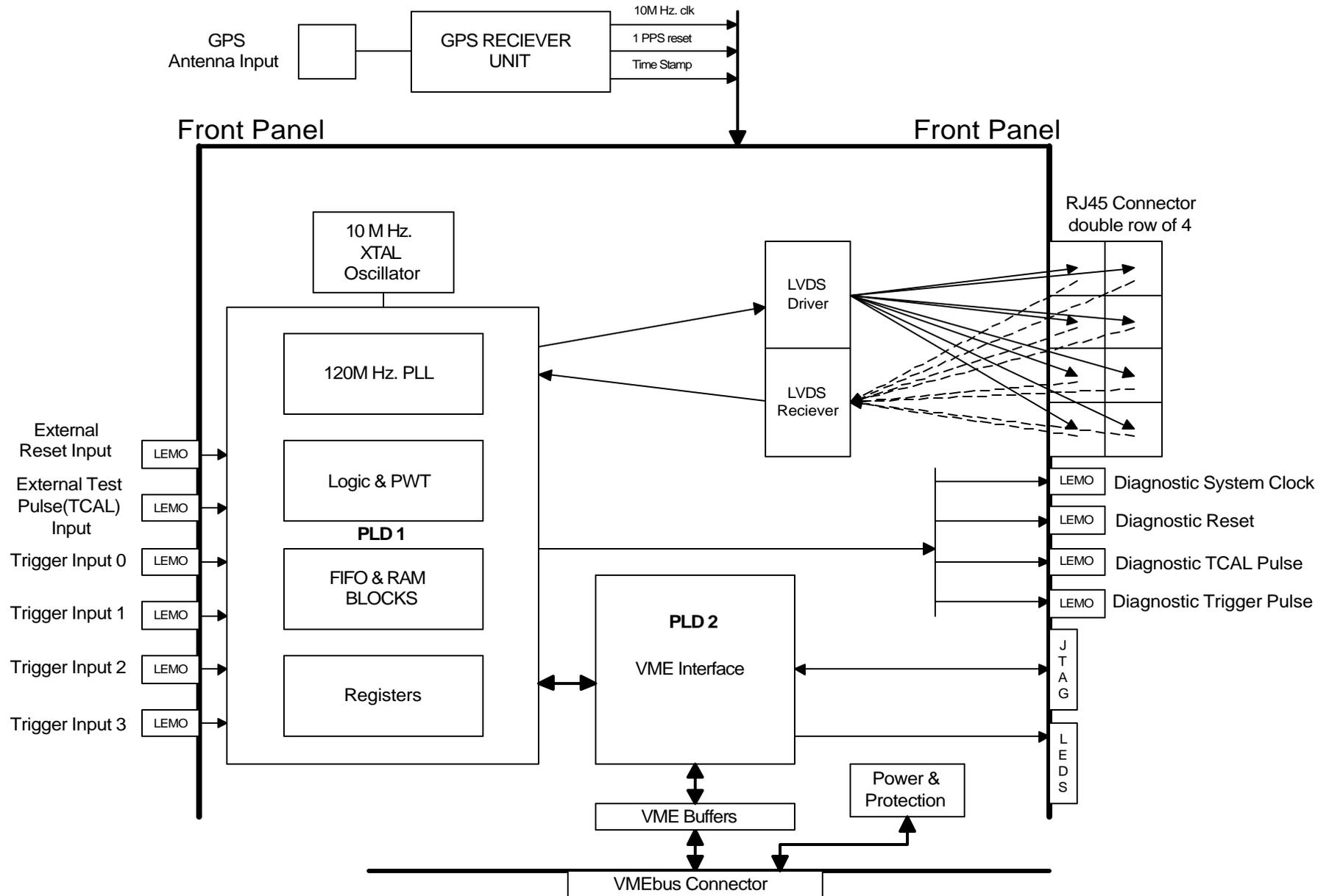
Trigger & Timing Module – Function

sh 3/23/07

- *Process Timing and trigger signals for DCAL system*
 - Receive signals from external GPS receiver – 1PPS, 10M Hz. Clock and Timestamp
 - Receive signals from external trigger electronics
 - Interface with VME host
- *Produce timing signals to the DCAL system*
 - Clock, Trigger, TCAL & Counter Reset in the form of a Pulse Width encoded serial bit stream

Trigger & Timing Module – Block Diagram

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Trigger & Timing Module – Status

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- Functional Specification – on going
- Part Selection – 50 %
- CAD work - started
 - part creation, schematic entry, PCB layout
- Firmware Design - started
 - VME interface, Timing Decoder, GPS interface(will continue during board layout)
- Board Fabrication, Assembly, Testing

Continued

Trigger & Timing Module – Status

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- Similar timing module was produced at Fermilab in the previous year for Minerva
 - 6U x 160mm VME format
 - RJ45 Category 5 bank output – LVDS
 - Starting with that boards CAD work and adding
- VME Interface work has been done previously, needs to be tweaked for TTM module
- GPS Receiver board/interface was done for Quarknet at Fermilab > looks similar to what is needed for TTM