Linear Collider Digital HCAL

Electronics for Resistive Plate Chambers

Presented By
Gary Drake
Argonne National Laboratory

Feb. 27, 2004

Outline of Talk

I. Detector Configuration

II. System Architecture

III. Physical Configuration

IV. Discussion of ASIC

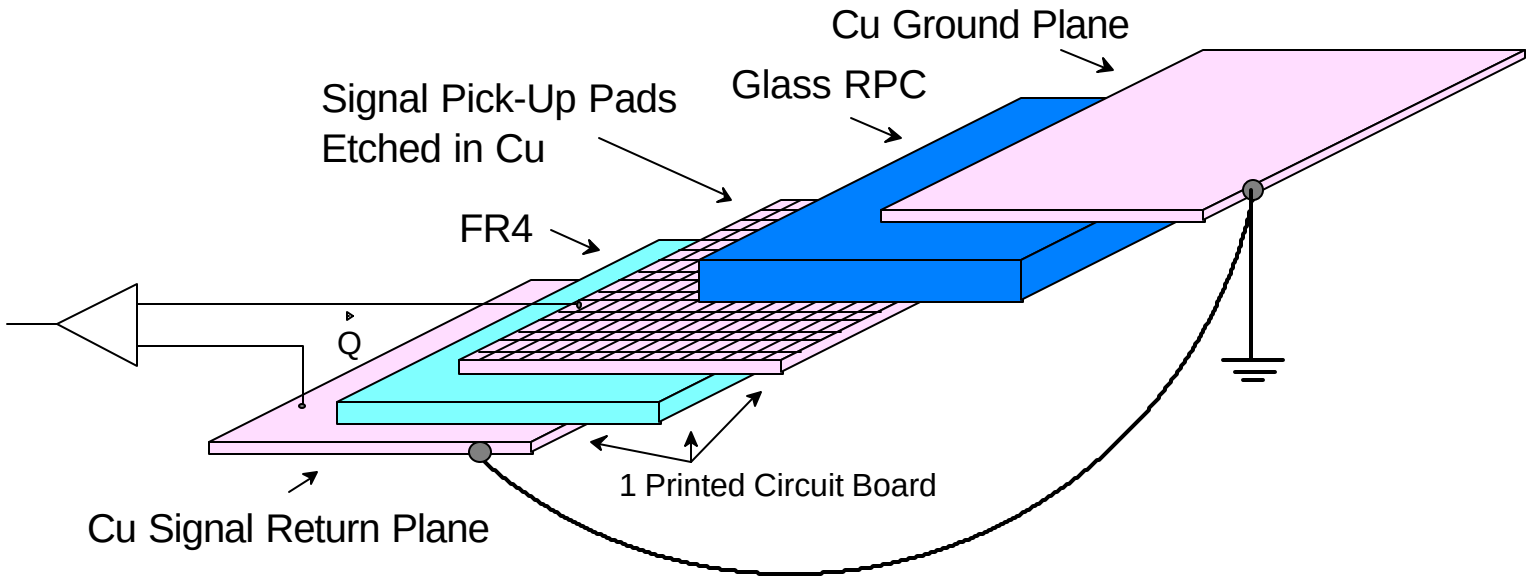
V. Summary

See:

www.hep.anl.gov/drake/linear_collider/040227_meeting.pdf

Detector Configuration

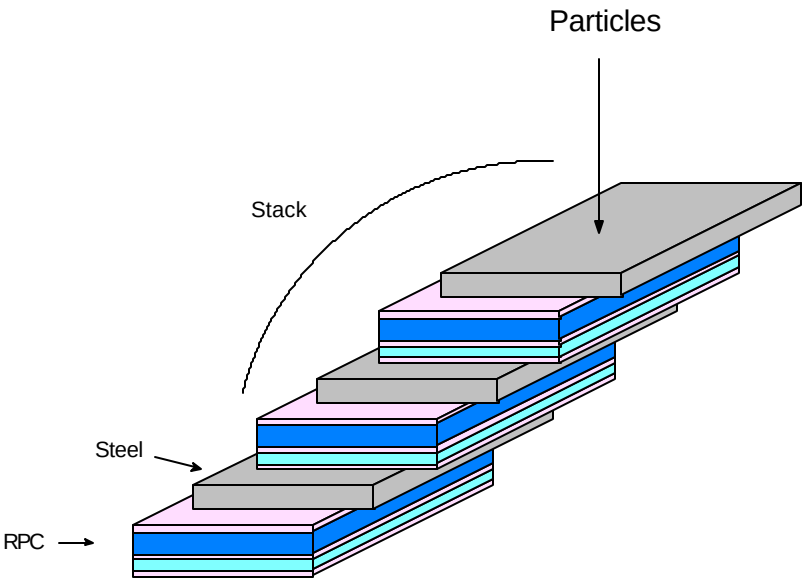
- **Anatomy of the LC RPC**

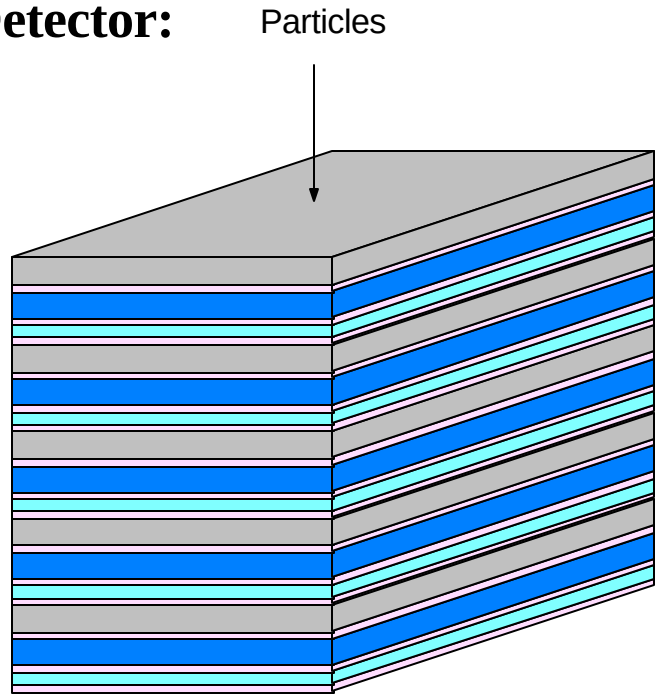


- **Ionization in Gas of RPC Induces Signal on Pad(s)**
- **Fast Current Pulse Flows Between Pads & Signal Return**
- **Pulse Size Depends on Gas & HV - Streamer vs. Avalanche**

Detector Configuration

- **Anatomy of the LC RPC (Cont.)**
  - **To Make the Prototype Hadronic Detector:**

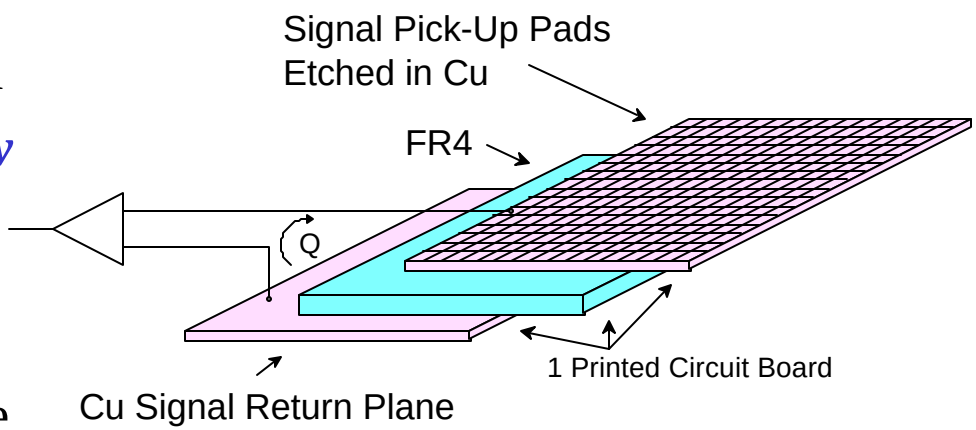




1 Cubic Meter "Prototype"
~400,000 Channels of RPC Readout
(Assumes 1 cm X 1 cm pads)

Detector Configuration

- **Anatomy of the LC RPC (Cont.)**
  - **The Nature of the Linear Collider Hadronic Calorimeter:**
    - Pads are 1 cm X 1 cm ®
      Creates Fine Segmentation
    - Concept of "***Particle Flow Algorithms***" to Analyze Energy Deposition
    - Analyze Hits (Digitally), Instead of Measuring Pulse Height



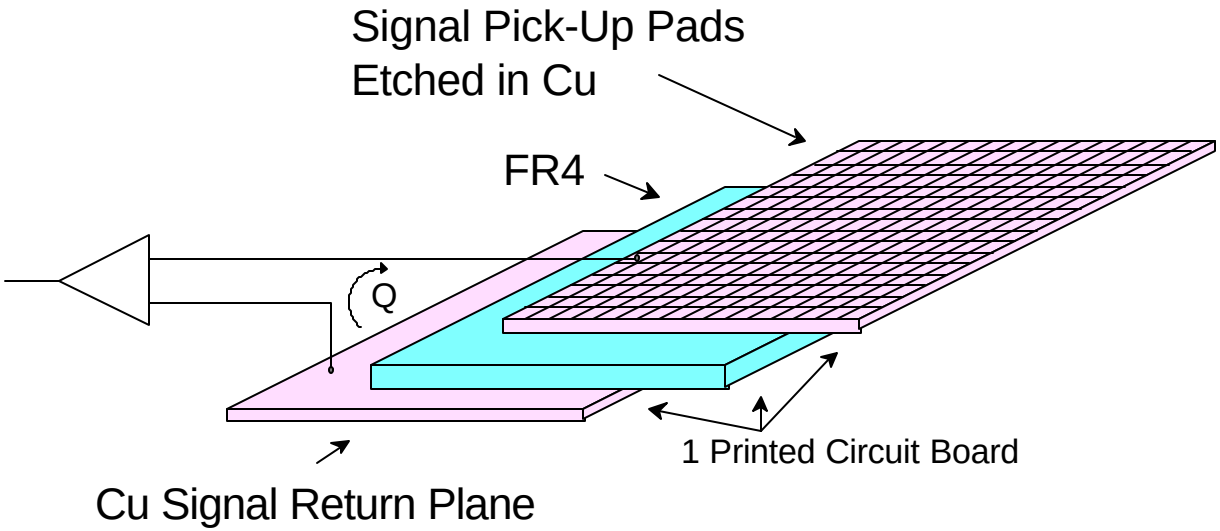
➢ **Trade Wide Dynamic Range, Tower Geometry, & Sampling Depth, for Fine Grain, Low Dynamic Range on Many Channels**

⇨ ***A 1-Bit ADC!***

⇨ ***Well-Suited for an ASIC***

Detector Configuration

- **Anatomy of the LC RPC (Cont.)**

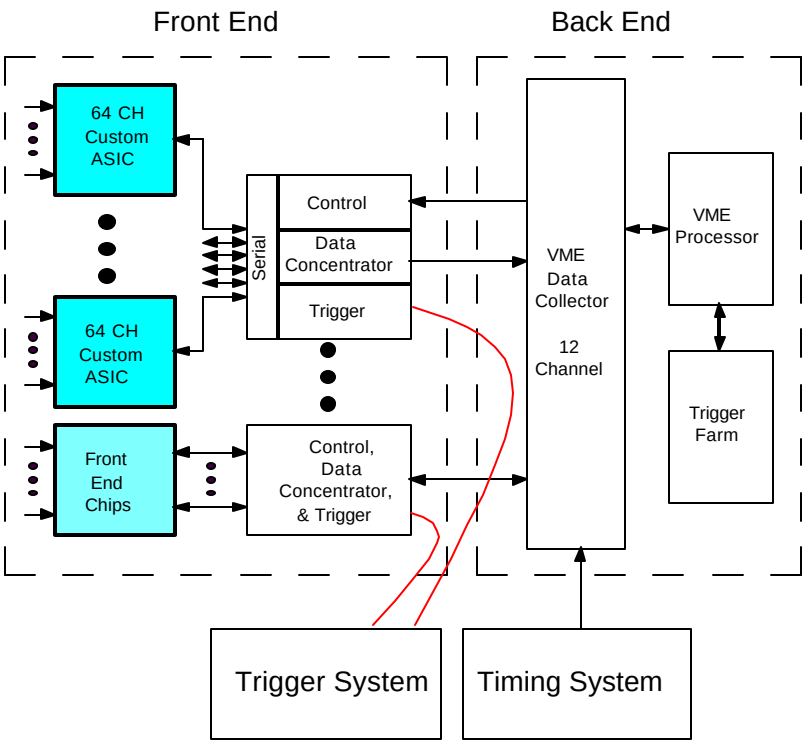


- **The Instrumentation Job:**
  - Receive Signals from Each Pad
  - Discriminate Signals as "Hits"
  - Tag Hits in Time to Facilitate Track Reconstruction

- **Primary Goals:**
  - ✶ **1 Bit Dynamic Range**
  - ✶ **Large Number of Channels**
  - ✶ **Cheap Electronics**

System Architecture

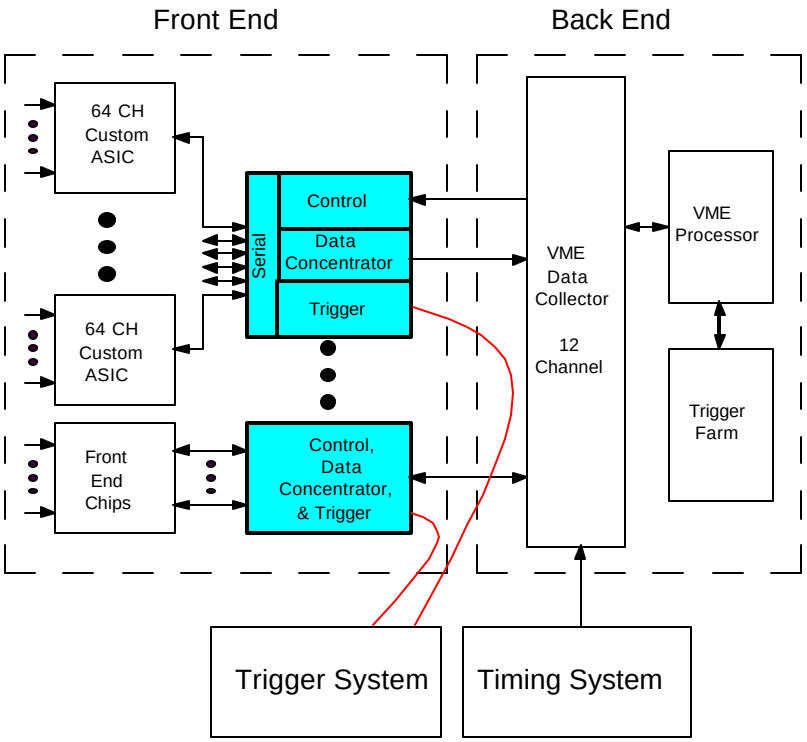
- **Front End**
  - **Custom ASIC**
    - Resides on Chambers
    - Performs Functions:
      - » Receive, Process, & Discriminate Detector Signals
      - » Timestamp Hits, & Record Hit Pattern
      - » Temporary Data Storage
      - » Serial Data Transmission
    - Can Self-Trigger, or Use External Trigger
    - Services 32-64 Detector Channels



⇨ ***More on This Later...***

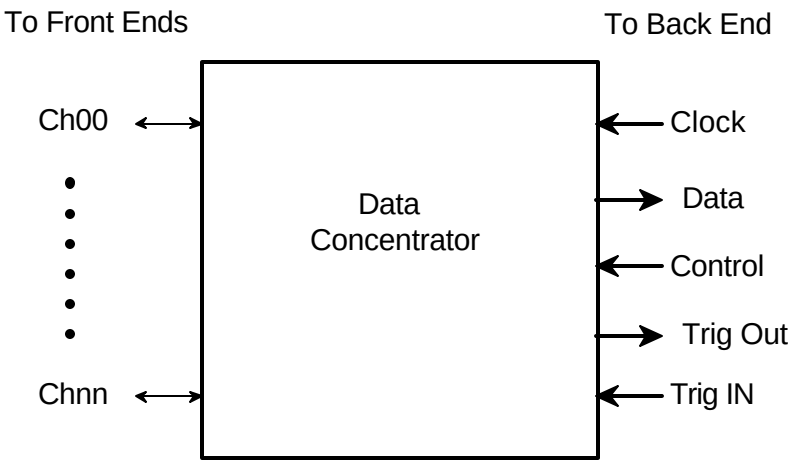
System Architecture

- **Front End (Cont.)**
  - **Data Concentrator:**
    - Concatenate Serial Data Streams from Several Chips ® Multiplexer
    - ***N*** Serial Lines In, 1 Serial Line Out
    - Drives Serial Line to Back End Read-Out Electronics
    - Handles Clock & Control Interface
    - Handles Trigger Interface



System Architecture

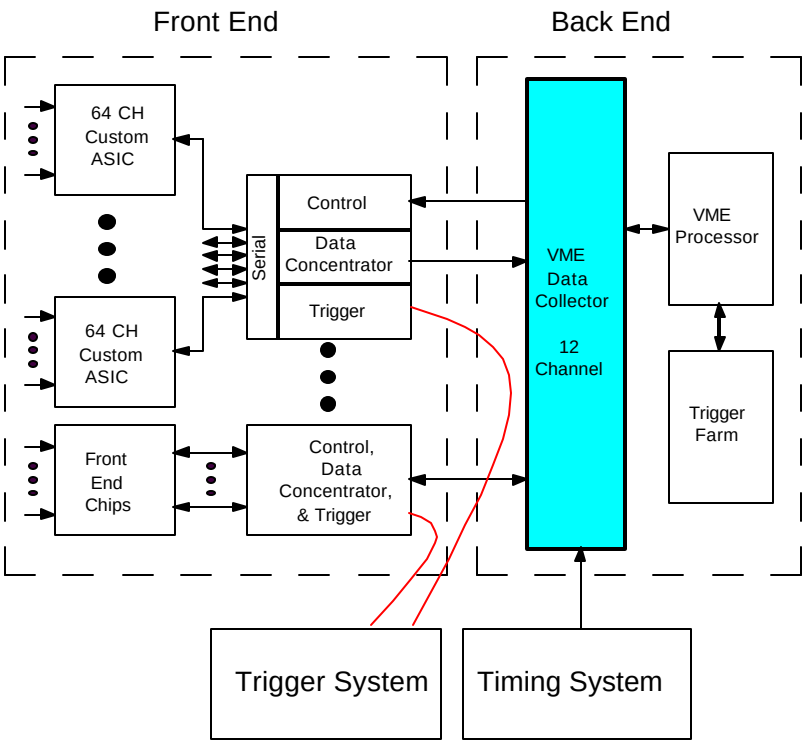
- **Front End (Cont.)**
  - **Data Concentrator (Cont.):**
    - Acts as Funnel for Data
    - Adds Chip ID to Data
    - Has Buffering
    - Has Flow Control



- **Needed to Reduce Back-End Costs - Expensive VME**
- **Relies on <u>Low</u> Trigger Rate**
- **Exploring Implementation with FPGAs**

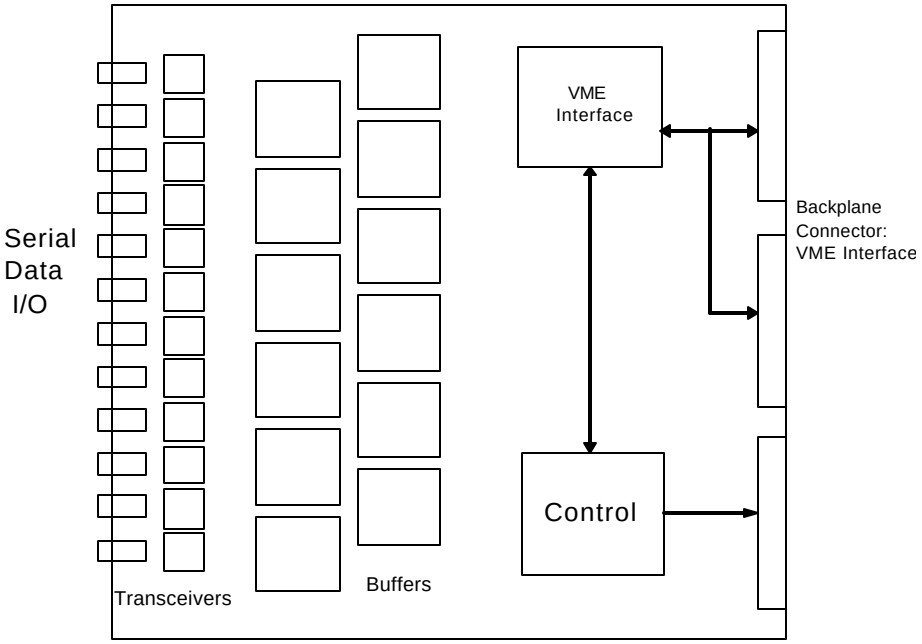
System Architecture

- **Back End**
  - **VME Data Collector:**
    - 9U x 400 mm VME
    - Receives Serial Data Streams from Several Data Concentrators
    - Stores Data in Buffers
    - Dual Buffers: Data Written into One While Processor Reads the Other
      - ® ”Buffer Swaps”



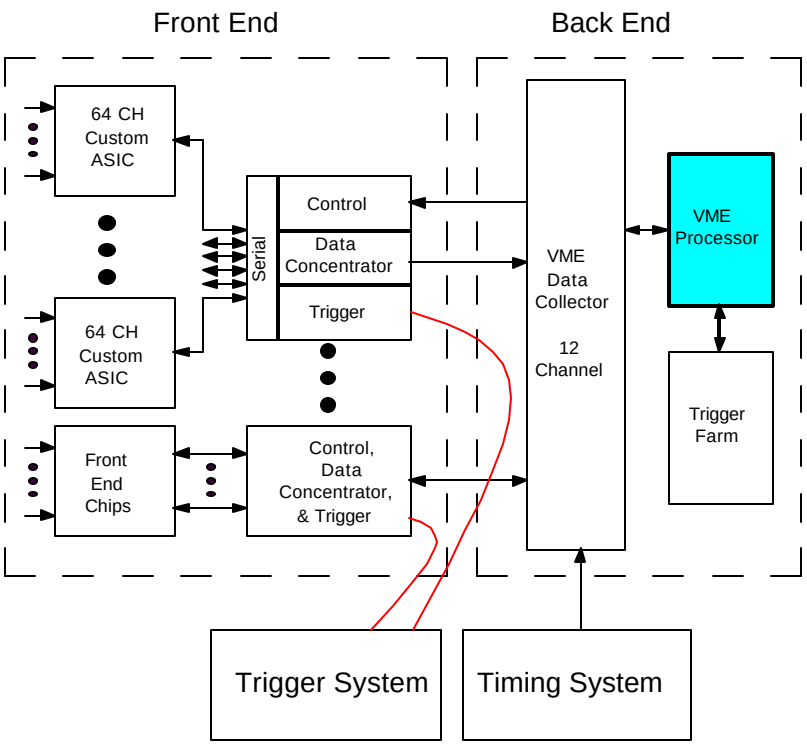
System Architecture

- **Back End (Cont.)**
  - **VME Data Collector (Cont.)**
    - Conceptual Implementation: 9U x 400mm VME, 12 Inputs
    - Receives Data Streams
    - Buffers Read from VME
    - Also Provides Control on Separate Path
    - Extensive Use of FPGAs - Provides High Degree of Flexibility



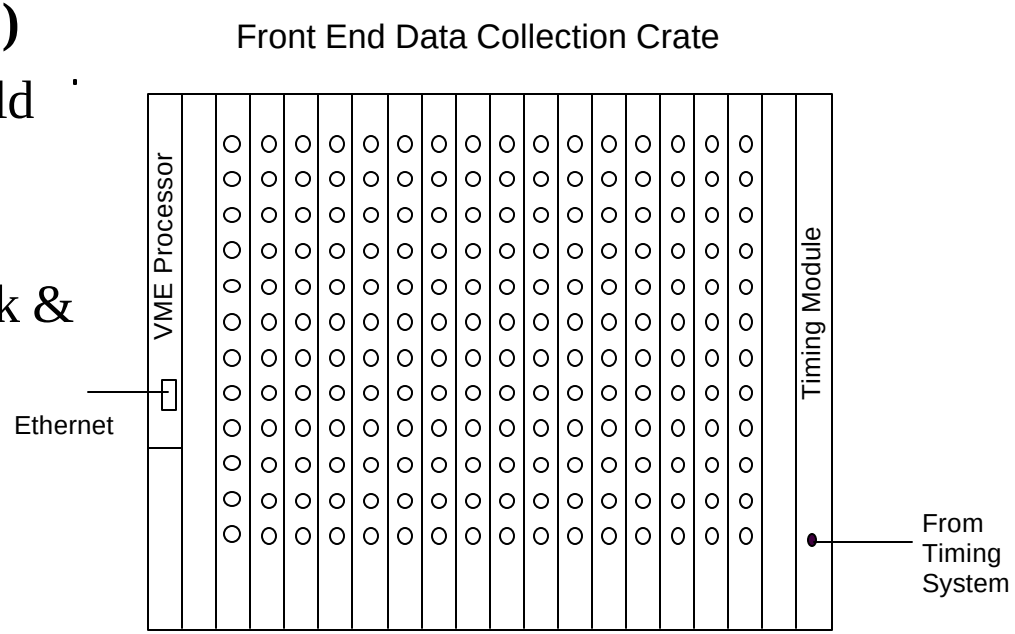
System Architecture

- **Back End (Cont.)**
  - **VME Processor:**
    - Buffer Swaps Coordinated by VME Timing Module using ISRs
    - Read Data from All Data Collectors in VME Crate
    - Forms Time Frames from Timestamps (~1 Sec)
    - Sends Time Frames to Trigger Farm for Processing



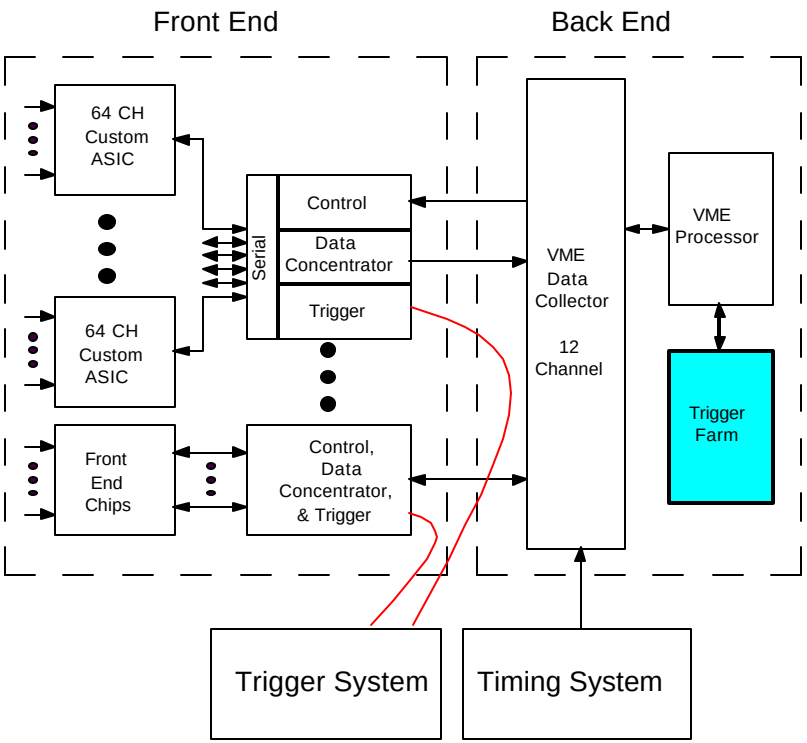
System Architecture

- **Back End (Cont.)**
  - **VME Processor (Cont.)**
    - VME Crate Can Hold ~20 Data Collectors
    - VME Processor Connects to Network & Trigger Farm



System Architecture

- **Back End (Cont.)**
  - **Trigger Farm:**
    - Receives Time Frames from All VME Processors in System
    - Uses Timestamps in Pattern Recognition Algorithm to Find Tracks
    - Write Good Data to Disk
    - Discards Junk



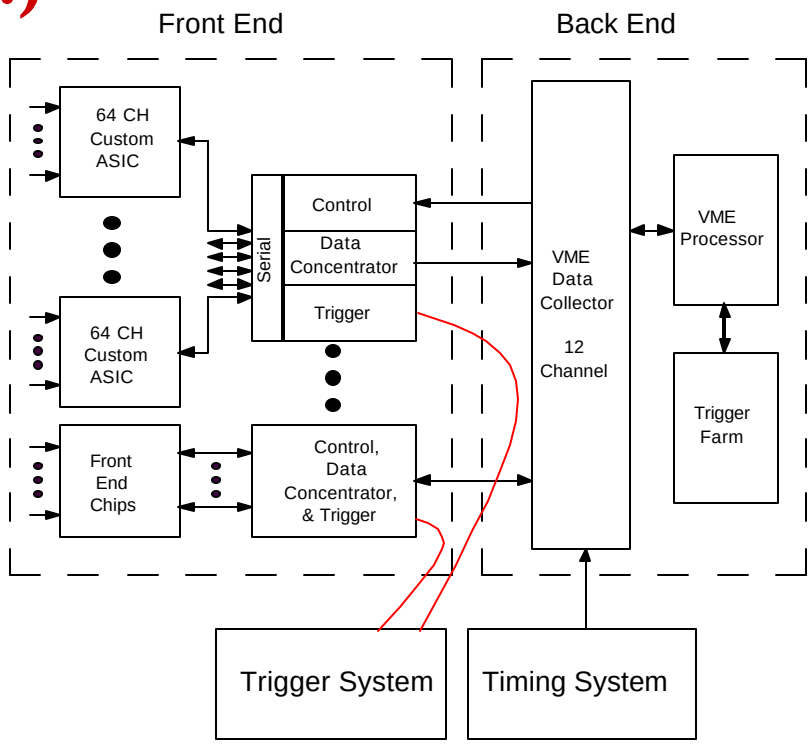
System Architecture

- **System Overview (Cont.)**

➢ **Architecture Based Upon Assumption of Low Trigger Rate (® LC, NOA)**

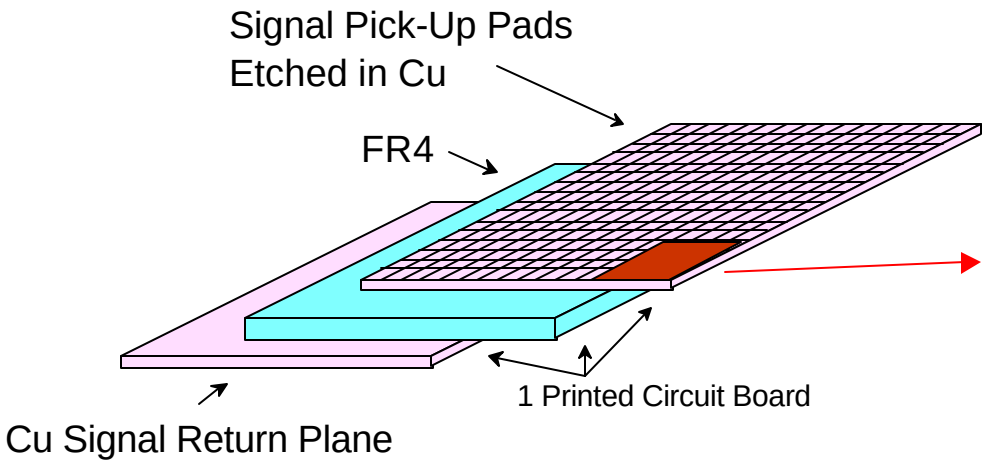
➢ **Events are Tagged with Timestamps at Front End to Allow Processing Latency**

➢ **Timestamps used for Event Reconstruction**
® **Similar to MINOS**

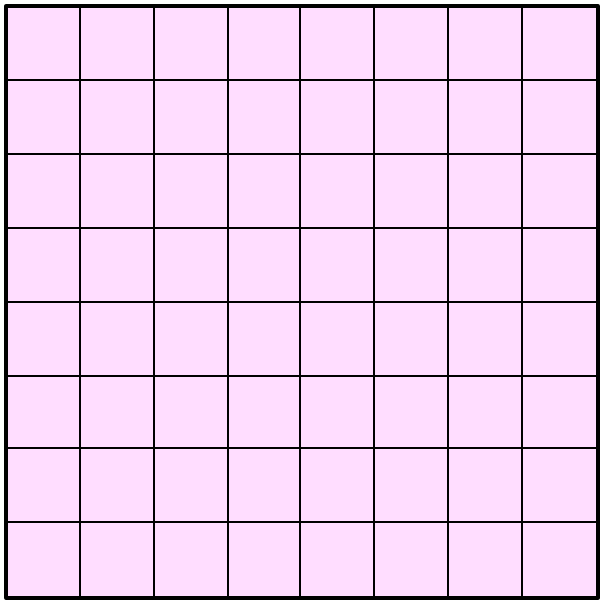


Physical Configuration

- **ASICs On the Detector**
  - **Basic Cell Grouping: 8x8 Cells**



8 x 8 RPC Cell Array
(Part of Single RPC Chamber)

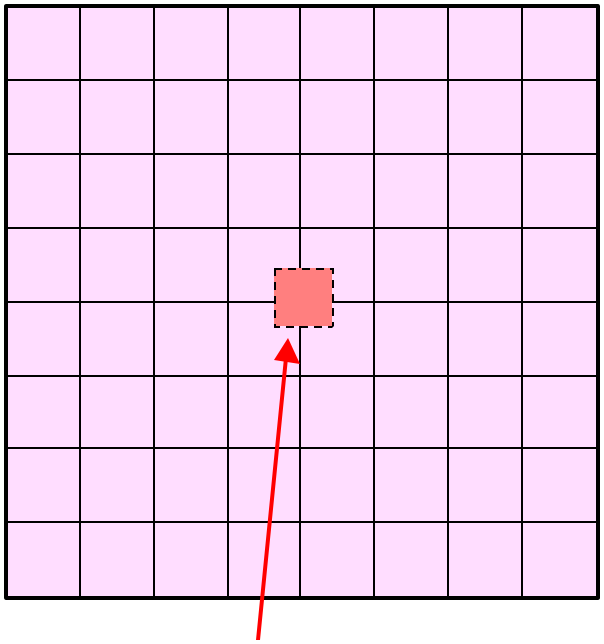


➢ **Several Implementation Ideas Under Discussion...**

Physical Configuration

- **"Ideal" Configuration: ASICs On-Chamber**
  - **Design Multi-Layer Printed Circuit Board**
  - **Incorporate Cell Structure and Signal Layers in Single PCB**
    - Detector Signals
    - Digital I/O
    - Power & Ground

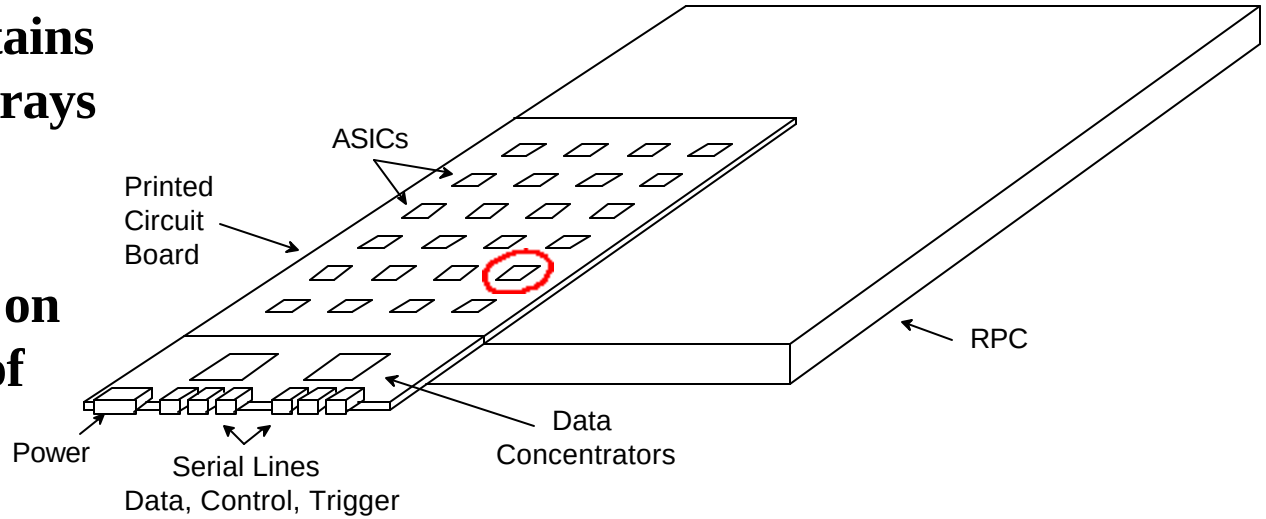
8 x 8 RPC Cell Array
(Part of Single RPC Chamber)



ASIC on Opposite Side of PCB

Physical Configuration

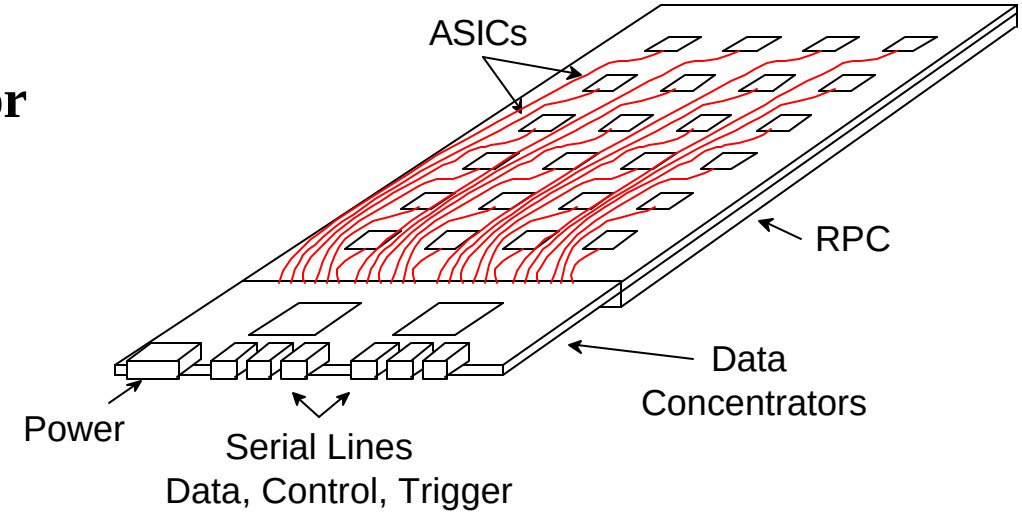
- **"Ideal" Configuration: ASICs On-Chamber (Cont.)**
  - **One PCB Contains Several 8x8 Arrays with Chips**
  - **Arrange Data Concentrators on Outside Edge of Chamber**



- **Pros: Short Detector Signal Transmission Path, Low Input Capacitance, Close to What is Needed in Final Design, No Dead Spaces from Circuitry, Low Assembly Labor**
- **Cons: Digital Noise, Board Complexity** ⇨ ***Likely to be Challenging...***

Physical Configuration

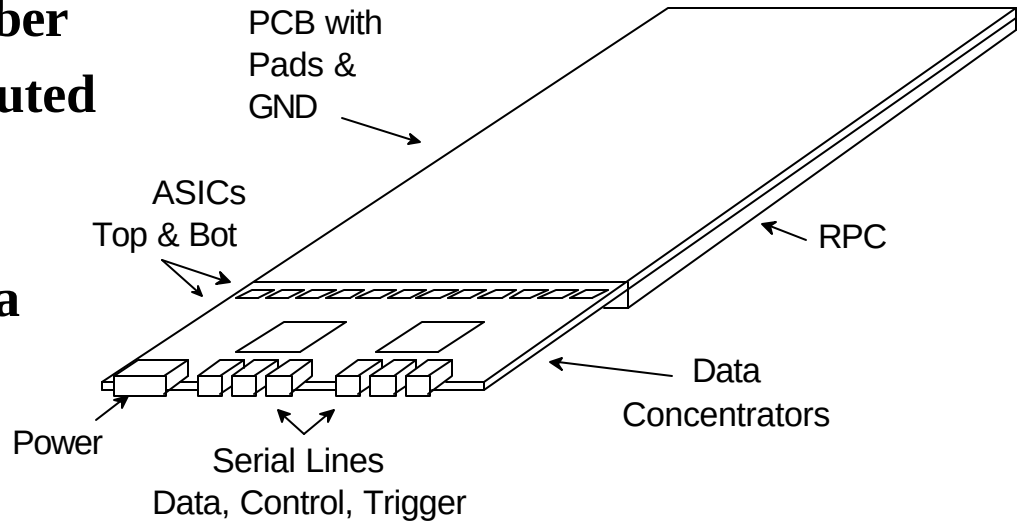
- **Alternate #1: ASICs On-Chamber with "Hair"**
  - **ASICs on Chamber**
  - **Use Multi-Conductor Cables for Digital Transmission, One per Chip**



- **Pros: Short Detector Signal Transmission Path, Low Input Capacitance, Would Work in Final Design, No Dead Spaces from Circuitry, Reduced Digital Noise**
- **Cons: Still May Have Digital Noise, Cable Quality, Assembly Labor**

Physical Configuration

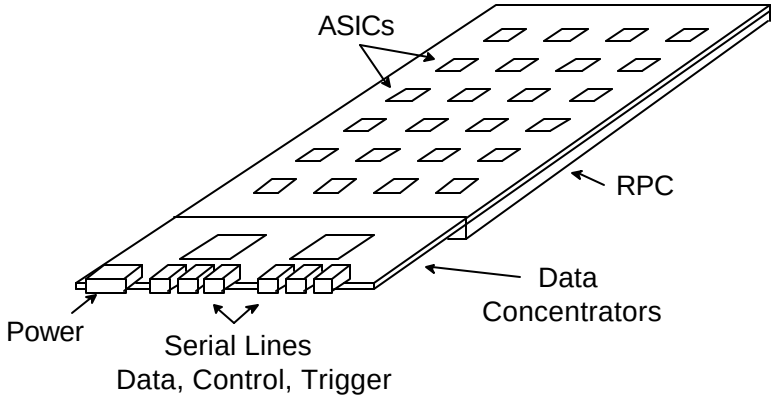
- **Alternate #2: ASICs Off Chamber**
  - **No ASICs on Chamber**
  - **Detector Signals Routed to Edges**
  - **ASICs on Separate Board, Close to Data Concentrators**

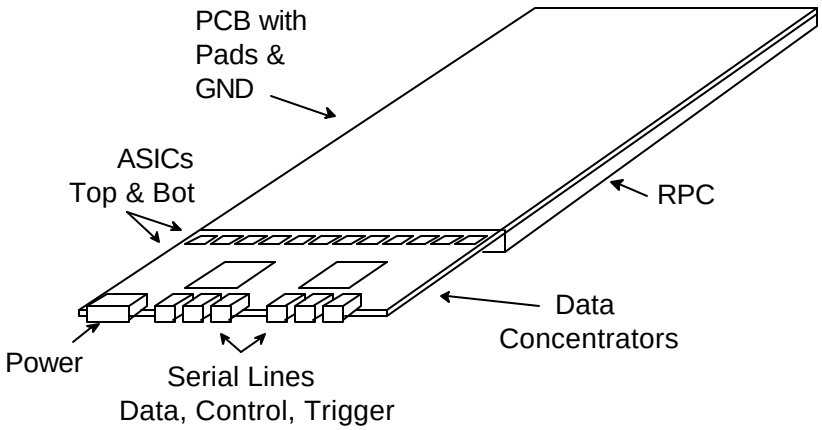


  - **Pros: Substantially Reduced Digital Noise Problems, Electronics Design De-coupled from Detector, Low Assembly Labor**
  - **Cons: Analog Crosstalk, Increased Detector Capacitance, Noise Pick-up on Long Analog Lines, Not Viable in Final Design of Detector**

Physical Configuration

- **ASICs On or Off Chamber**





- **R&D Planning in Progress to Choose Best Implementation**
- **Basic Functionality of ASIC (Mostly) Independent...**

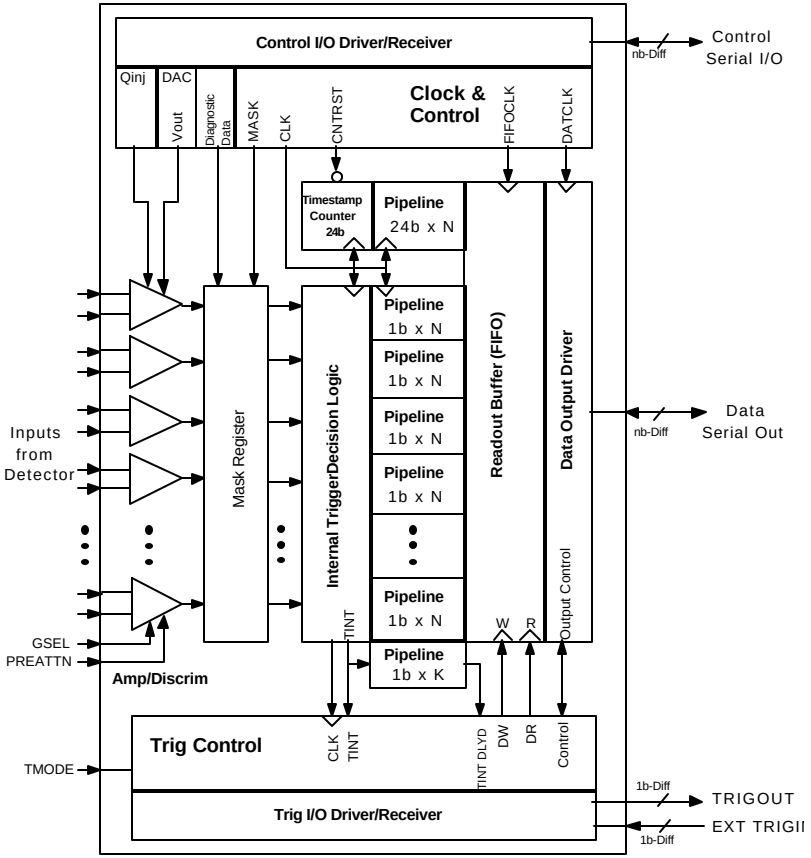
Physical Configuration

- **Implementation with Other Detectors**

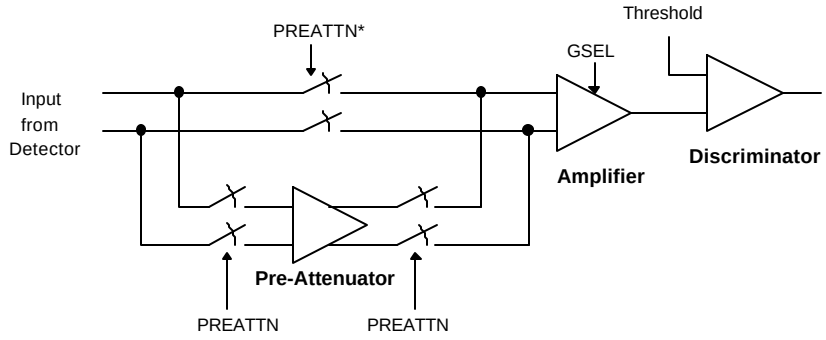
Parameter	Linear Collider RPCs	Linear Collider GEMS	NUMI Off-Axis RPCs	Linear Collider Scintillator
Type	Avalanche	(Gas)	Streamer	Solid, Si PMs
Geometry	Pads	Pads	Strips	Tiles w/Fibers
Capacitance	10-100 pF	10-100 pF	110 ohm Transmission Line	~10 pF
Smallest Signal	~100 fC	~5 fC	1 pC	~100 fC
Pulse Width	~5 nS	~3 nS	~100 nS	~20 nS
Rise Time	~2 nS	?	~10 nS	~5 nS
Largest Signal	~10 pC	~100 fC	~100 pC	~10 pC
Noise Rates	~0.1 Hz	?	(~10 Hz)	?
Env. Noise Susceptibility	Low	Low	Mod (High)	Low

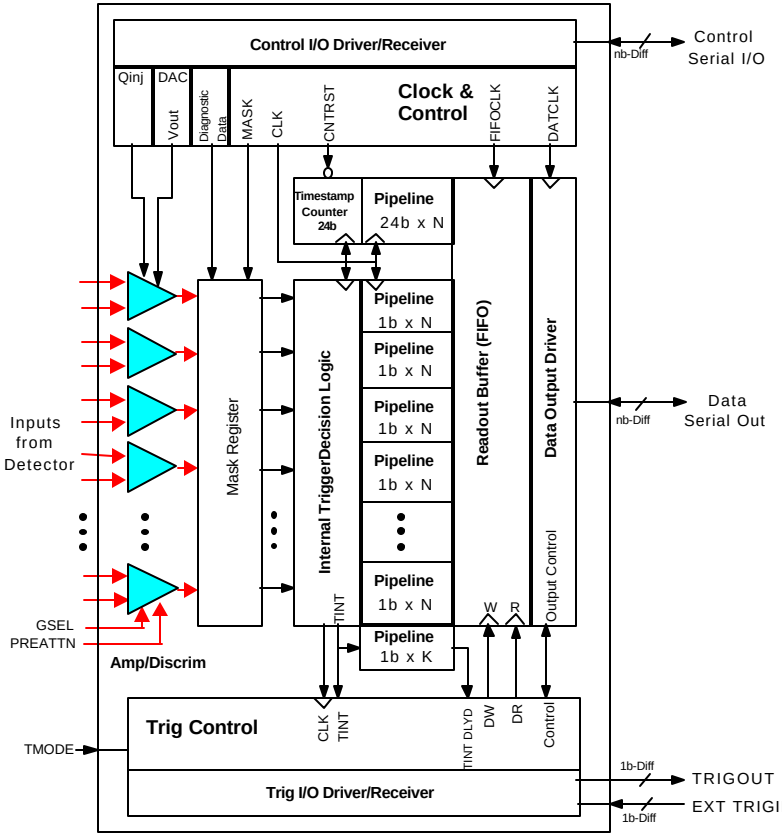
Front End ASIC

- **Basic Architecture**
  - Front End Amplifier & Discriminator Senses Hits Above Threshold
  - 24-Bit Timestamp Counter Runs at 10 MHz
  - Comparator States Clocked into Shift Register
  - Save States & Timestamp on Ext. Trig. or Self-Trigger
  - Serial I/O – Separate Data, Control, & Trigger
  - Services 32-64 CH

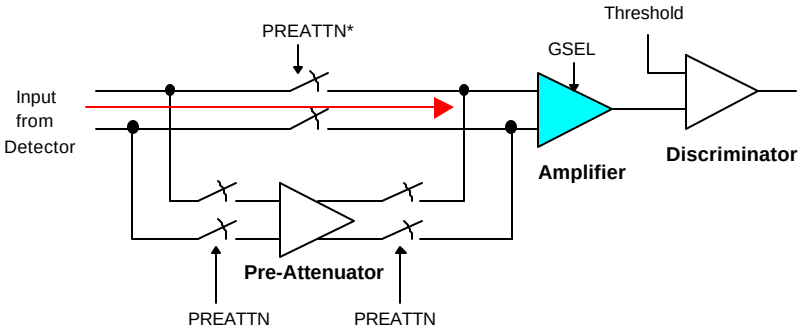


- **Amplifier/Discriminator**
  - **3 Functional Blocks**
    - Amplifier
    - Discriminator
    - Pre-Attenuator



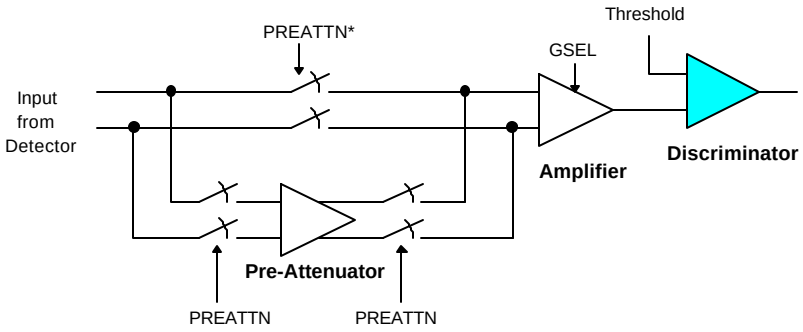


- **Amplifier/Discriminator (Cont.)**
  - **Amplifier**
    - Receive & Process Charge Pulses (Assume Neg. Charge)
    - Output is a Voltage, Proportional to Total Charge
    - Fast Rise Time is Important, But May Have Shaping
    - Requires 2 Selectable Gains: ~1 pC/V (Avalanche RPC), ~0.1 pC/V (GEM) Set By ***GSEL***
    - May Be Single-Ended Input (But Requires Return Current Path)



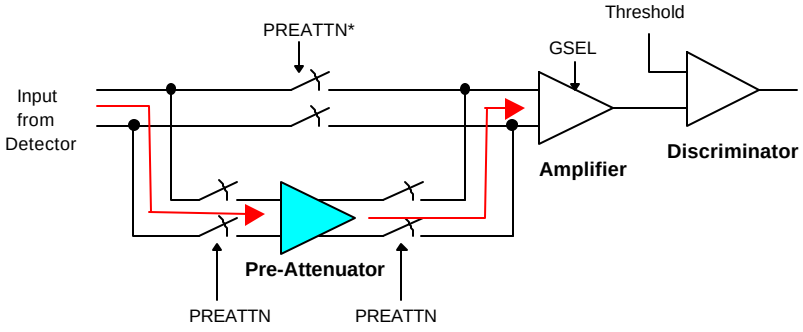
• Amplifier/Discriminator (Cont.)

- **Discriminator**
  - Compare Amplifier Voltage to Threshold Voltage
  - Latch if Over-Threshold
  - Latch Only Once per Pulse
  - Register State on Clock Edge, & Reset Latch
    - No Time Over Threshold
  - Threshold Voltage Common to All Channels
    ® Need Amplifier Offset Compensation



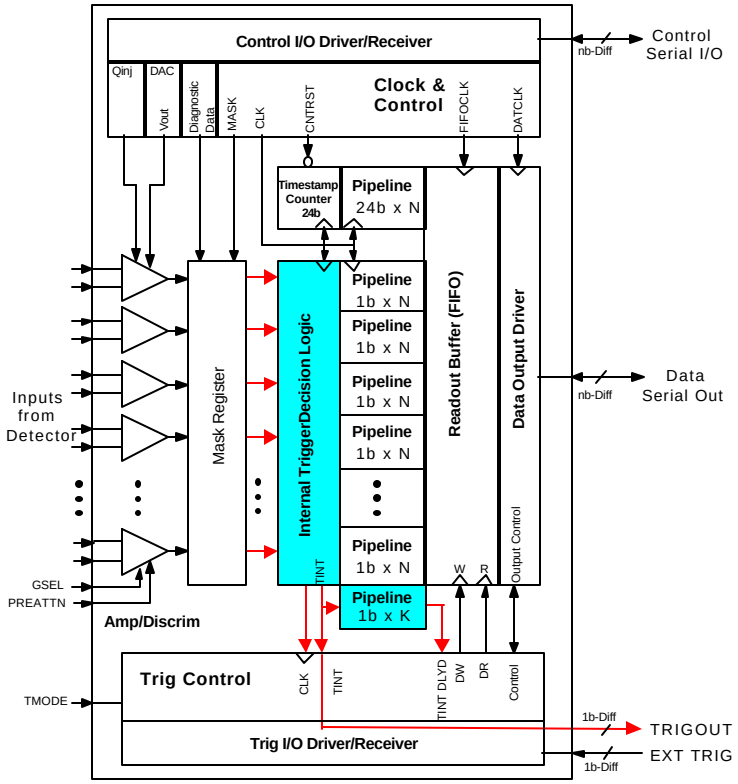
Amplifier/Discriminator (Cont.)

- **Pre-Attenuator**
  - Needed for RPC Streamers
  - Can be Voltage Amplifier, with Resistive Termination (110 Ohms of Trans. Line)
  - Attenuate Signal by ~X10
  - Must be Differential, to Handle Pos. & Neg. Charge
  - Output is a Current, Compatible with Amp
  - Switch In with ***PREATTN***



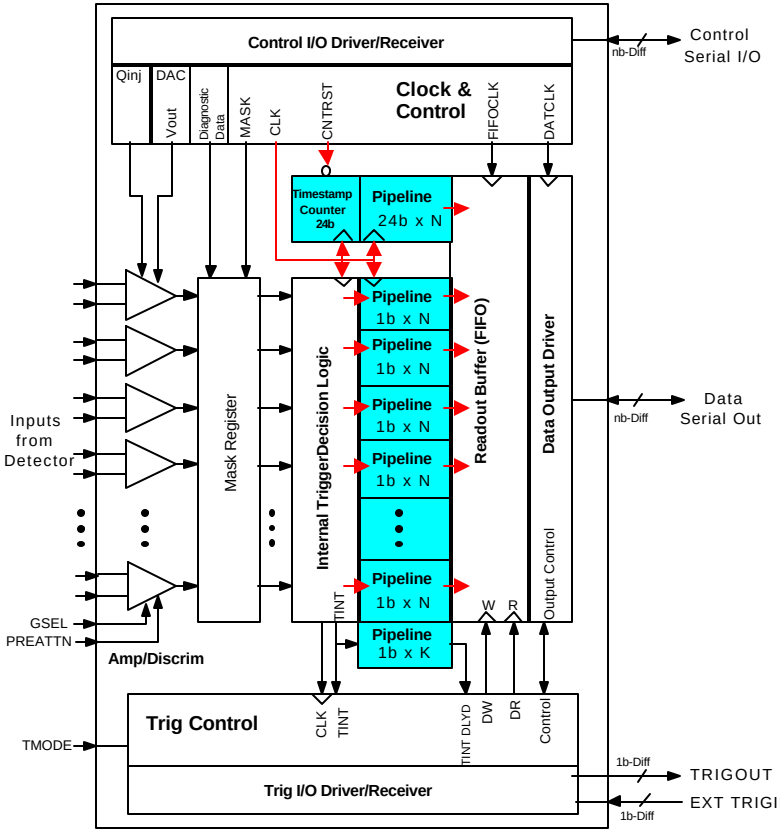
• Internal Trigger Signal Formation

- **Form *TINT* from "OR" of All Discriminators, Evaluated at End of Clock Cycle**
- **TINT Used for:**
  - Send Signal ***TRIGOUT*** to External Trigger System
  - Self-Trigger for Data
- **Copy of TINT is Delayed, Used to Capture Data in Self-Trigger Mode**



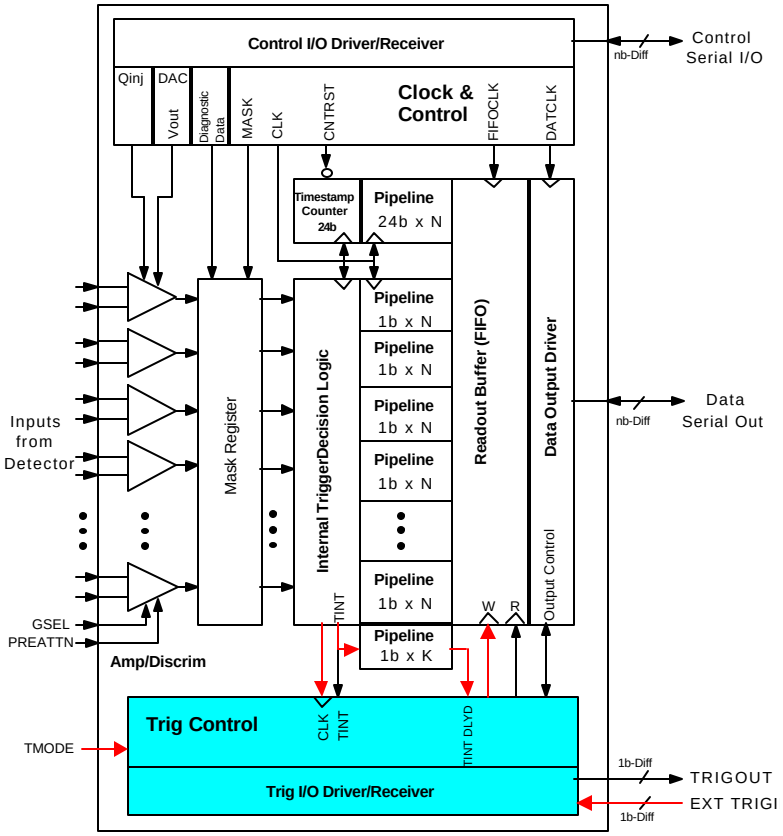
Front End ASIC

- **Pipeline & Timestamp**
  - **Pipeline:**
    - Pipeline for Ext. Trigger Decision
    - Bit Pattern Shifted Through Pipeline with 10 MHz Clock
    - Store Bits in Read-Out Buffer on Trigger Accept
    - 20 Stages of Delay = 2 uSec
  - **Timestamp:**
    - Timestamp Counter Runs at 10 MHz → 100 nS Resolution
    - Store Timestamps in Read-Out Buffer on Trig. Accept
    - Reset Counters Globally 1/Sec → Need 24 Bits



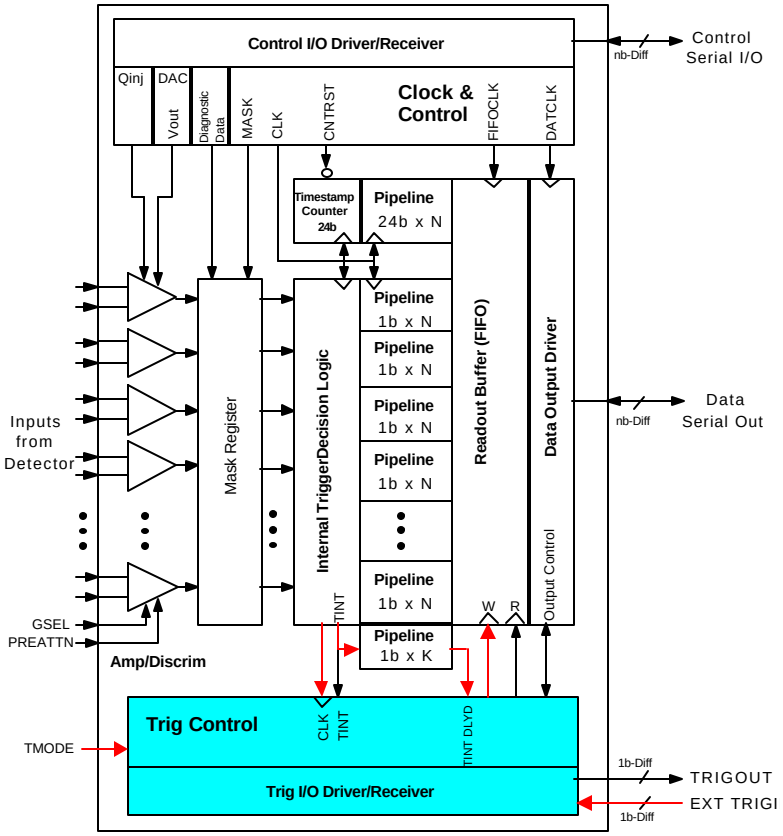
• Triggering Data for Readout

- **2 Trigger Modes:**
  - Self-Trigger:
    - » Auto-Generate Trigger Accept from "OR" of Discriminator States
    - » Timed to Capture Event of Interest at End of Pipeline
  - External Trigger
    - » Receive Signal from External Trigger System
    - » Required Timing Determined by Pipeline Depth



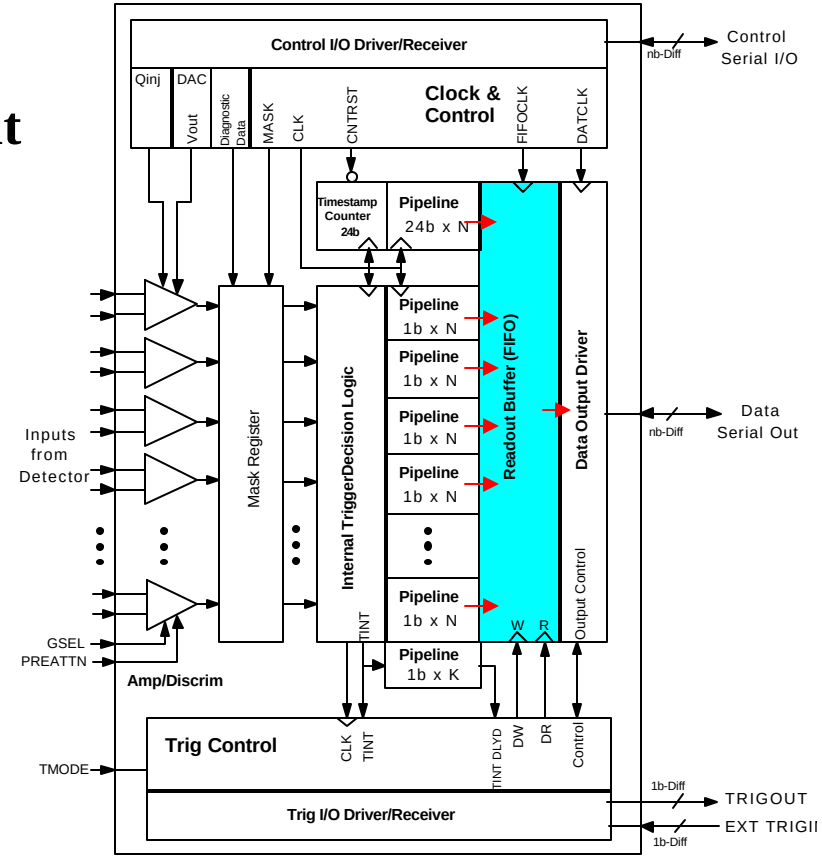
• Triggering Data for Readout (Cont.)

- **Trigger Mode Set by External Pin *TMODE***
- **In Either Case, Trigger Accept Writes Data from Pipeline into Readout Buffer**



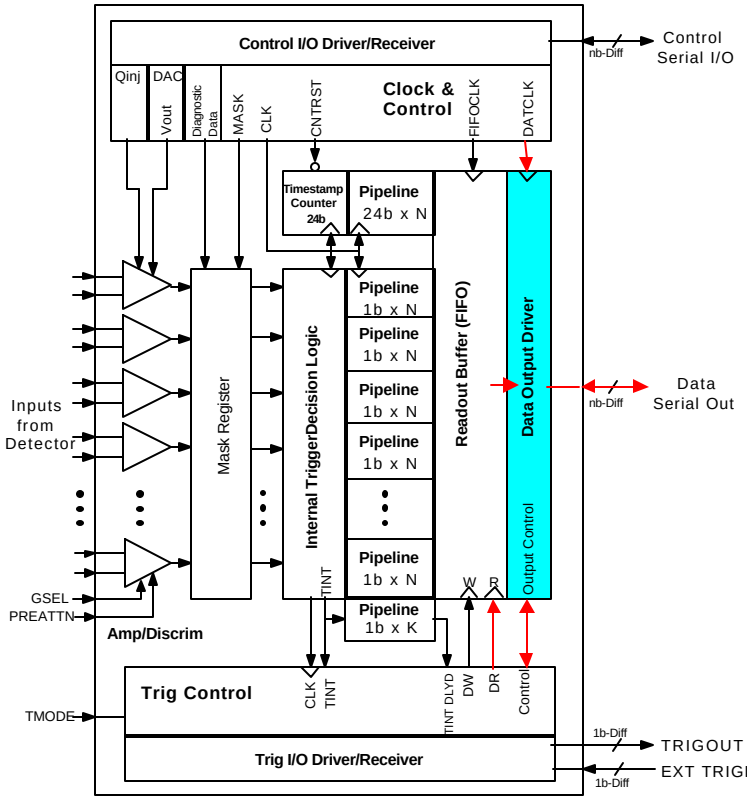
Front End ASIC

- **Readout Buffer**
  - **Trigger Accept Causes *Event Data* to be Written into Readout Buffer**
    - ***Event Data* is Defined as 64 Comparator States in a Given Clock Cycle, Plus 24 Bits of Timestamp**
  - **Readout Buffer Configured as FIFO, Capable of Storing 16 Events**
  - **When Readout Buffer NOT EMPTY, Control Circuitry Writes First Event to Output Driver for Transmission**



Front End ASIC

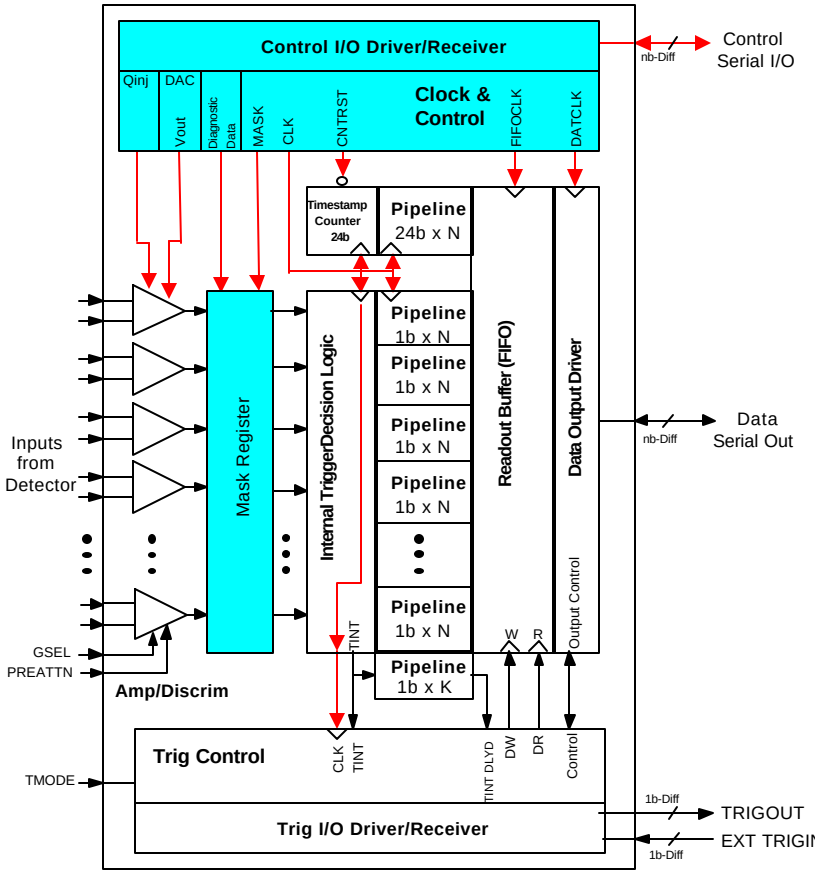
- **Output Driver**
  - **Receives Events from Readout Buffer**
  - **Serializes Data, & Transmits Using Serial Communication Protocol**
    - Handshake, Flow Control
    - Parity, Start, Stop, Data Bits
    - NRZ, Framing, ...
  - **Bit Slice Using 10 MHz Clock**
  - **Hardware Implementation: Differential Current Steering**



➢ **Prefer Standard, Commercial Hardware & Comm. Protocols**

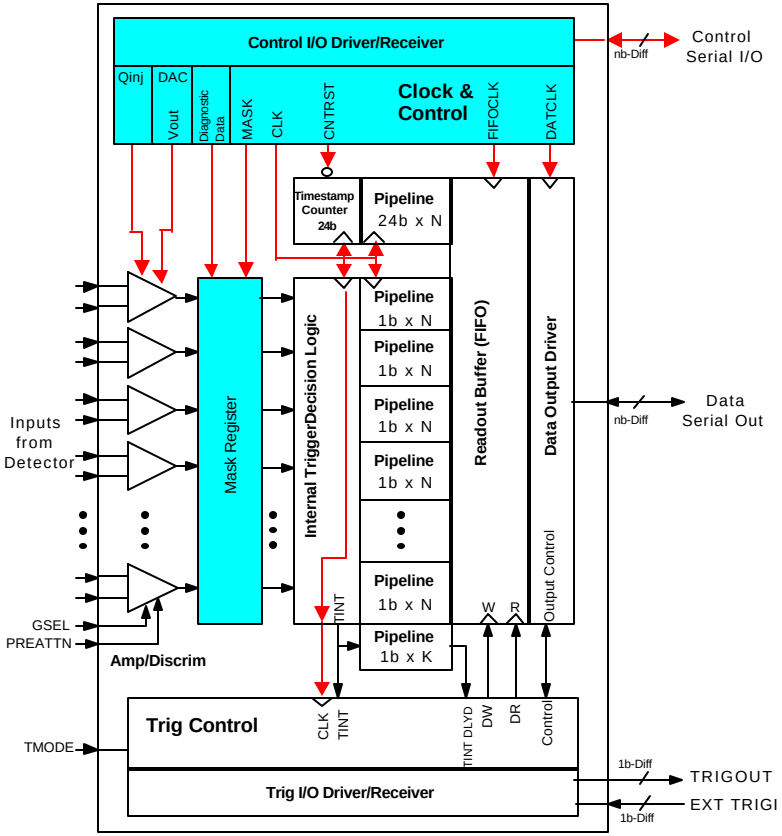
Front End ASIC

- **Control**
  - **3 Requirements for Control:**
    - Provide 10 MHz Clock
      - » Synchronized Over All Chips in System
    - Time-Critical Functions
      - » Counter Reset
      - » Charge Injection
    - Static Functions
      - » Read/Write Registers



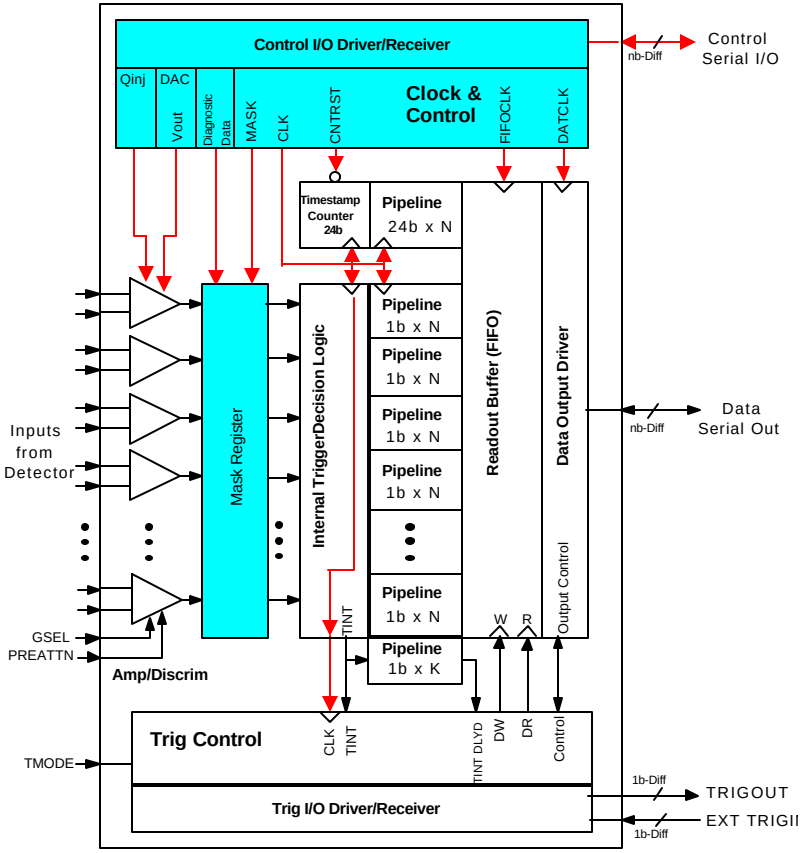
Front End ASIC

- **Control (Cont.)**
  - **Registers:**
    - Threshold DAC
      - » 6-7 Bit Dynamic Range
      - » Common to All Channels
    - Mask Register
      - » Mask Off Noisy Channels
    - Charge Injection
      - » Check All Channels Alive
      - » Calibrate Against Threshold (If Have Variable Charge…)
      - » Calibrate Timestamp (If Have Precision QINJ Time…)



Front End ASIC

- **Control (Cont.)**
  - **Registers (Cont.):**
    - Diagnostic Data
      - » Send Known Bit Pattern Out Data Link of Chip
  - **Bi-Directional Serial Communication Protocol**
    - Handshake, Flow Control
    - Parity, Start, Stop, Data Bits
    - NRZ, Framing, ...
  - **Bit Slice Using 10 MHz Clock**
  - **Hardware Implementation: Differential Current Steering**



Summary

- **Primary Goal of Electronics for RPCs:** ***CHEAP***
  - Low Event Rate (Mostly Noise)
  - Low Dynamic Range (1 Bit)
  - Low Clock Speed
  - Funnel Many Channels into a Read-Out Board (Reduce Expensive VME Real Estate)

- **Requires ASIC to Achieve Low Cost & Desired Performance**
  - Not Particularly Difficult, But Will Require Design Time
  - Chip Has Many Blocks, Each Block Relatively Straight-Forward
  - Need to Begin ASIC Development Soon
  - Conceptual Design Document Nearly Ready...

Summary

- **Still Needing Work:**
  - Front End PCB R&D
  - Serial Data Transmission Scheme & Format
  - Other Design & Performance Details of ASIC (Need Input from Chip Designers…)
  - Design of Data Concentrator
  - Timing
  - Trigger