Electronics
for
Linear Collider Digital HCAL

Presented By
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Outline of Talk

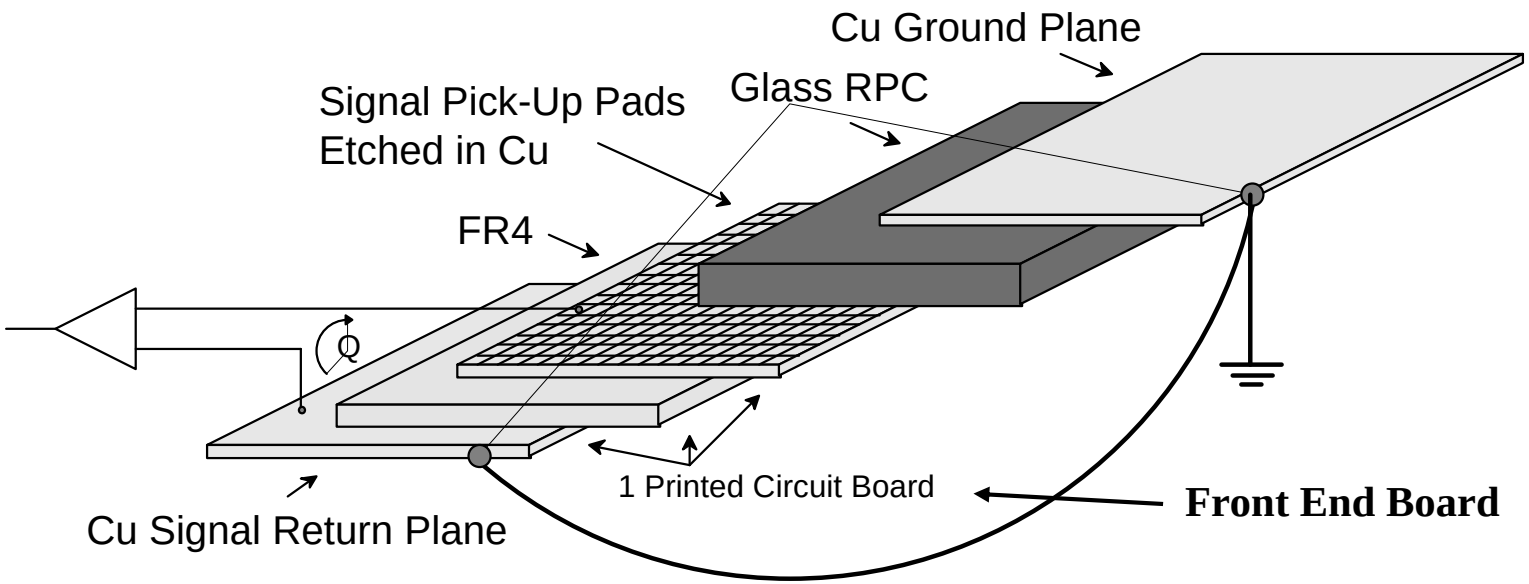
I. Detector Configuration
II. System Architecture
III. Implementation
IV. Summary of System Components
V. Overall Plan & Goals

See:

www.hep.anl.gov/drake/linear_collider/041217_meeting.pdf

Detector Configuration

- **Anatomy of the LC RPC**

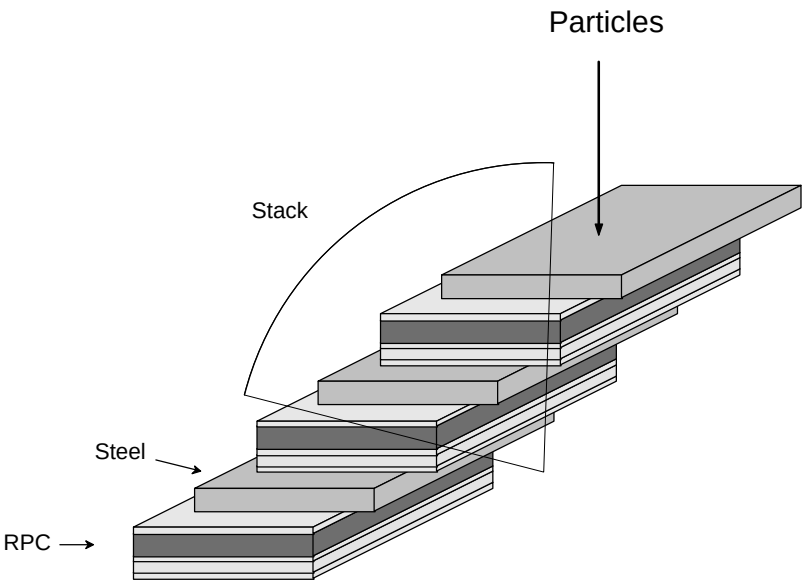


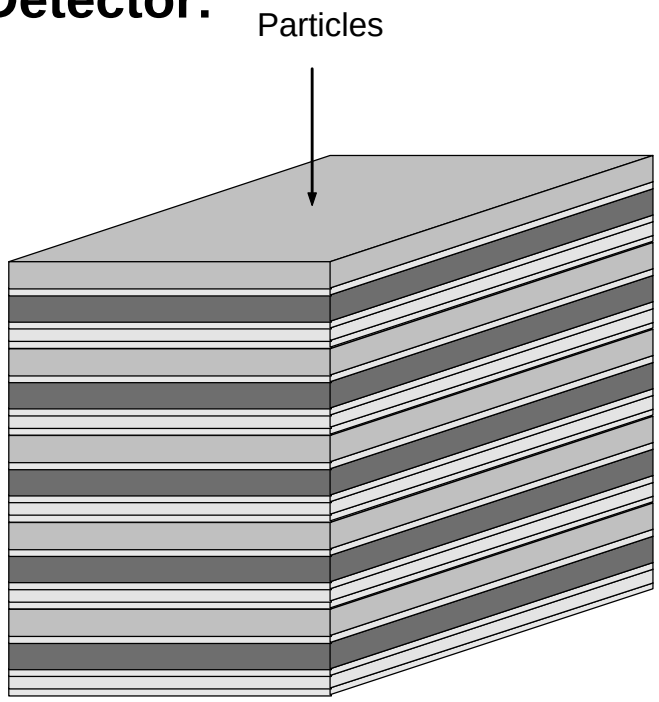
- Ionization in Gas of RPC Induces Signal on Pad(s)
- Fast Current Pulse Flows Between Pads & Signal Return
- Pulse Size Depends on Gas & HV - Streamer vs. Avalanche

⇨ ***We Will Use Avalanche Mode***

Detector Configuration

- **Anatomy of the LC RPC (Cont.)**
  - **To Make the Prototype Hadronic Detector:**

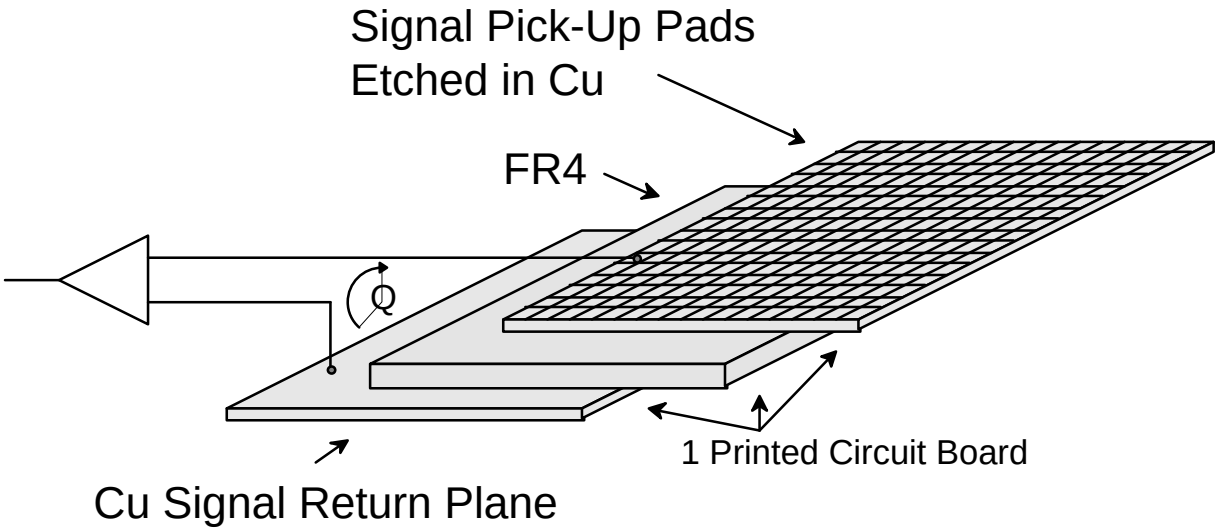




1 Cubic Meter "Prototype"
~400,000 Channels of RPC Readout
(Assumes 1 cm X 1 cm pads)

Detector Configuration

- **Anatomy of the LC RPC (Cont.)**



- **The Instrumentation Job:**
  - Receive Signals from Each Pad
  - Discriminate Signals as “Hits”
  - Tag Hits in Time to Facilitate Track Reconstruction

➢ ***Primary Goals:***

✶ ***1 Bit Dynamic Range***

✶ ***Large Number of Channels***

✶ ***Cheap Electronics***

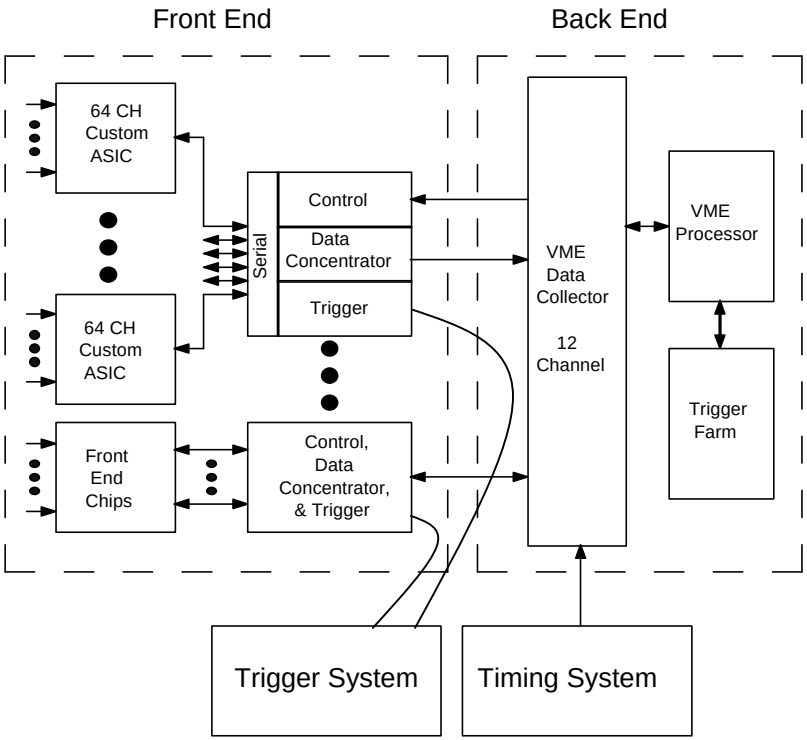
Detector Configuration

- **GEMs**
  - **Common Basic Architecture**
  - **Differences Accommodated in Front End ASIC**

Parameter	RPCs	GEMS
Type	Avalanche	(Gas)
Geometry	1cm x 1 cm Pads	1 cm x 1 cm Pads
Capacitance	10-100 pF	10-100 pF
Smallest Signal	~100 fC	~5 fC
Pulse Width	~5 nS	~3 nS
Rise Time	~2 nS	?
Largest Signal	~10 pC	~100 fC
Noise Rates	~0.1 Hz	?
Env. Noise Susceptibility	Low	Low

System Architecture

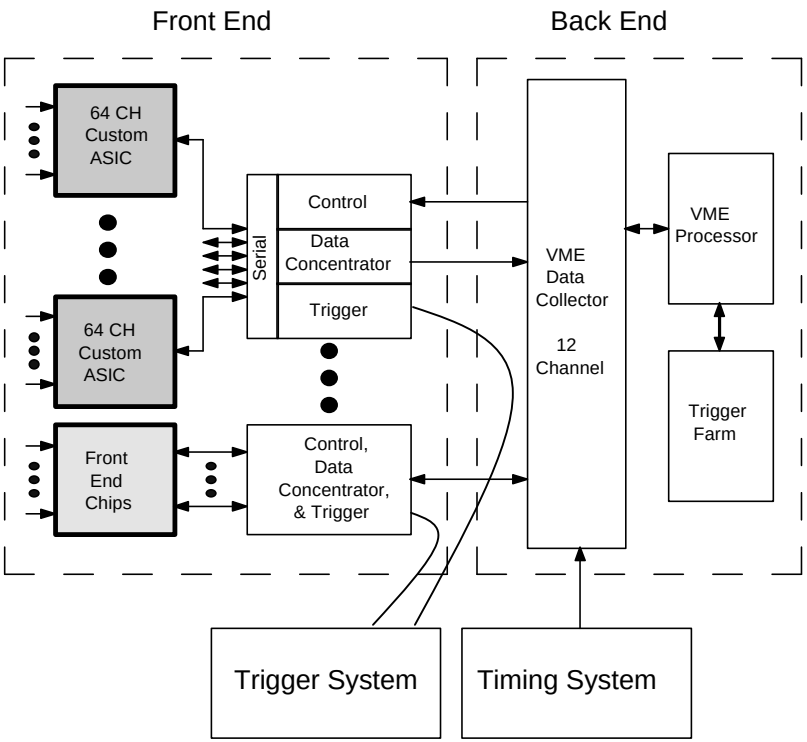
- **System Block Diagram**
  - ***Architecture Based Upon Assumption of Low Trigger Rate***
  - ***Events are Tagged with Timestamps at Front End to Allow Processing Latency***
  - ***Timestamps used for Event Reconstruction***
    - ® ***Similar to MINOS***



System Architecture

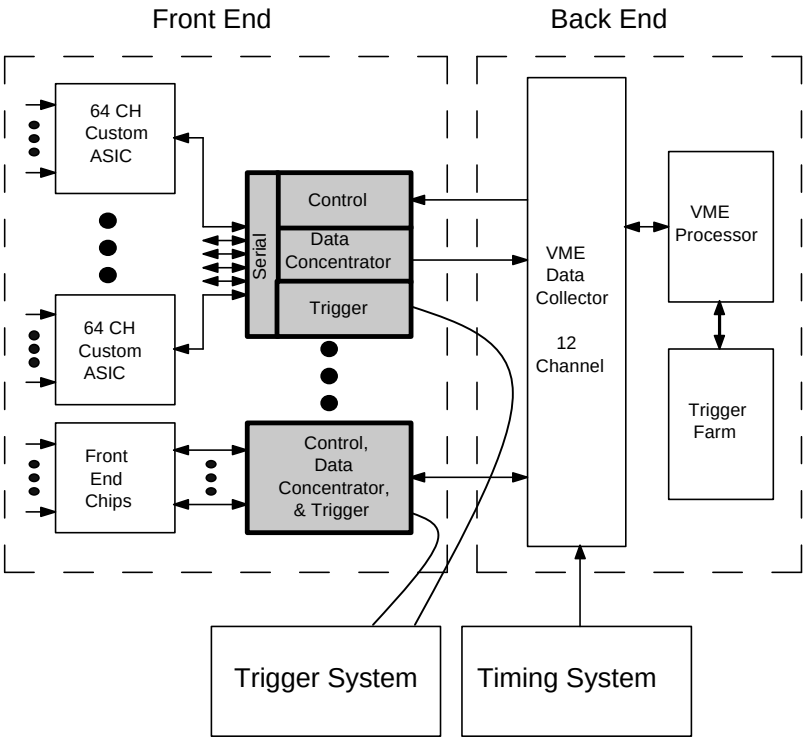
- **Front End**

- **Custom ASIC**
  - Performs Functions:
    - » Receive, Process, & Discriminate Detector Signals
    - » Timestamp Hits, & Record Hit Pattern
    - » Temporary Data Storage
    - » Serial Data Transmission
  - Can Self-Trigger, or Use External Trigger
  - Services 64 Detector Channels
- **Mother Board**
  - Chips Reside on Chamber



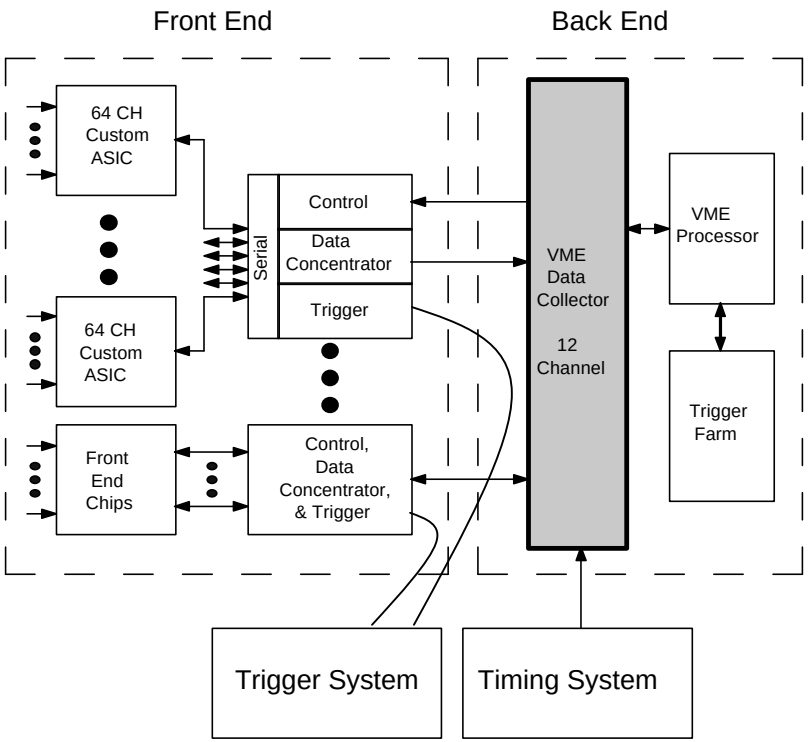
System Architecture

- **Front End (Cont.)**
  - **Data Concentrator:**
    - Concatenate Serial Data Streams from Several Chips ® Multiplexer
    - ***N*** Serial Lines In, 1 Serial Line Out
    - Drives Serial Line to Back End Read-Out Electronics
    - Handles Clock & Control Interface
    - Handles Trigger Interface



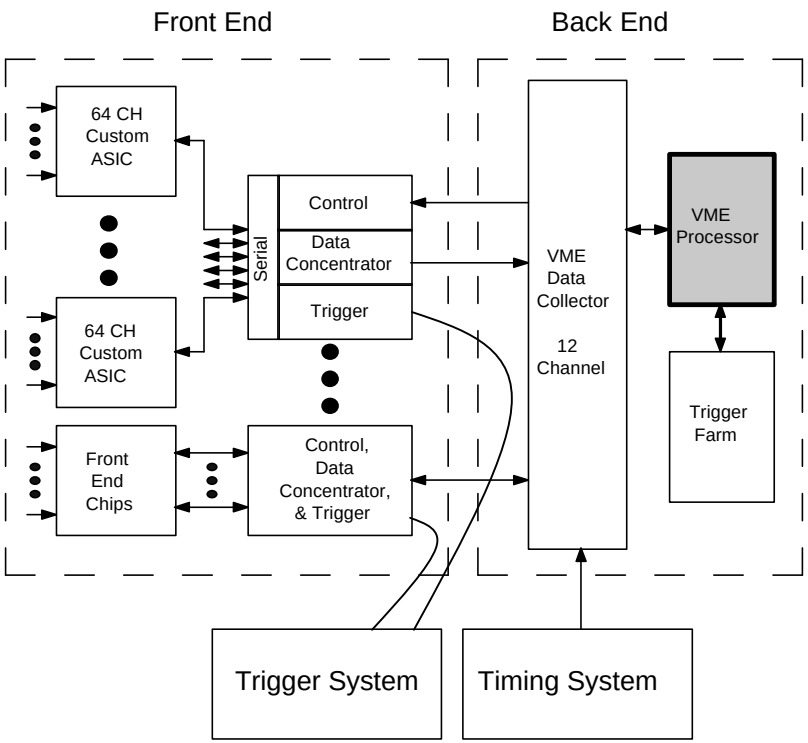
System Architecture

- **Back End**
  - **Data Collector:**
    - 9U x 400 mm VME
    - Receives Serial Data Streams from Several Data Concentrators
    - Stores Data in Buffers
    - Dual Buffers: Data Written into One While Processor Reads the Other
      - ® ”Buffer Swaps”
        - ® No Deadtime



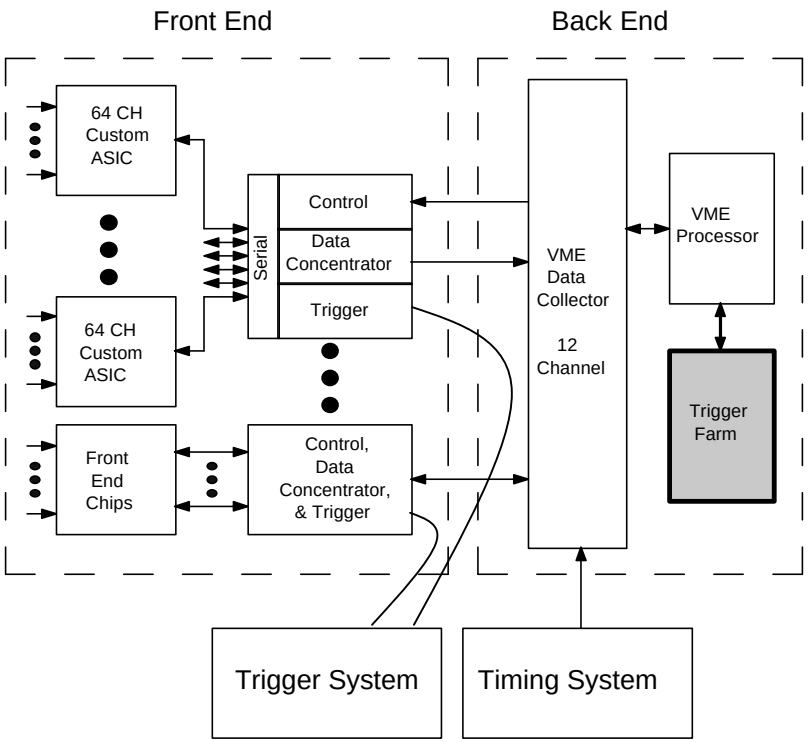
System Architecture

- **Back End (Cont.)**
  - **VME Processor:**
    - Buffer Swaps Coordinated by VME Timing Module using ISRs
    - Read Data from All Data Collectors in VME Crate
    - Forms Time Frames from Timestamps (~1 Sec)
    - Sends Time Frames to Trigger Farm for Processing



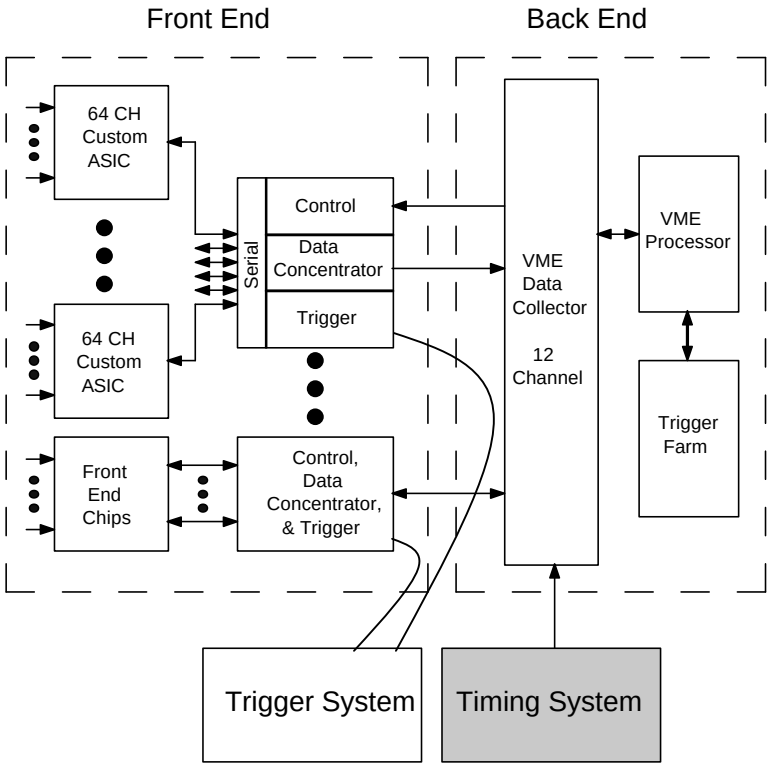
System Architecture

- **Back End (Cont.)**
  - **Trigger Farm:**
    - Receives Time Frames from All VME Processors in System
    - Uses Timestamps in Pattern Recognition Algorithm to Find Tracks
    - Write Good Data to Disk
    - Discards Junk



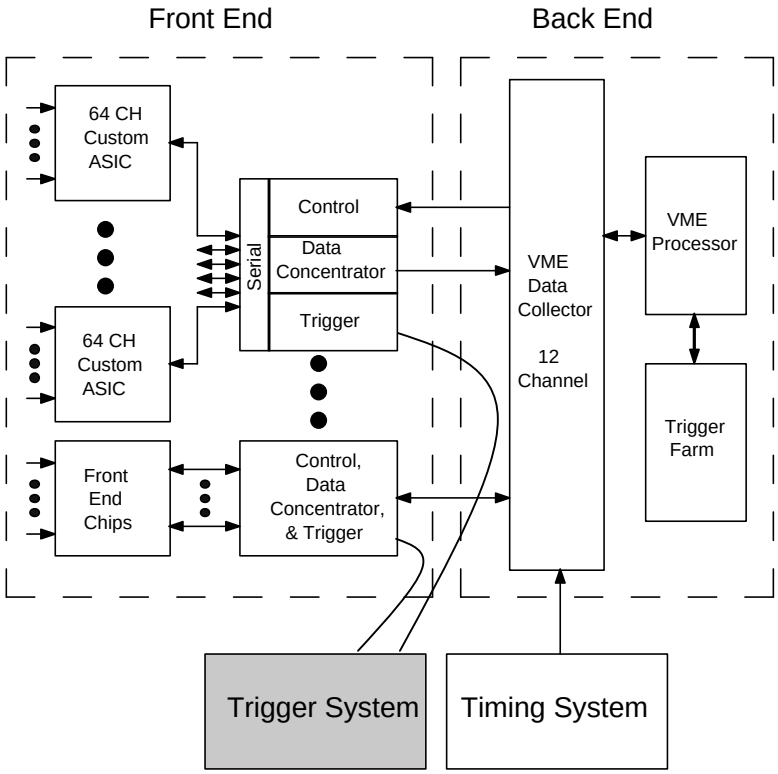
System Architecture

- **Timing System**
  - **Functions:**
    - Distribute Timing Signals to Front Ends for Timestamping
    - Provide Timing for Data Collectors & VME Processors
    - Interface to Beamline System



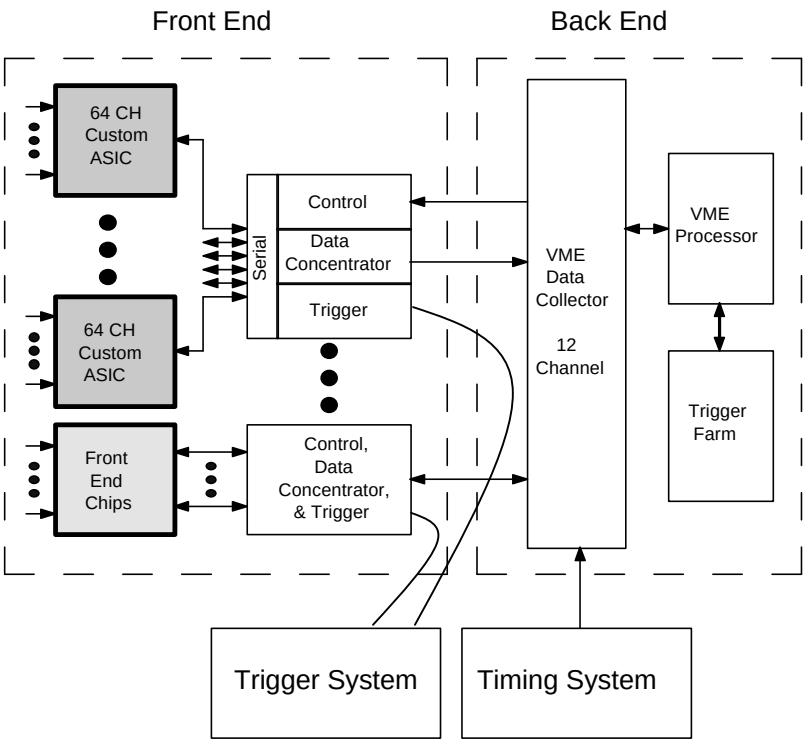
System Architecture

- **Trigger System**
  - **Functions:**
    - Simple Gate for Beam Spill
    - Trigger from Beam Telescope
    - Ability to Force Triggers to Study Noise
    - Interface to Other LC Systems Later



Implementation

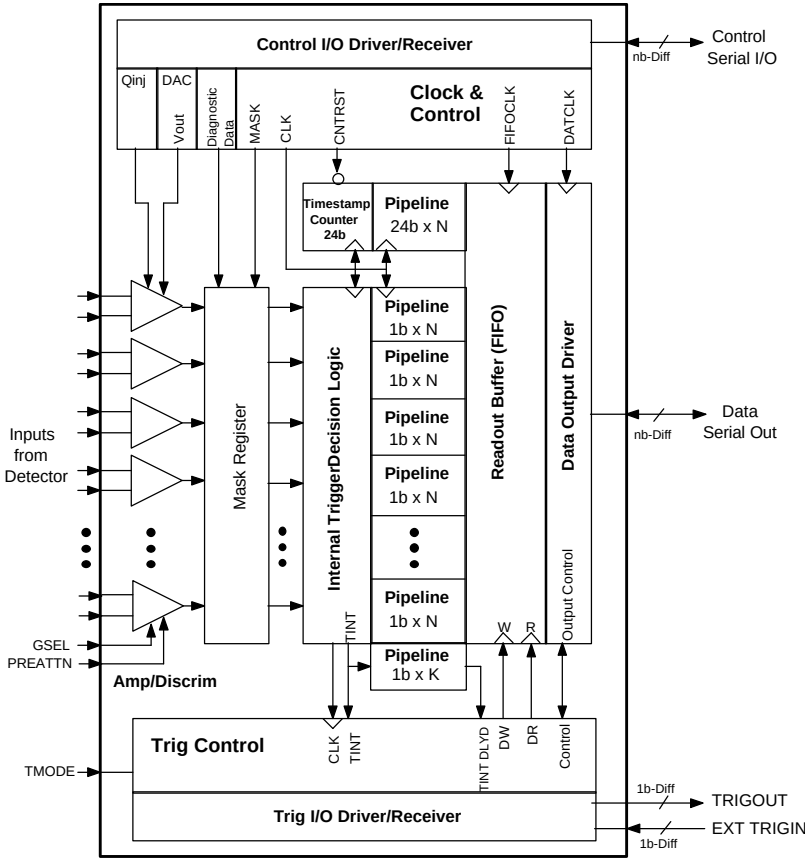
- **Front End**
  - **Custom ASIC**
  - **Front End PC Board (Pads for Chamber)**



Implementation

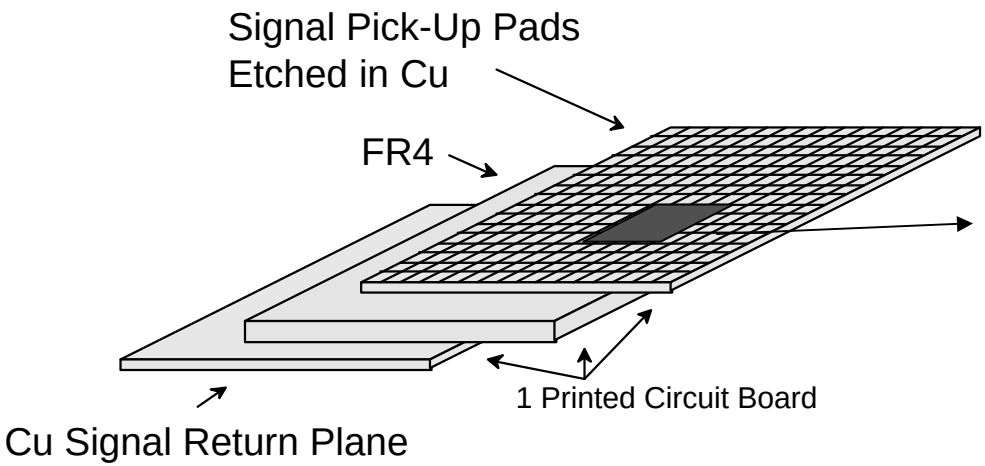
- **Front End (Cont.)**
  - **Custom ASIC**
    - Front End Amplifier & Discriminator Senses Hits Above Threshold
    - 24-Bit Timestamp Counter Runs at 10 MHz
    - Comparator States Clocked into Shift Register
    - Save States & Timestamp on Ext. Trig. or Self-Trigger
    - Serial I/O – Separate Data, Control, & Trigger
    - Services 64 CH

⇨ ***Design in Progress at FNAL...***



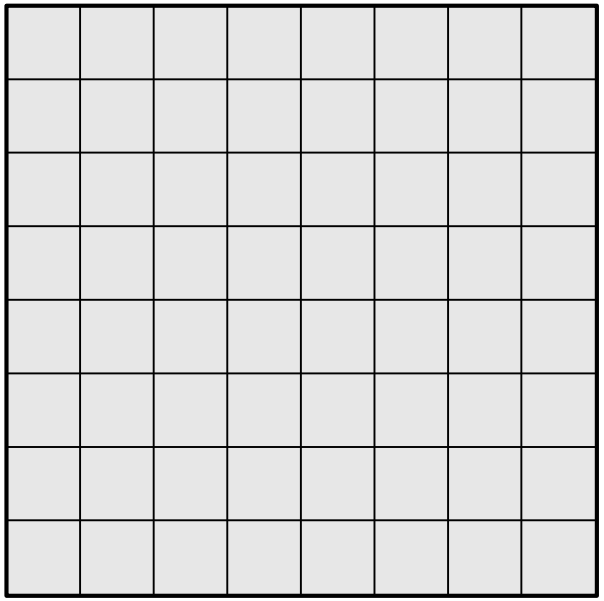
Implementation

- **Front End (Cont.)**
  - **Front End PC Board (Pads for Chamber)**



Basic Cell Grouping: 8x8 Cells

8 x 8 RPC Cell Array
(Part of Single RPC Chamber)

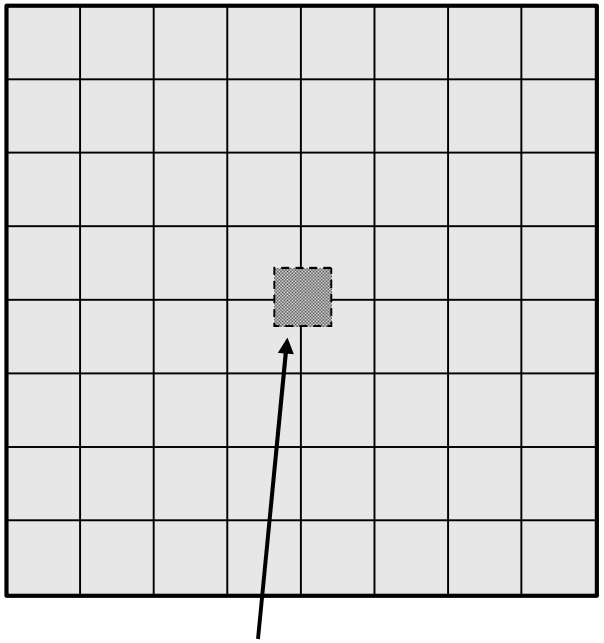


Implementation

- **Front End (Cont.)**
  - **Front End PC Board (Cont.)**
    - Design Multi-Layer Printed Circuit Board
    - Incorporate Cell Structure and Signal Layers in Single PCB
      - » Detector Signals
      - » Digital I/O
      - » Power & Ground

⇨ ***ASICs on Detector.***

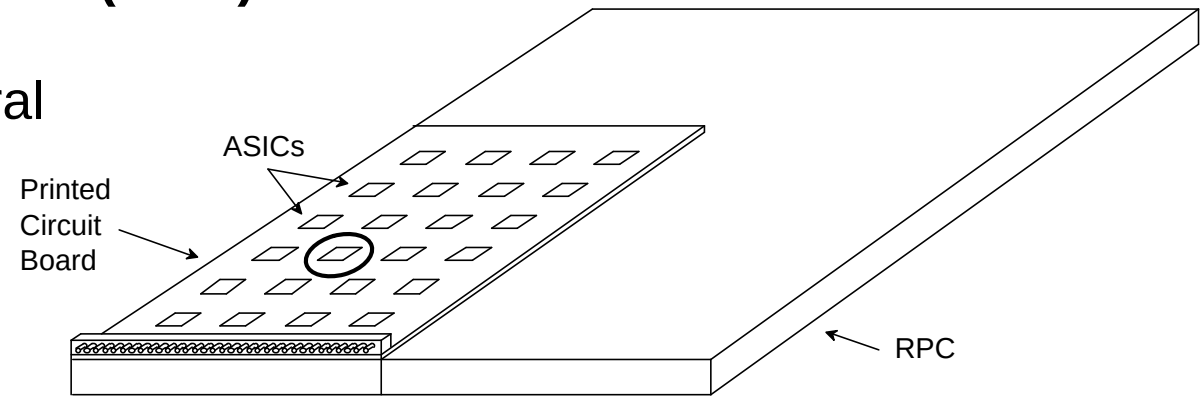
8 x 8 RPC Cell Array
(Part of Single RPC Chamber)



ASIC on Opposite Side of Pads

Implementation

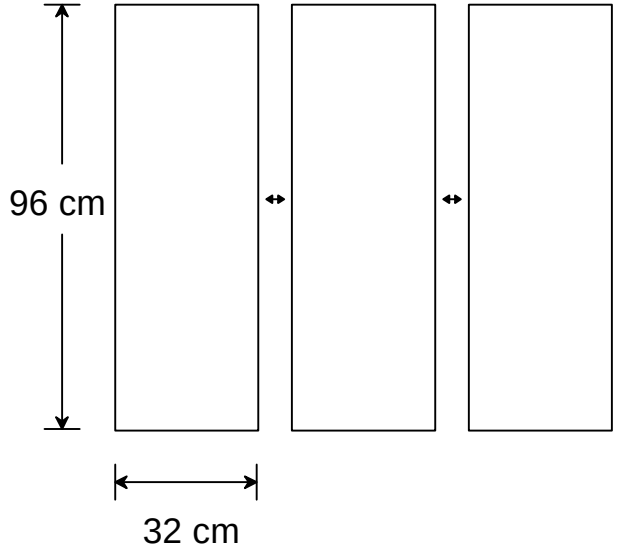
- **Front End (Cont.)**
  - **Front End PC Board (Cont)**
    - One PCB Contains Several 8x8 Arrays with Chips
    - Arrange Data Connectors on Outside Edge of Chamber



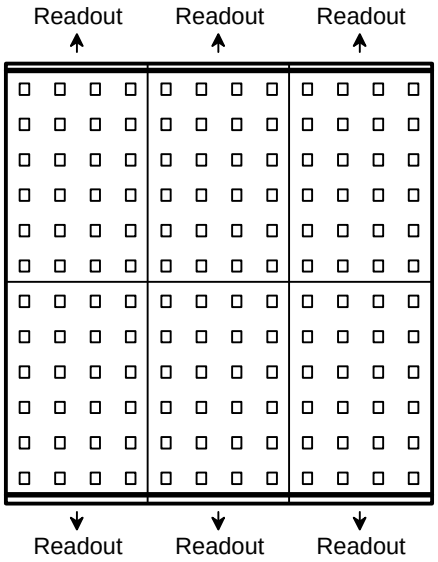
- **Short Detector Signal Transmission Path,**
  Low Input Capacitance, Close to What is Needed in Final Design,
  No Dead Spaces from Circuitry, Low Assembly Labor
- **Digital Noise, Board Complexity** ⇨ ***Likely to be Challenging...***

Implementation

- **Front End (Cont.)**
  - **Front End PC Board (Cont)**



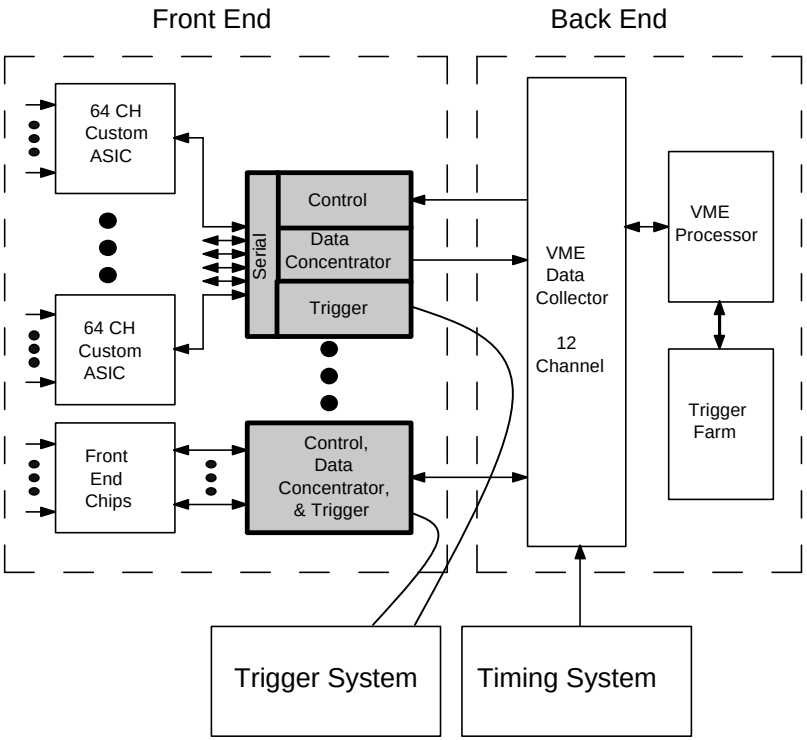
3 Chambers Form a Plane



2 Front End Boards/Chamber
6 Front End Boards/Plane
24 ASICs/Board
144 ASICs/Plane
9216 Channels/Plane

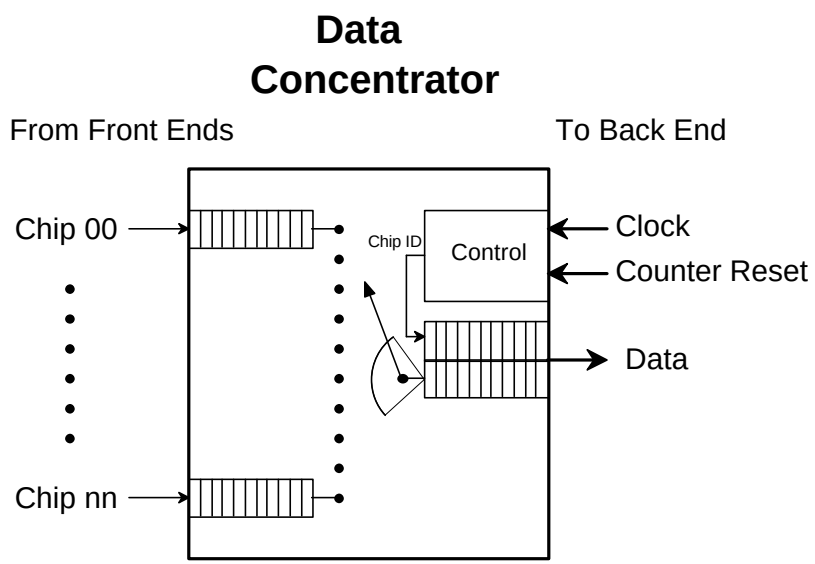
Implementation

- **Front End (Cont.)**
  - **Data Concentrator**
  - **Data Concentrator PC Board**



Implementation

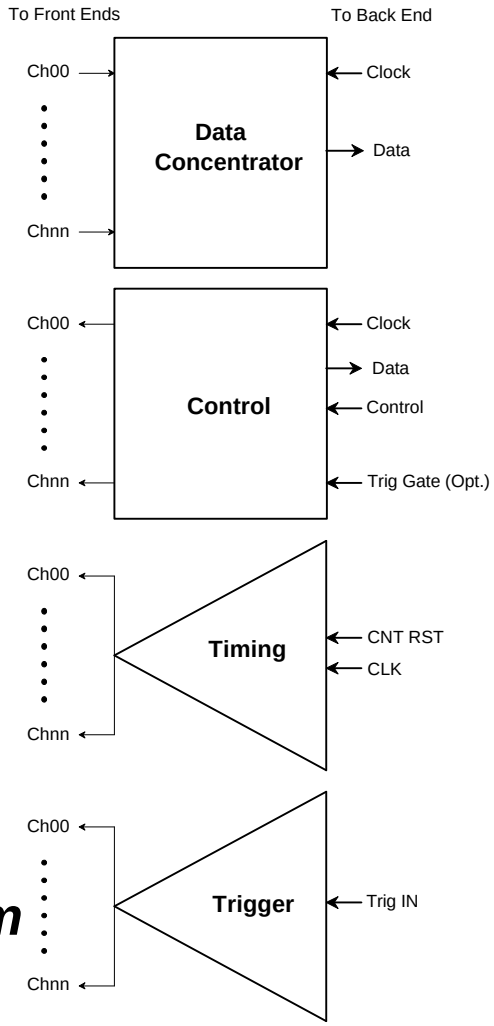
- **Front End (Cont.)**
  - **Data Concentrator (Cont.):**
    - Acts as Funnel for Data
    - Adds Chip ID to Data
    - Has Buffering
    - LVDS Inputs
    - High-Speed Output



- ***Needed to Reduce Back-End Costs - Expensive VME***
- ***Relies on <u>Low</u> Trigger Rate***
- ***Implementation with FPGAs***

Implementation

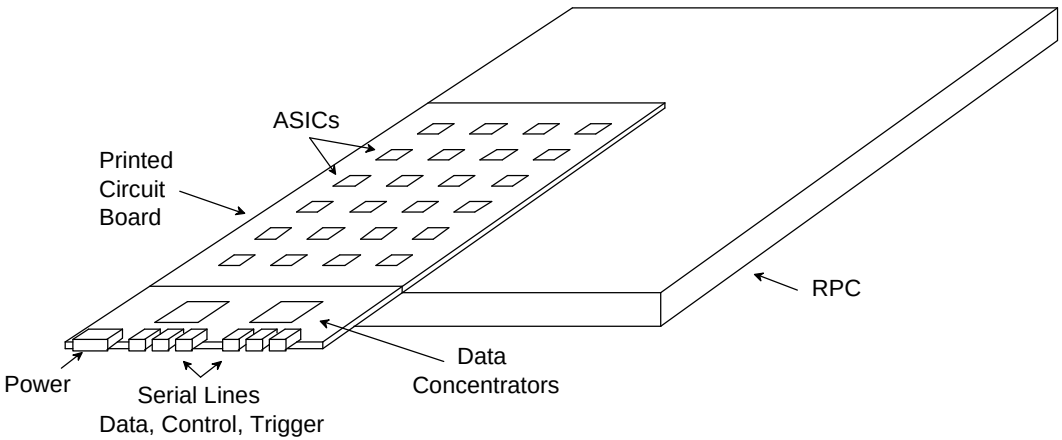
- **Front End (Cont.)**
  - **Data Concentrator (Cont.):**
    - Control
      - » Handful of Control Functions Needed for Chips
      - » Use Trigger Gate for Test Beam?
    - Timing
      - » Clock - Critical, 10 MHz Dist
      - » Counter Reset - Critical, Sync to 1 Clock Cycle Over Detector
    - Triggering
      - » Distribution of External Trigger



- ***LVDS I/O***
- ***Challenge to Reduce Lines to Minimum***

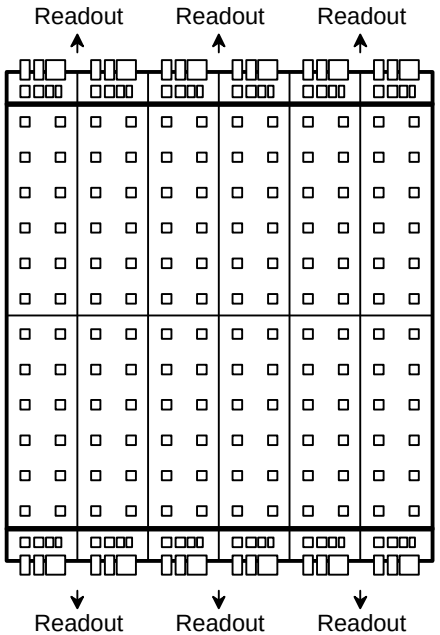
Implementation

- **Front End (Cont.)**
  - **Data Concentrator PC Board**
    - Host for Data Concentrator Circuitry
    - Plugs Into Front End Board
    - Interface for Power Distribution
    - Forms Integral Unit with Front End PC Board



Implementation

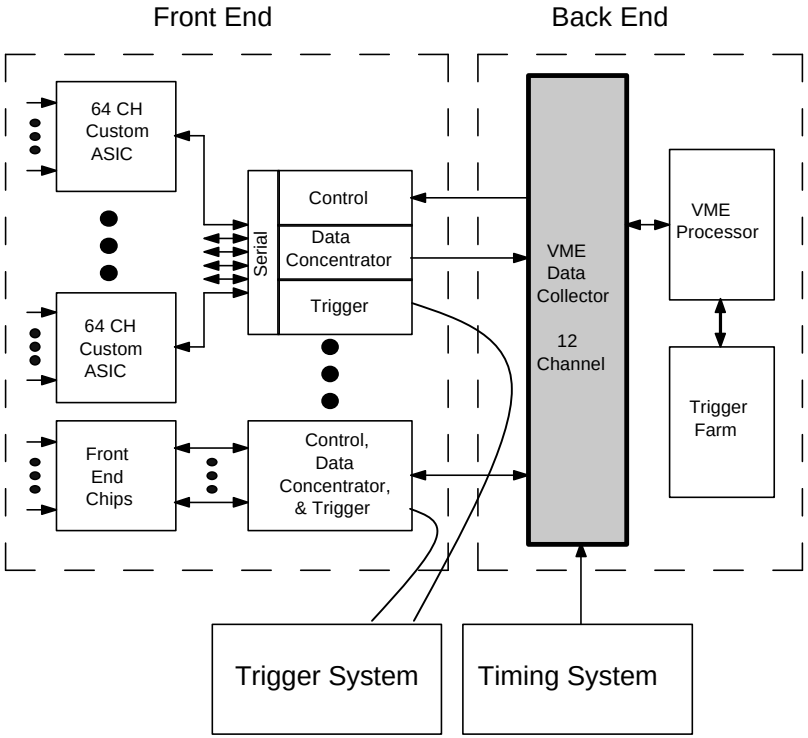
- **Front End (Cont.)**
  - **Data Concentrator PC Board**
    - Each Data Concentrator Reads Out 12 Chips, or 768 Channels



6 Front End Boards/Plane
24 ASICs/Board
2 Data Concentrators/FEB
12 Data Conc./Plane

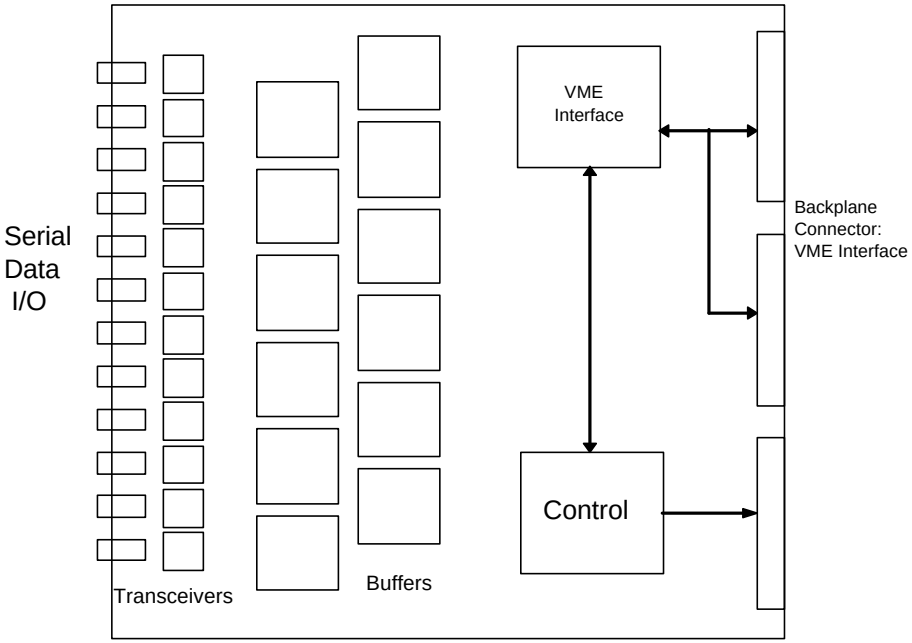
Implementation

- **Back End**
  - **VME Data Collector**



Implementation

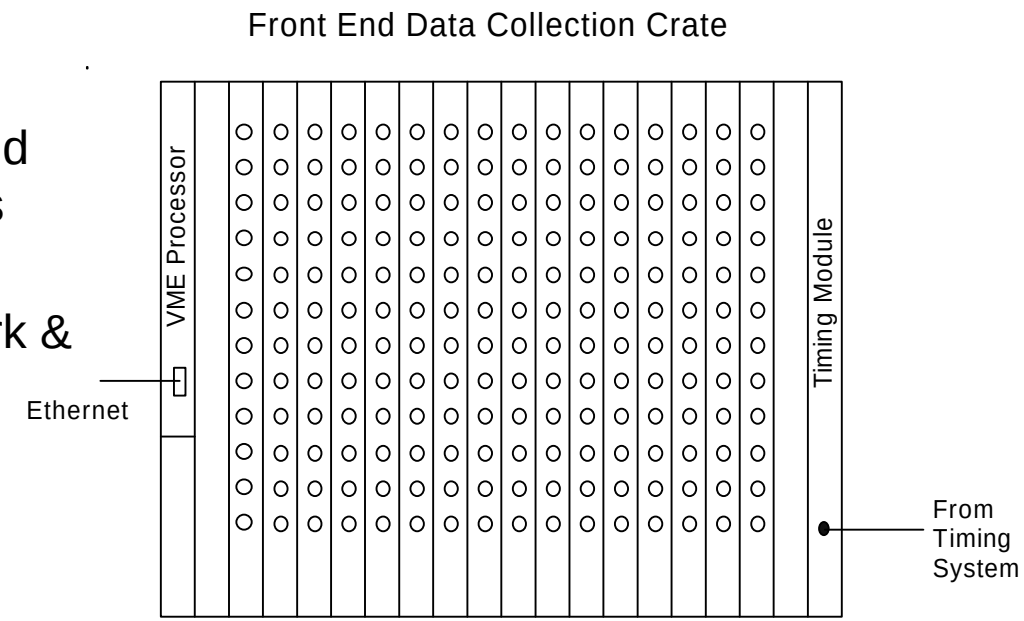
- **Back End (Cont.)**
  - **VME Data Collector (Cont.)**
    - Conceptual Implementation: 9U x 400mm VME, 12 Inputs
    - Receives Data Streams
    - Buffers Read from VME
    - Also Provides Control on Separate Path
    - Extensive Use of FPGAs - Provides High Degree of Flexibility



⇨ ***Each Data Collector Reads Out 1 Plane!***

Implementaton

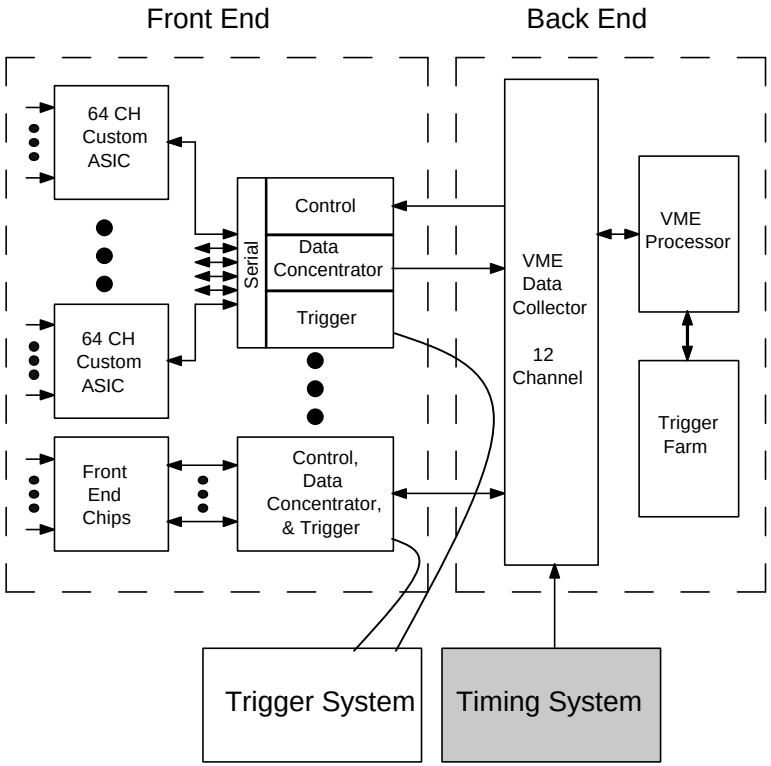
- **Back End (Cont.)**
  - **VME Data Collector (Cont.)**
    - VME Crate Can Hold ~16 Data Collectors
    - VME Processor Connects to Network & Trigger Farm



⇨ ***Need ~3 Crates***

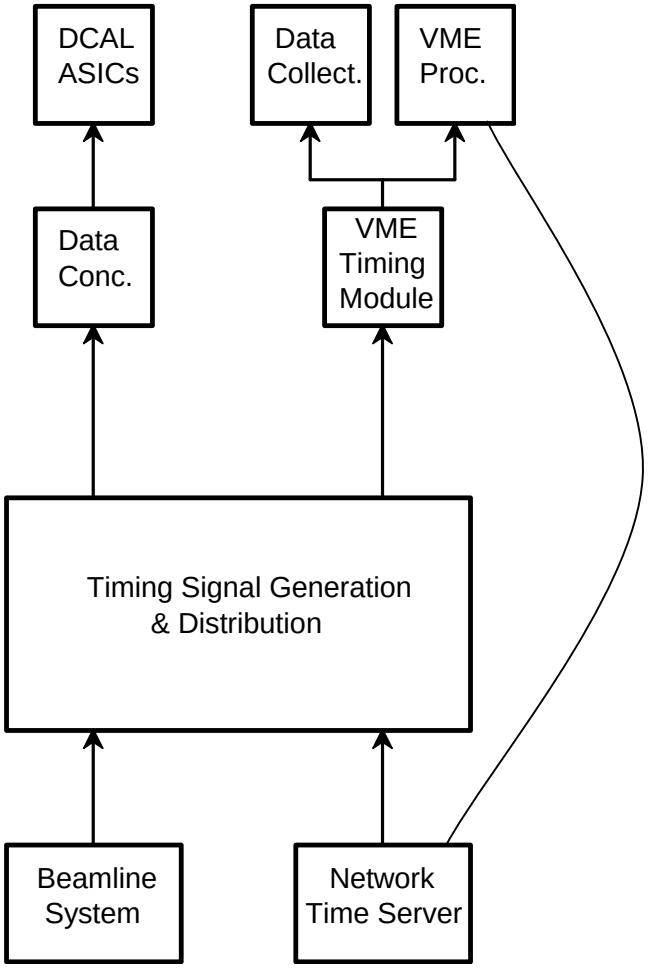
Implementation

- **Timing System**



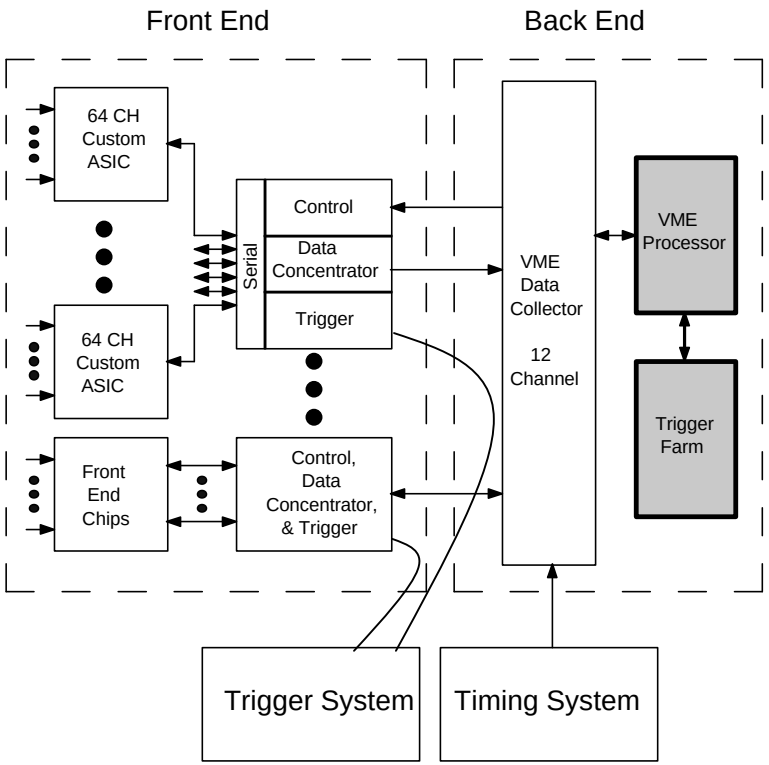
Implementation

- **Timing System**
  - **Functions:**
    - Distribute 53 MHz Clock to Front End Chips for Timestamping (100 nS)
    - Distribute Counter Reset to Front End Chips for Synchronization
    - Generate Buffer Swaps & 1 Sec. Time Frame Signal for Data Collectors & VME Processors
    - Interface to Beamline System



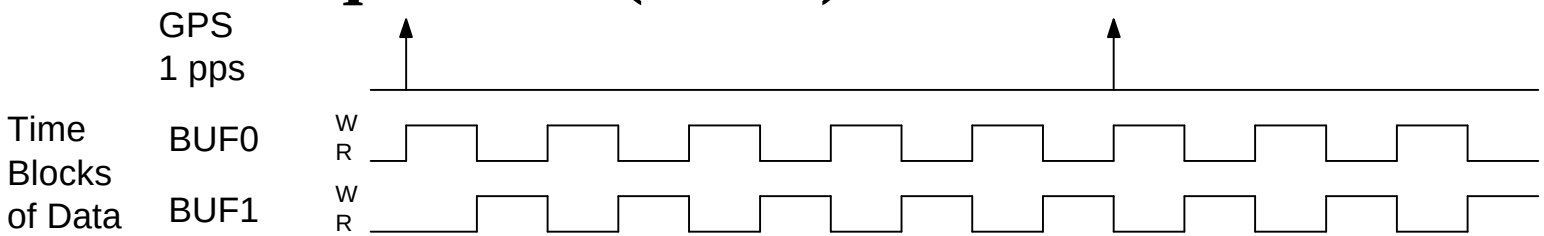
Implementation

- **Data Acquisition**
  - **VME Processor & Trigger Farm:**



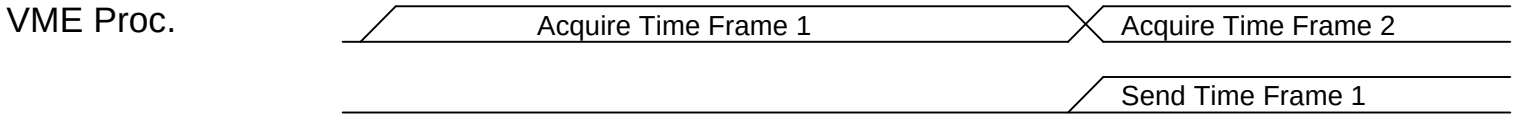
Implementation

- **Data Acquisition (Cont.)**

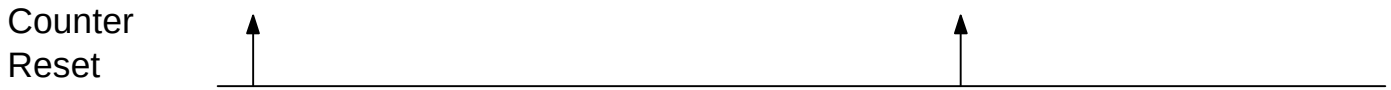


Time Blocks of Data Acquired from Data Collectors by VME Processor.
Time Blocks Concatenated Over 1 Second to form a Time Frame
Buffer Swaps Controlled by VME Timing Module using VME ISRs.
All Data Collectors Operate Synchronously, Along with VME Processor.

At 1 pps Intervals, VME Processor Sends Time Frame to Trigger Proc..

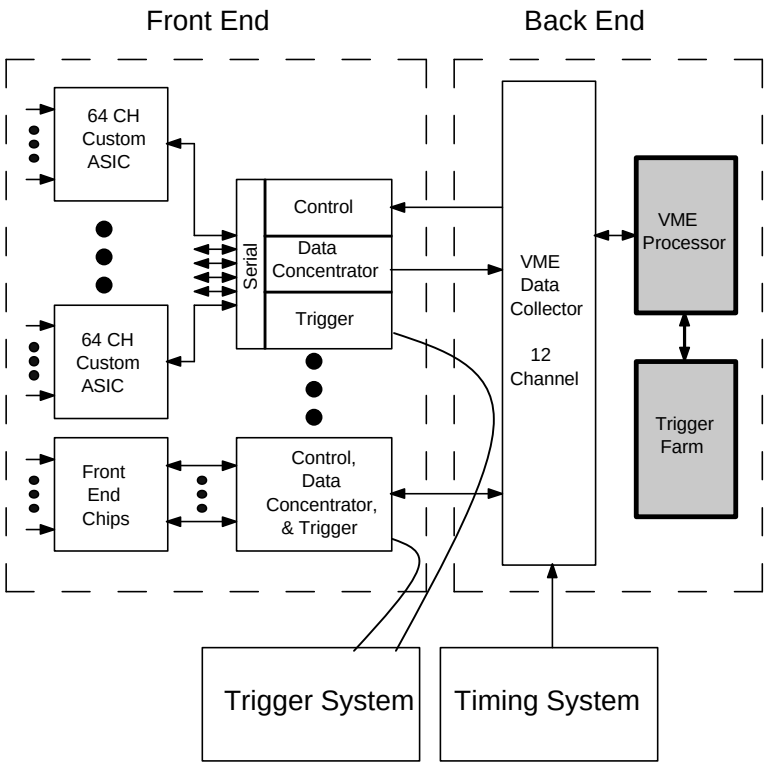


Timestamp Counters in Front Ends Also Being Reset by 1 pps



Implementation

- **Data Acquisition**
  - **VME Processor & Trigger Farm:**
    - Trigger Processor Receives data from 1 Second Interval from Entire Detector
    - Timestamps are Unique in a Given Record
    - TP Sorts Data in Time
    - Using Geometry Info, Then Find Events in Time & Space
    - Isolated Hits are Noise
    - Save Good Events to Disk



Summary of System Components

- **Counts of Components**

Component	#/Chamber	#/Plane	Total
Planes	-	1	40
Chambers	1	31	120
DCAL ASIC	24	144	5760
FE Bds	2	6	240
Data Conc.	4	12	480
Data Collector	-	1	40
VME Crates	-	-	3

⇨**368,640 Readout Channels**

Summary of System Components

- **List of Primary Design Subprojects**
  - **Front End ASIC** ⇨ *FNAL ASIC Design Group*
  - **Front End PC Board** ⇨ *Need Strong Analog Experience*
  - **Data Concentrator & Host PC Board** ⇨ *Digital Design*
  - **Data Collector** ⇨ *Digital Design*
  - **DAQ, Inc. VME Processor, DAQ Code, Network Comm.** ⇨ *VME Processors & Prog.*
  - **Trigger Processor, Inc. On-Line Trigger Algorithms, Event Selection, Event Archiving** ⇨ *Trigger Algorithms*
  - **Timing System** ⇨ *Timing System Design, Signal Distribution*
  - **Trigger System** ⇨ *Trigger Signal Distribution*
  - **Infrastructure, Inc. Crates, Power Supplies, Cabling** ⇨ *Power Systems*

Summary of System Components

- **List of Primary Design Issues**
  - **Front End ASIC**
    - Analog Signal Processing
    - Final Control Protocol
    - ***Testing of 1st Version of Chip - Bench, CR Teststand***
  - **Front End PC Board**
    - Routing Details, PCB Layers, Power Dist., Digital Noise Abatement
    - Connections Between Boards
    - Connection to Data Concentrator
    - Minimization of Support Components

Summary of System Components

- **List of Primary Design Issues (Cont.)**
  - **Data Concentrator & PC Board**
    - Nature of Output Data Link
      - ⇨Noise & Event Rate
        - ⇨Bandwidth
    - Nature of Control Interface & Implementation
  - **Data Collector**
    - Input Data Link
    - Control Interface

Summary of System Components

- **List of Primary Design Issues (Cont.)**
  - **DAQ, Inc. VME Processor, DAQ Code, Network Comm.**
    - Understand Bandwidth & Event Rates
    - Specify Platform & Op. Sys.
  - **Trigger Processor, Inc. On-Line Trigger Algorithms, Event Selection, Event Archiving**
    - Understand Bandwidth & Event Rates
    - Implement Sorting & Event Selection Algorithms
    - Specify Platform & Op. Sys.

Summary of System Components

- **List of Primary Design Issues**
  - **Timing System**
    - Identification of Signals
    - Specification of Sources and Destinations
    - Nature of Distribution
  - **Infrastructure, Inc. Crates, Power Supplies, Cabling**
    - Needs Complete Specification

Overall Plan & Goals

- Begin Design Effort & Meetings After Jan. 1
- Draft of Specifications for All Subsystems By Mar. 1
- 1st Round of Prototype Development Through Summer
- Begin Subsystem Tests with Fake Data Sources ~Fall 2005

- Chip Tests ~Aug., 2005
- Chip Production Starts ~Oct., 2005
- Packaged Chips Feb., 2006?

- Begin Small System Tests ~Mar., 2006
- Begin Final Production ~June 1, 2006