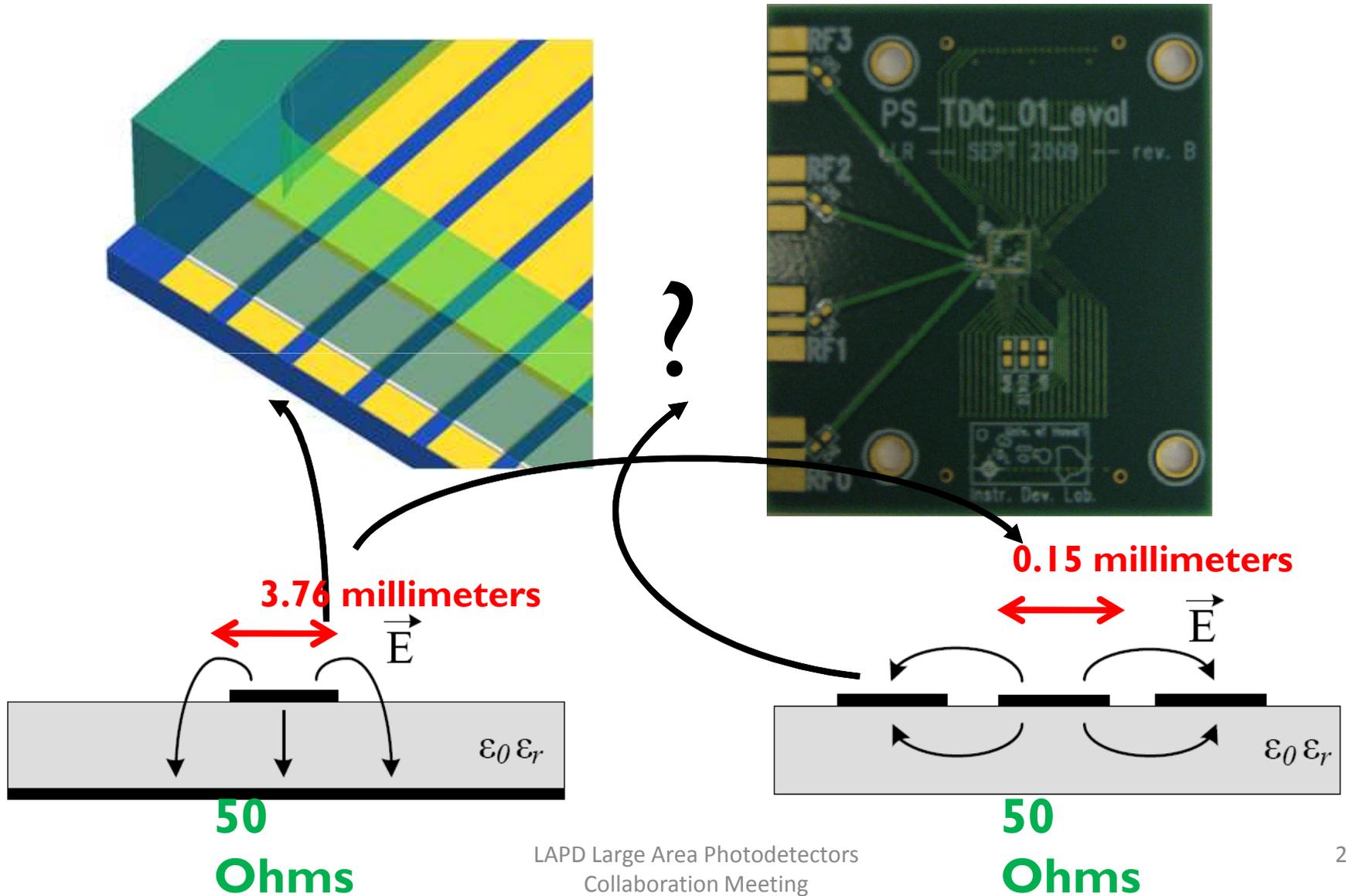


Detector to chip assembly

Detector to chip



General assembly: idea 1



On PCB:

Sampling ASICs (bump bonded)

FPGA (bump bonded)

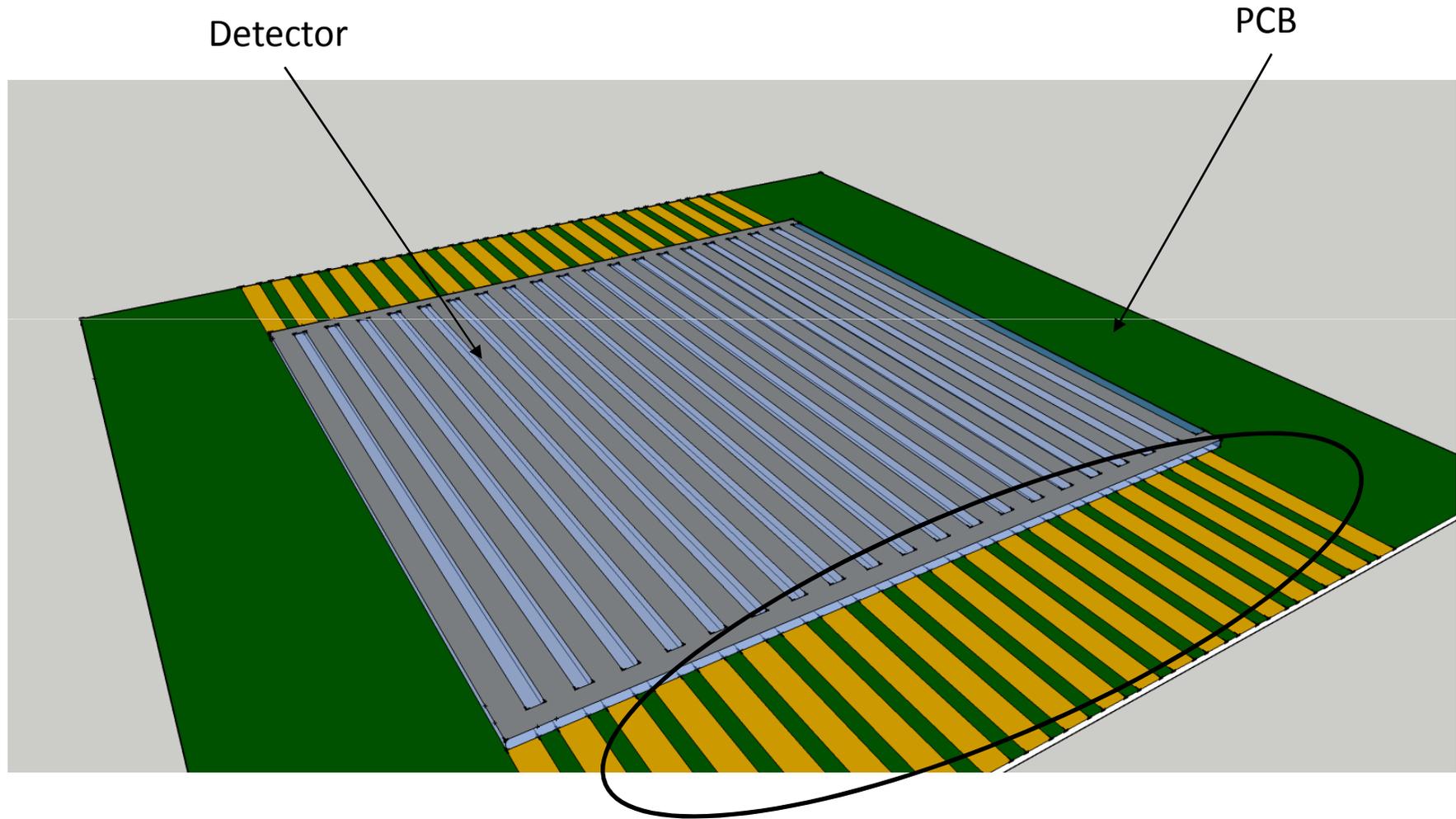
Opto: Clock in, Trigger in, Data out

Clock chip (phase, jitter)

Power: Voltage regulators, High voltage

Power planes

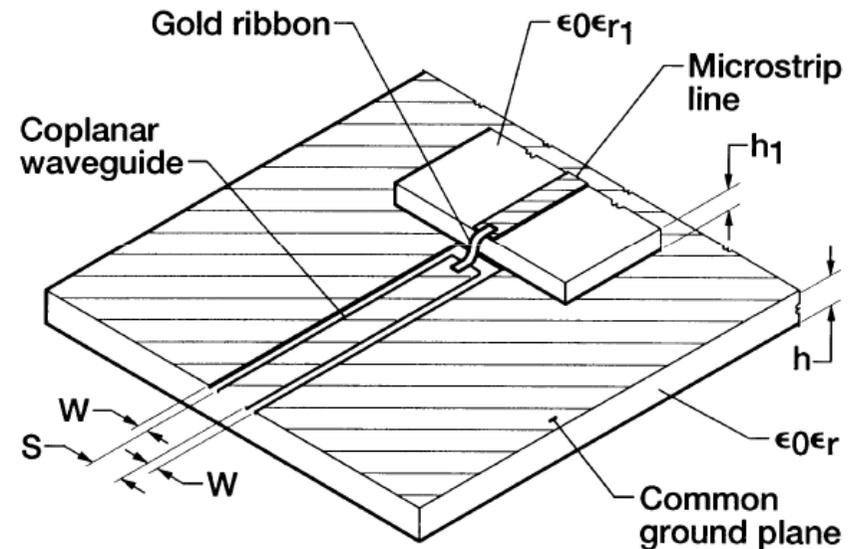
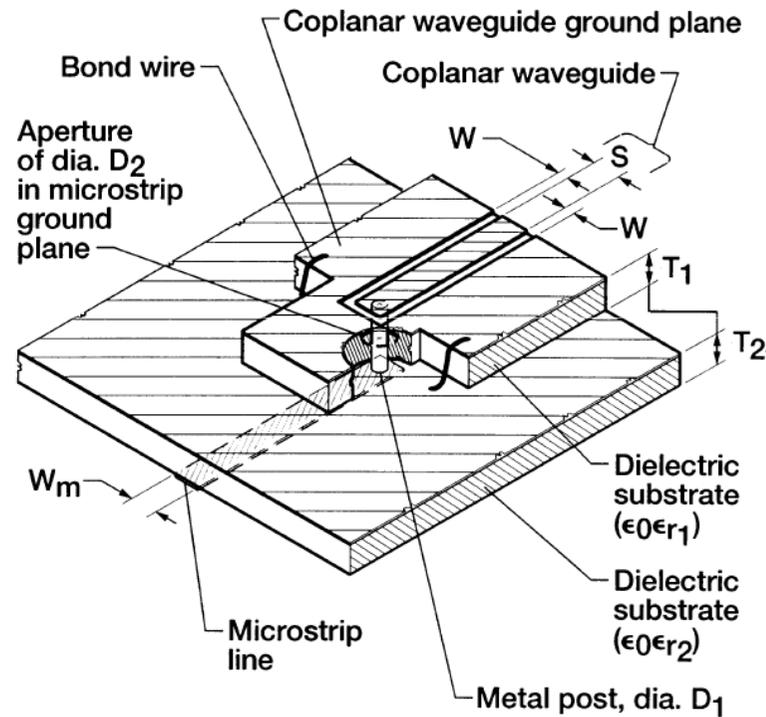
General assembly: idea 2



Electronic readout here

Idea 2: The connexion

Mixing of these two ideas



For a better timing and 50 Ohms matching a more clever structure can be think of. But this should be good enough -> will be simulated, designed and tested.