Picosecond sampling chip design

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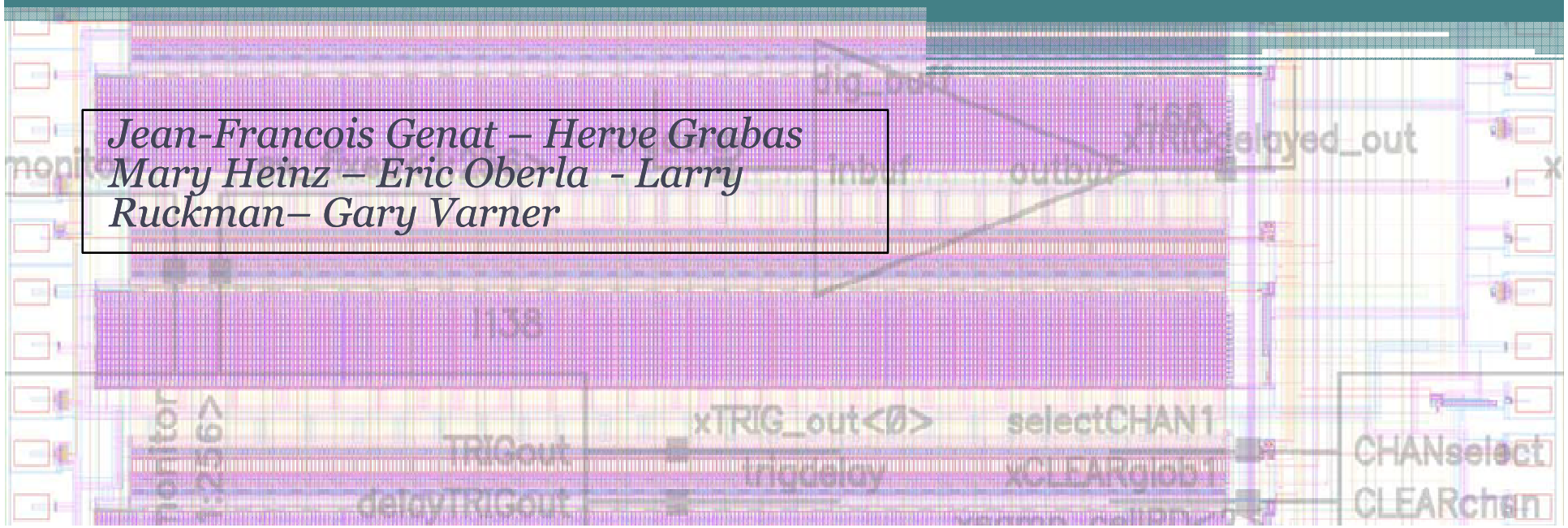
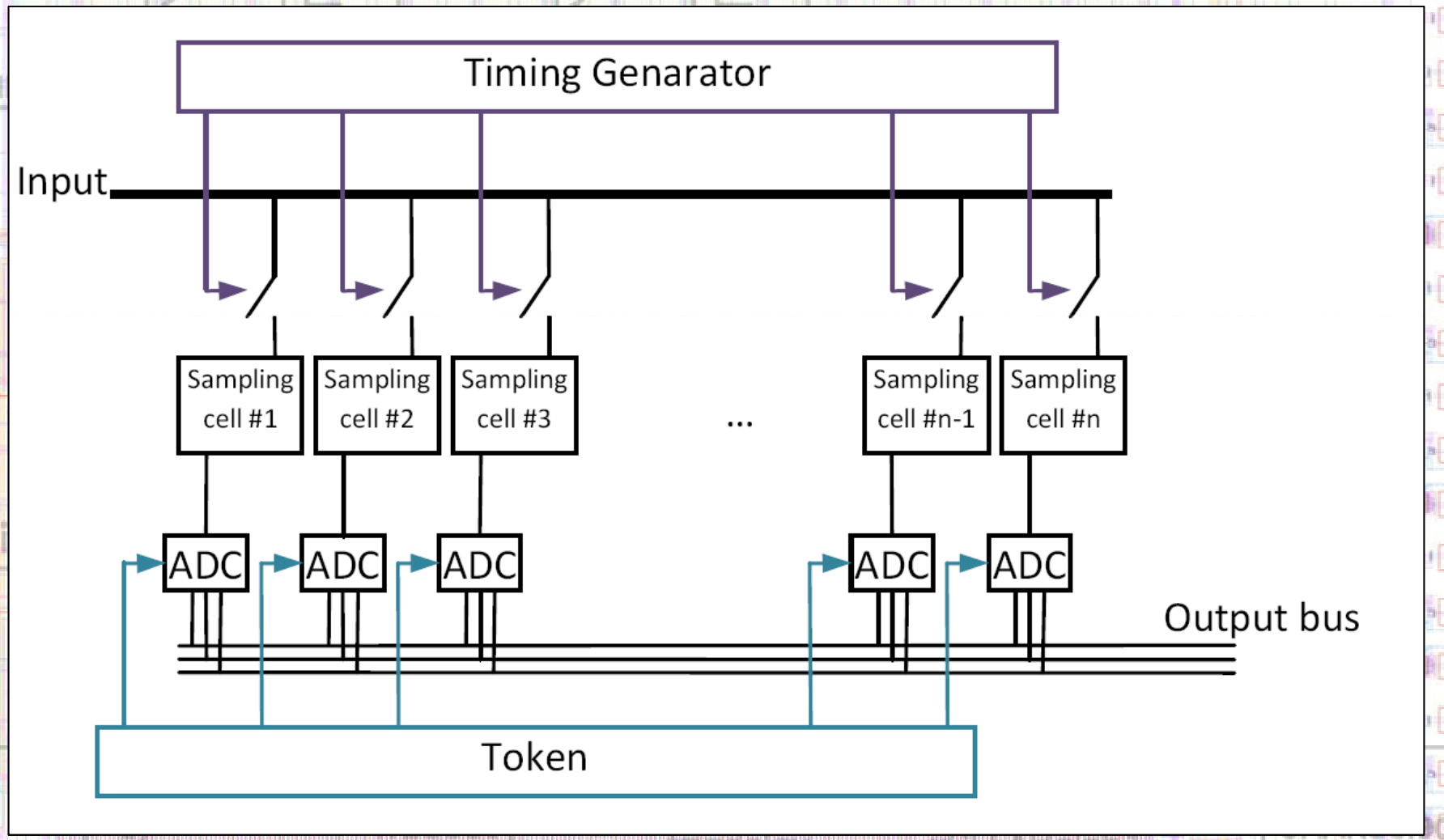
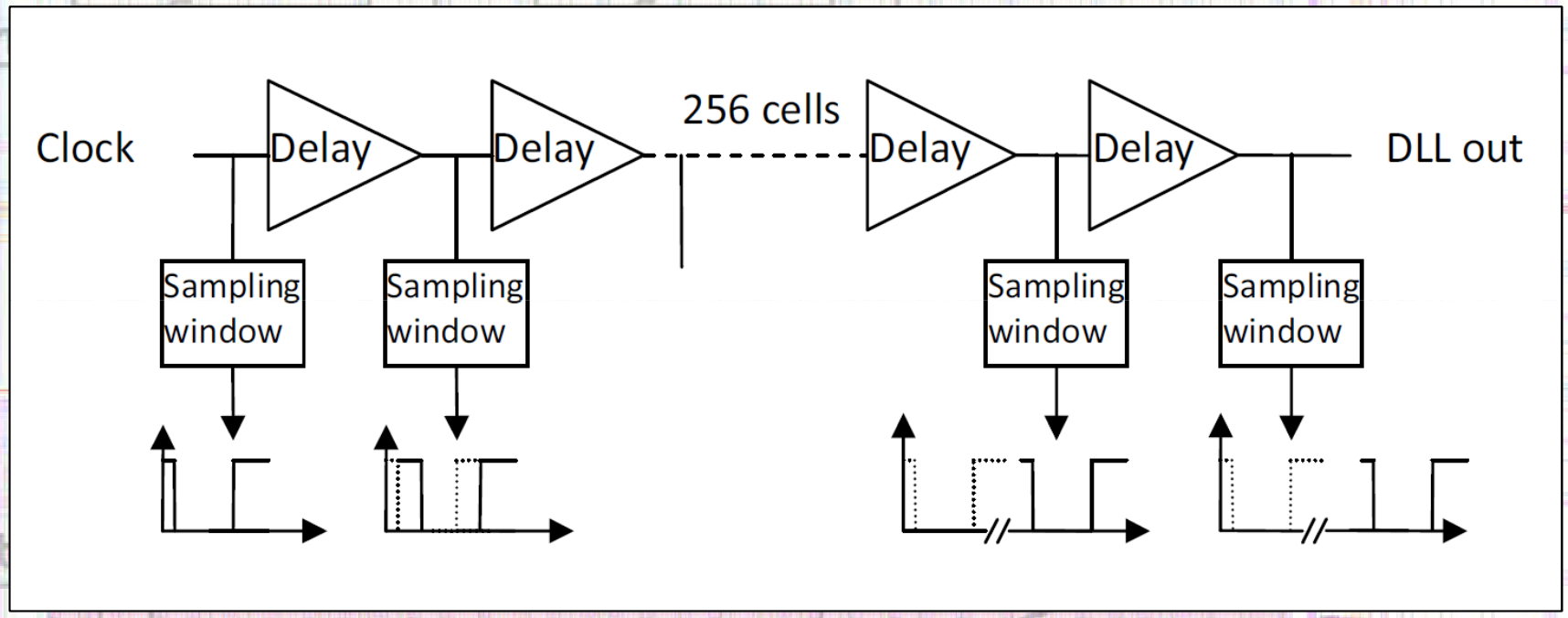


Overall presentation : the principle

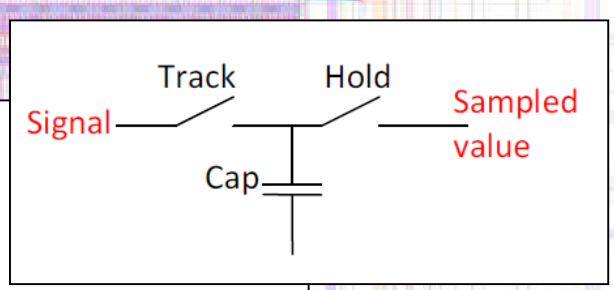


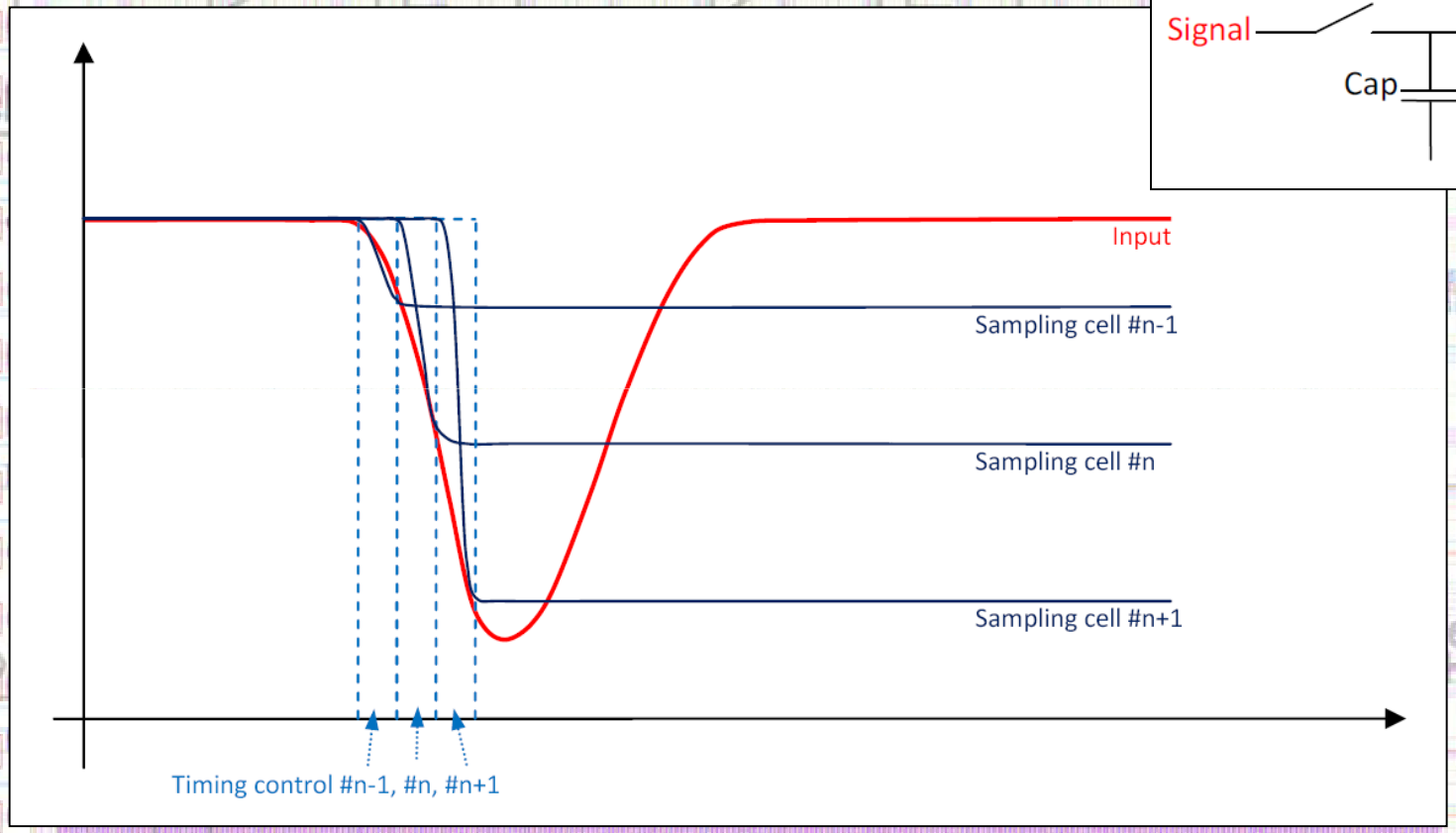
The timing generator



Generates a sampling frequency equals to $\frac{1}{\text{Delay}}$

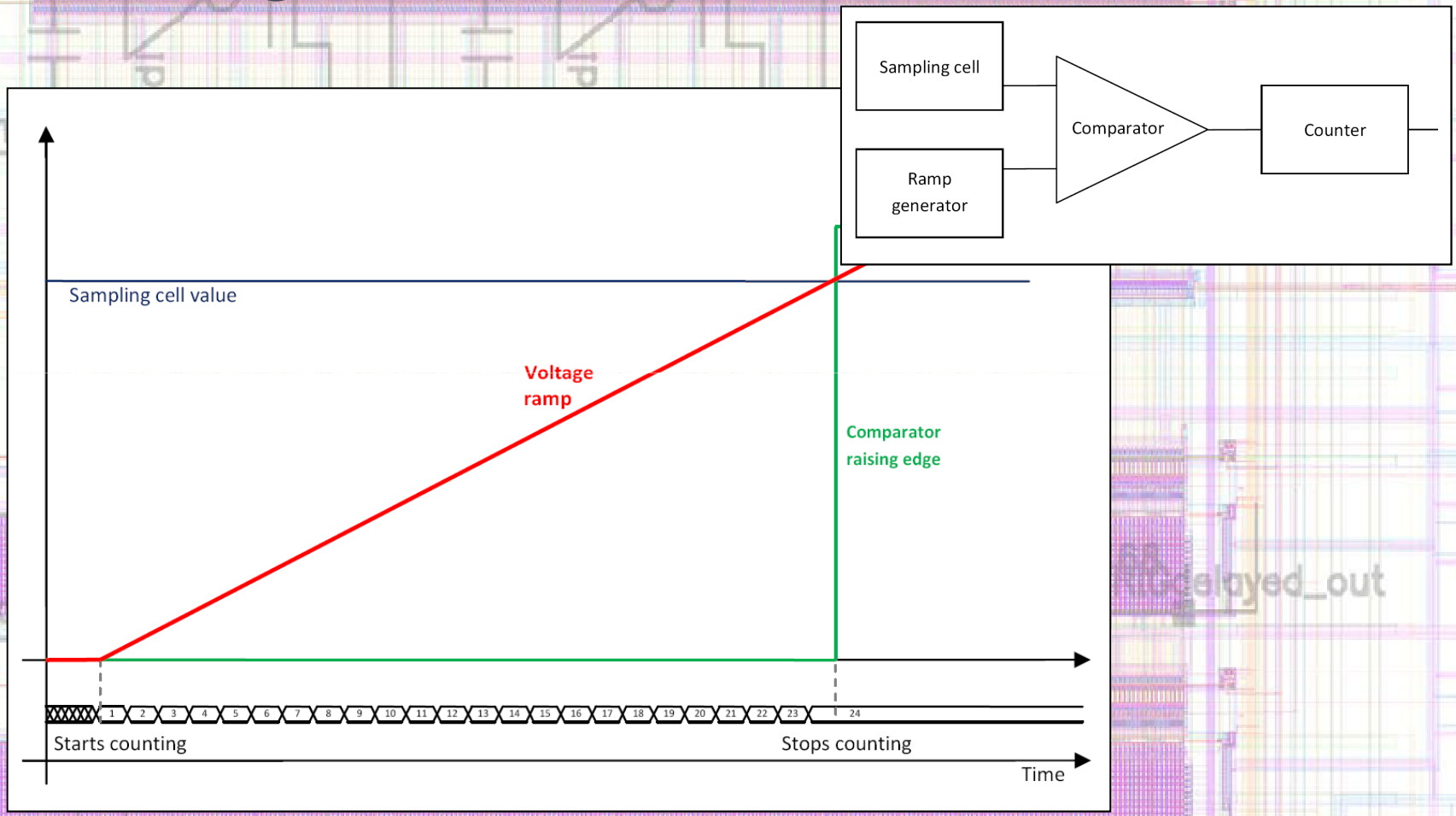
The signal sampling





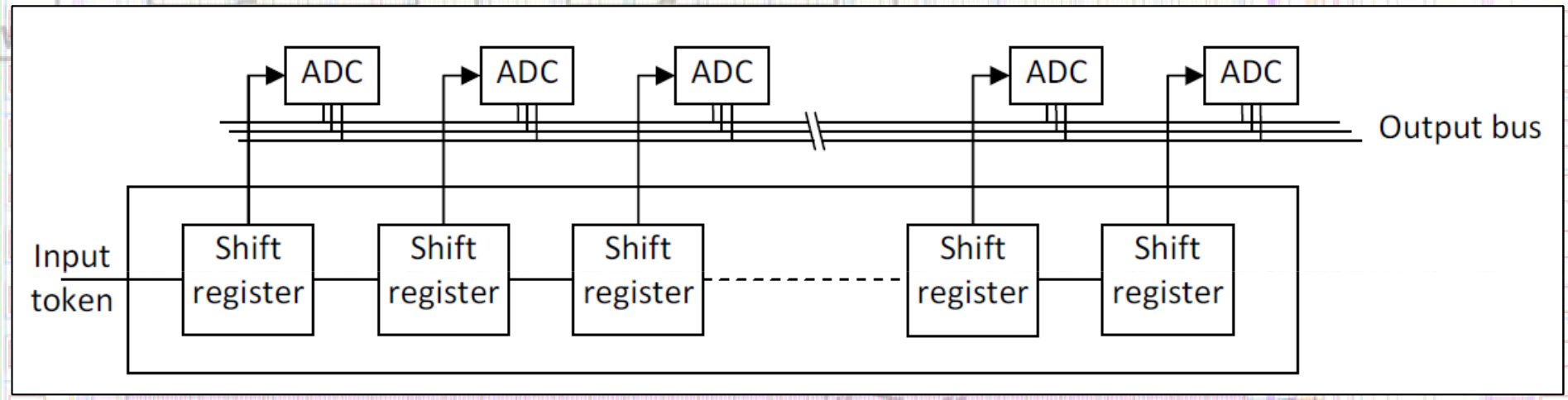
For each sampling window the signal is track and then hold in a sampling cell.

The digitization



Wilkinson ADC: Start ramp and counter, when the comparator fires it stops the counter which holds the digitized value of the sampling cell

Token readout



-Shift register made from 256 D-flip flops passes 'token' signal.

-Each flip flop's Q output controls read switch in corresponding ADC register

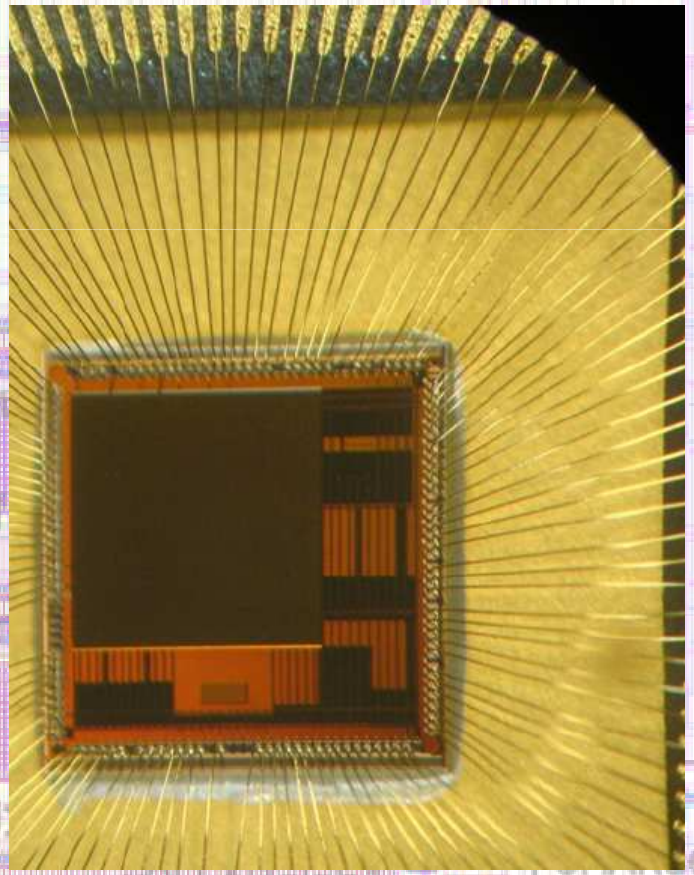
-40 MHz Read clock common to all flip flops

Chip design

Process IBM
0.13micron

Submitted
through Mosis

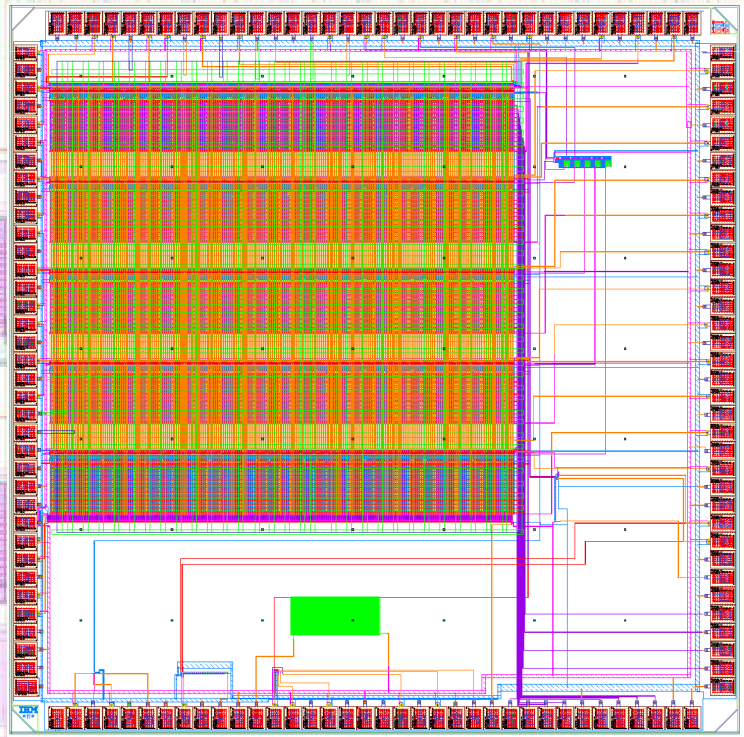
Packaged and flipped
Chips fabricated



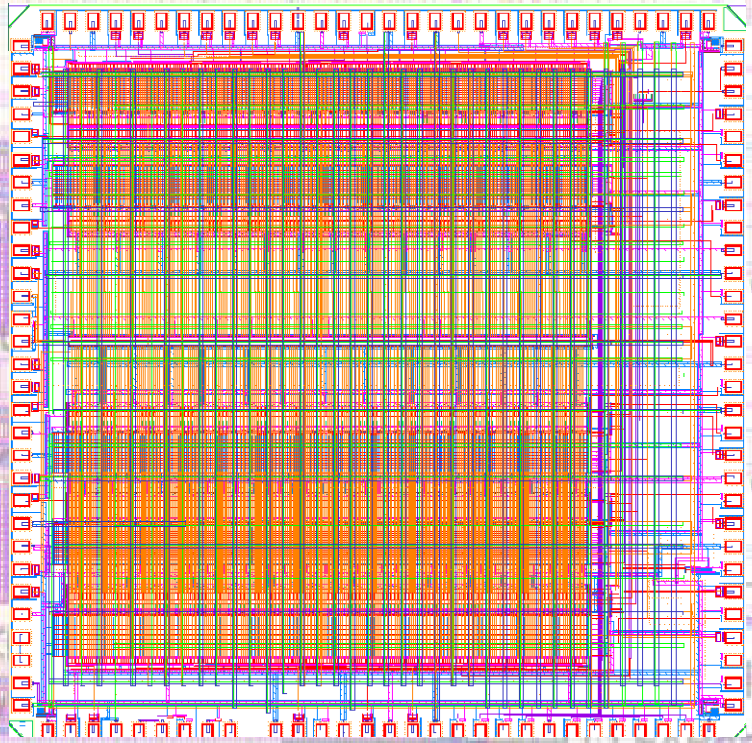
Design Status

- So far two chips have been made:

psTDC_01

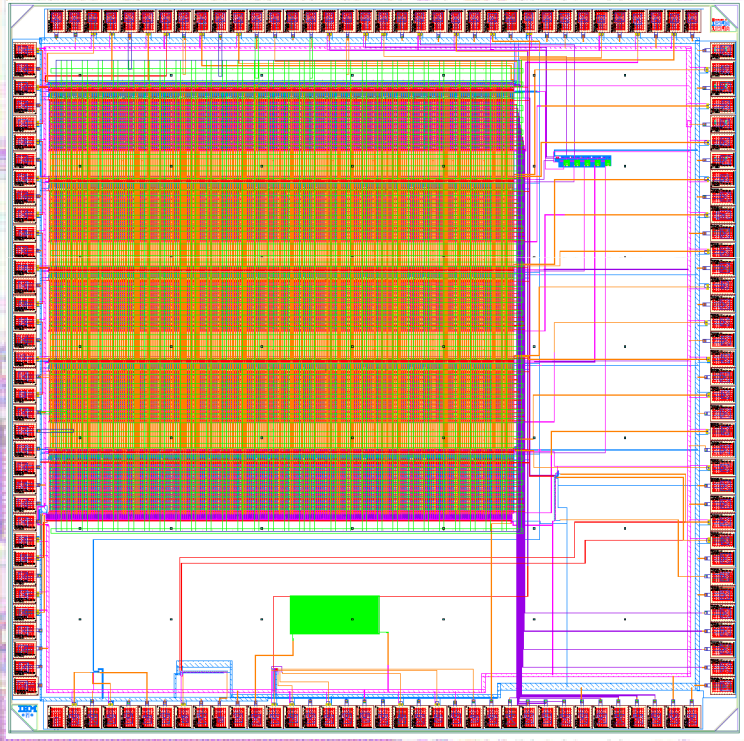


psTDC_02

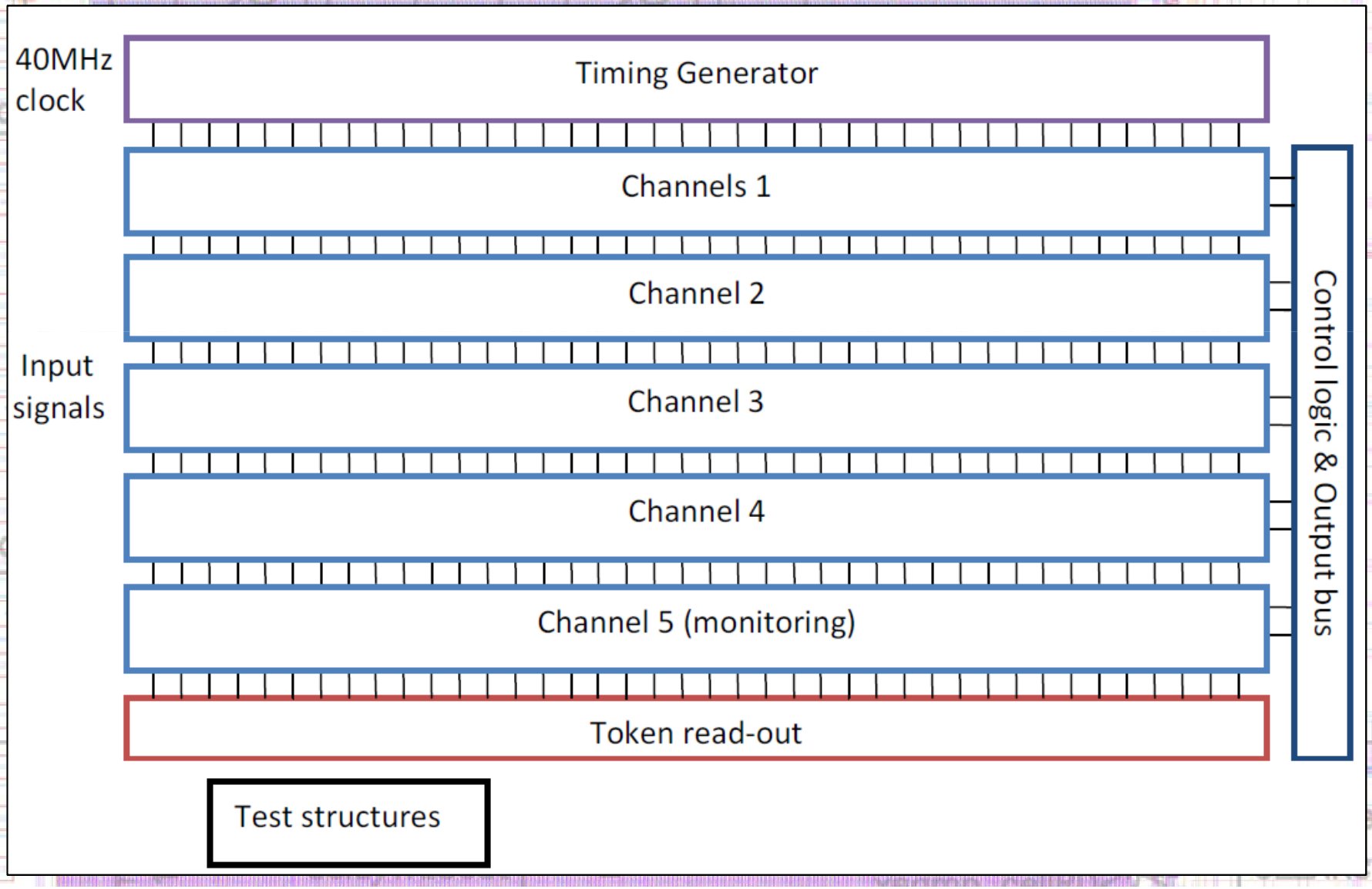


Chip psTDC_01 Specifications

- Targeted 10~15Gs/sec
- ~2GHz analog bandwidth
- 4 Channels
- 256 cells
- 12 bit ADC

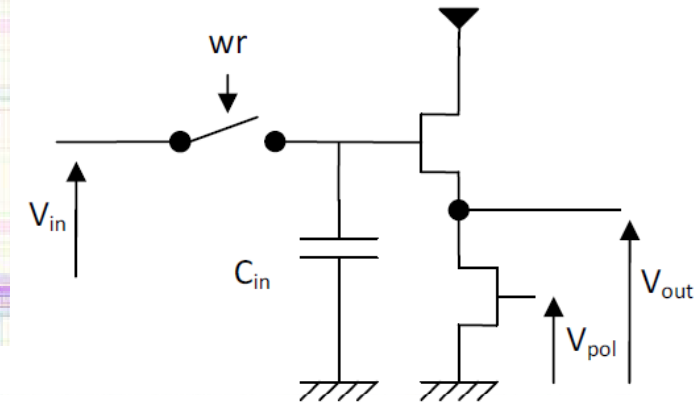


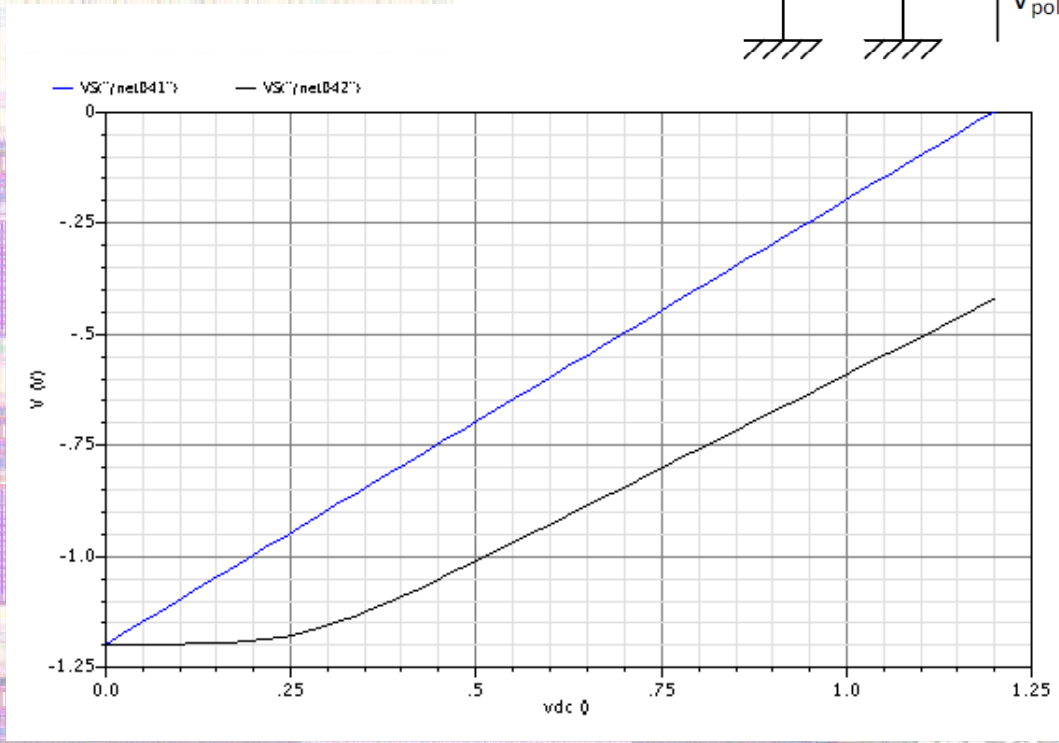
Chip psTDC_01 scheme



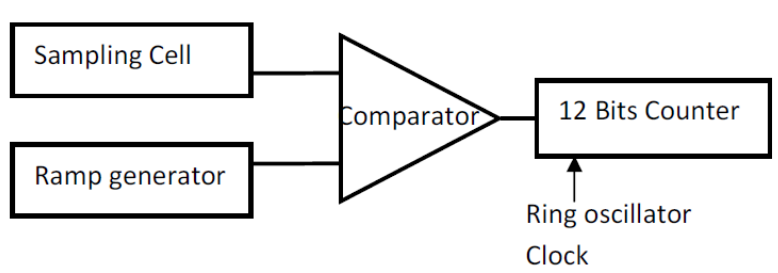
psTDC_01 Sampling cell

- Source follower structure
- Infinite input impedance, small output inpedance
- Advantage: very simple and very fast
- Drawback: drop of tension (Vt) and very important current consumption.

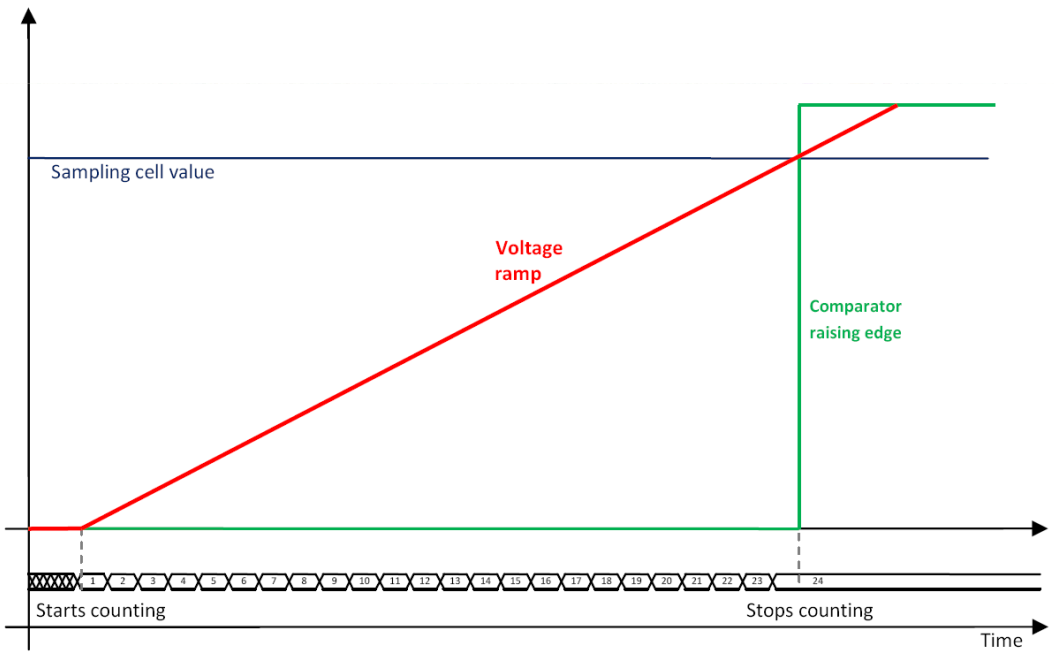




Conversion block



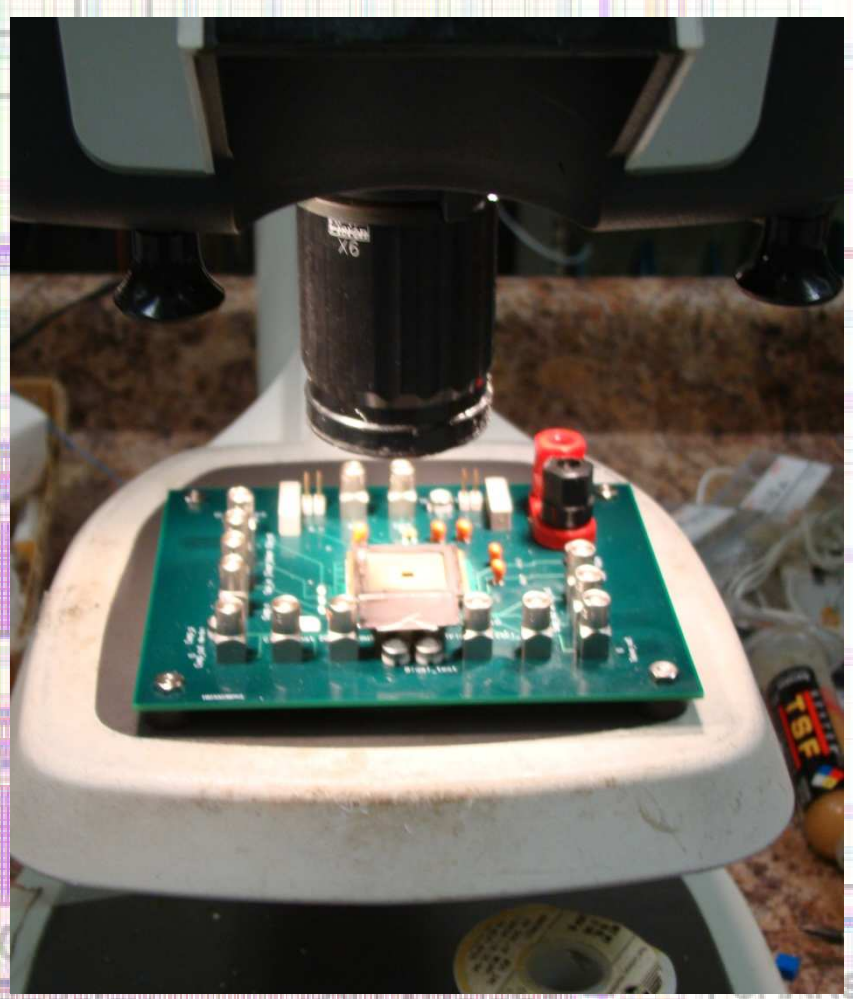
- At the beginning of the digitization the counter starts counting and the ramp is send to every comparator via a buffer.
- When the ramp reaches the value stored in the sampling cell, the comparator fires and stops the counter.
- The value available at the output of the counter is then the digitized value of the value inside the sampling cells.



Testable structures

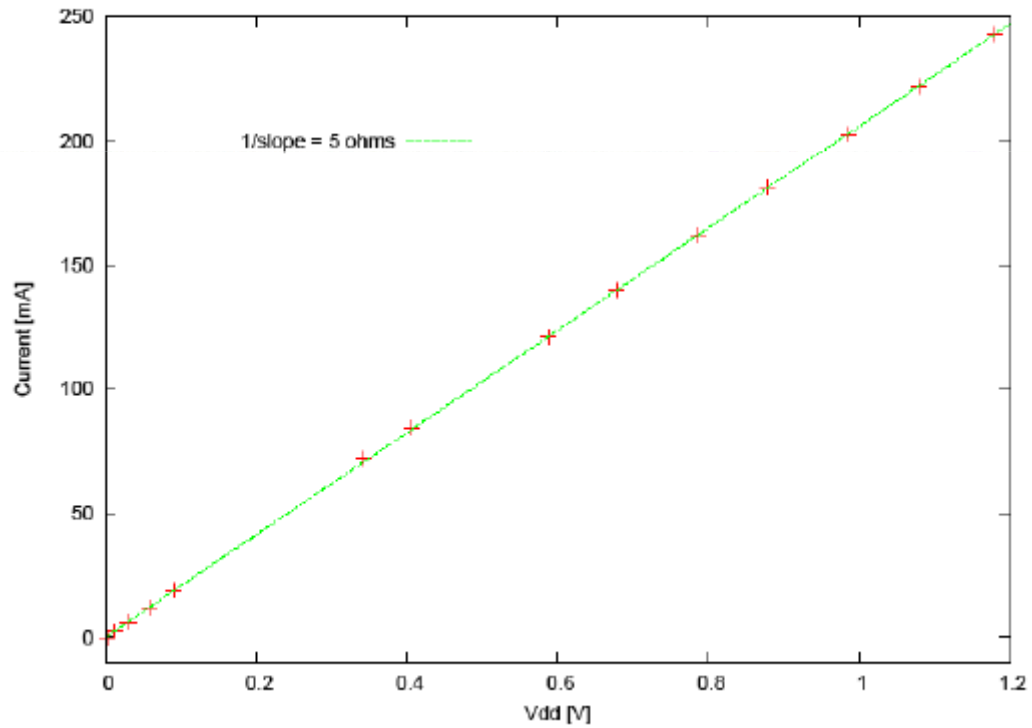
The structures that could be separately tested in the chip were:

- Comparator
- Sampling cell
- Token Readout
- Ring oscillator
- Ramp generator

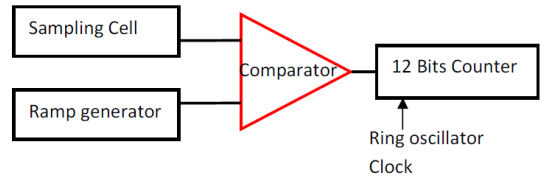


Chip test results : Power

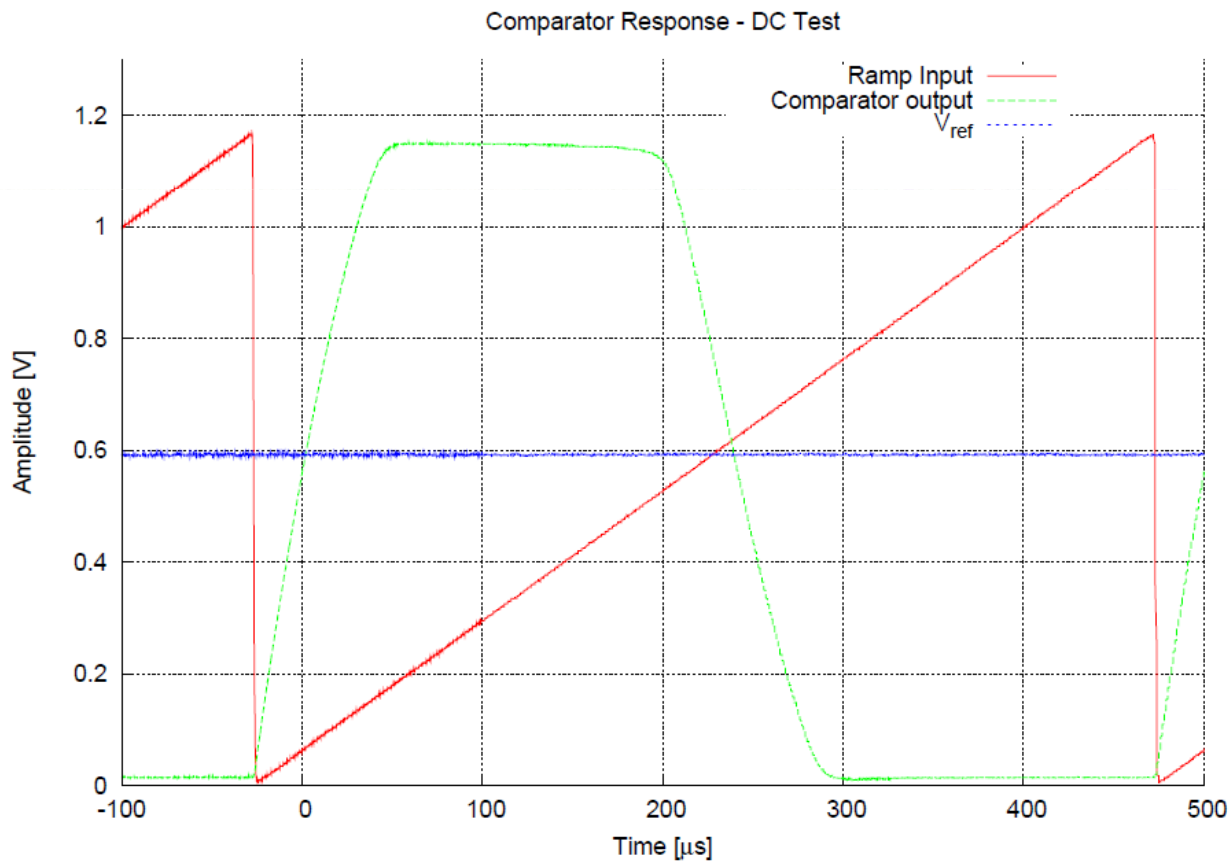
- When ramping Vdd we see a purely ohmic behavior.
- At 1.2V the chip is using 250mA.
- The behavior is due to the ESD protection diodes put on the input pads. The diodes used were only to be use for bandgaps circuits.
- The double diode configuration create a 170 Ohm path from the Input to Vdd andGnd.



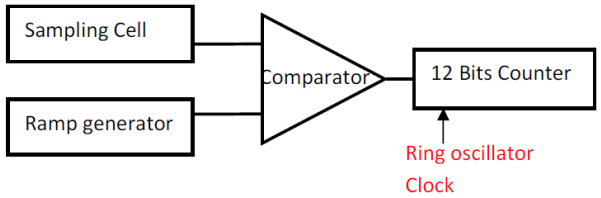
Test structure results: comparator

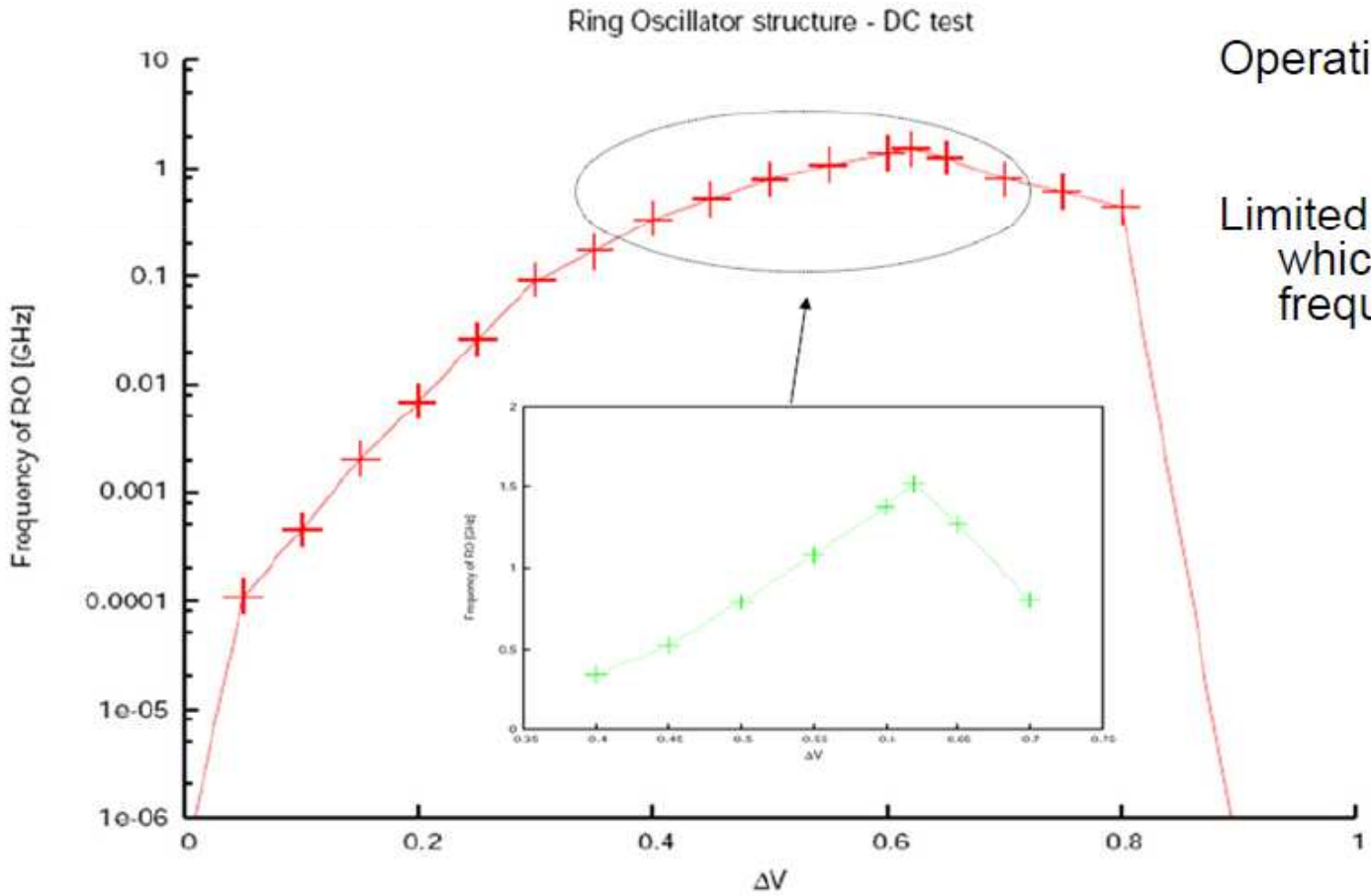


- No buffering at the output of the comparator which makes considerably slower.
- The good news is that it is working over the full dynamic, however its real response time cannot be plotted.
- Inside the converting cells of the chip, the output capacity to drive is much smaller, it should therefore be faster



Test structure: Ring oscillator



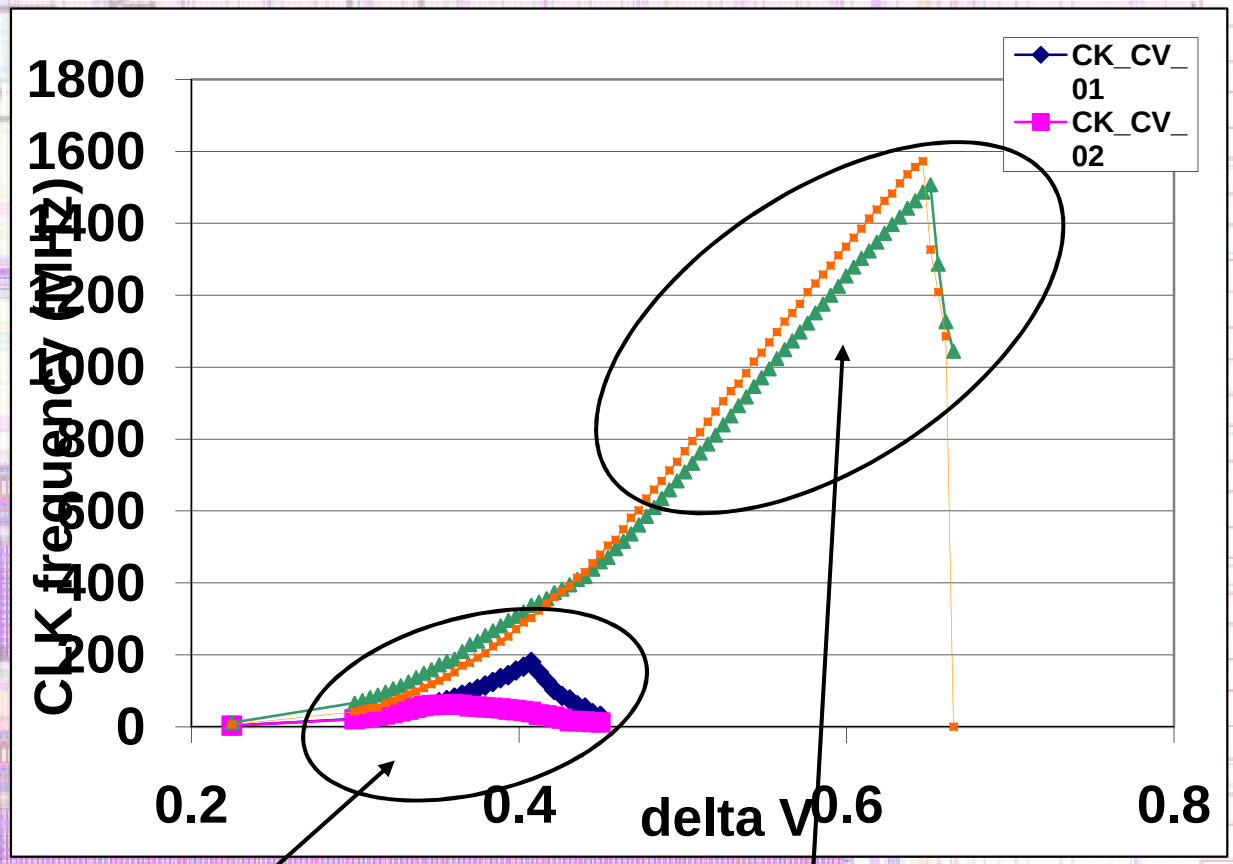


Operational to 1.5 GHz

Limited by 12 bit counter, which fails at this frequency

Ring Oscillator: Inside the chip

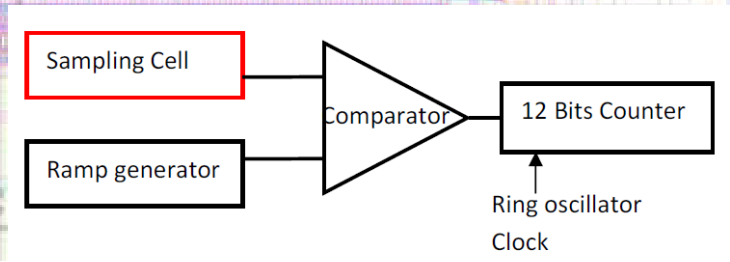
- The ring oscillator inside the chip fails around 200MHz.
- The poor behavior is due to the important capacitive load of the wires inside the chip.
- A better buffering (clock tree) need to be implemented, to reach the full speed.



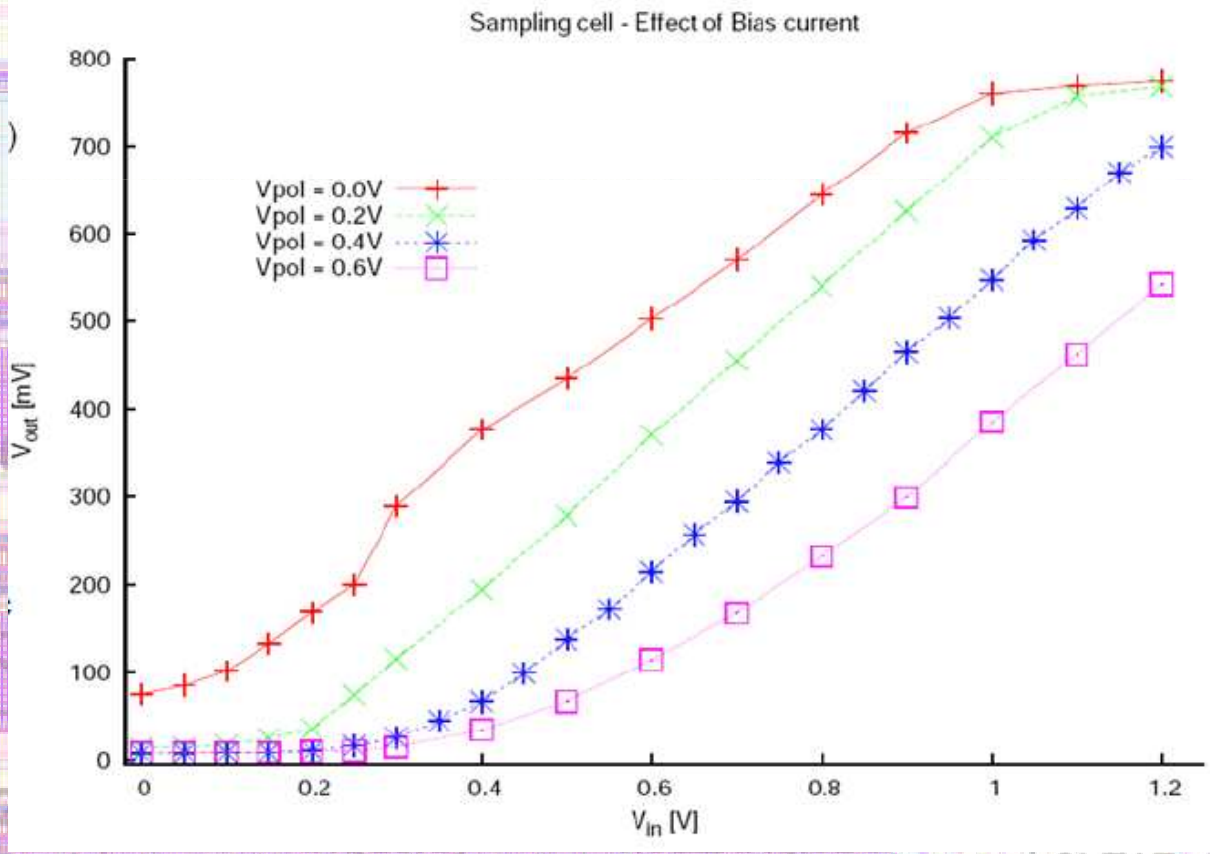
Inside the chip

Test structures

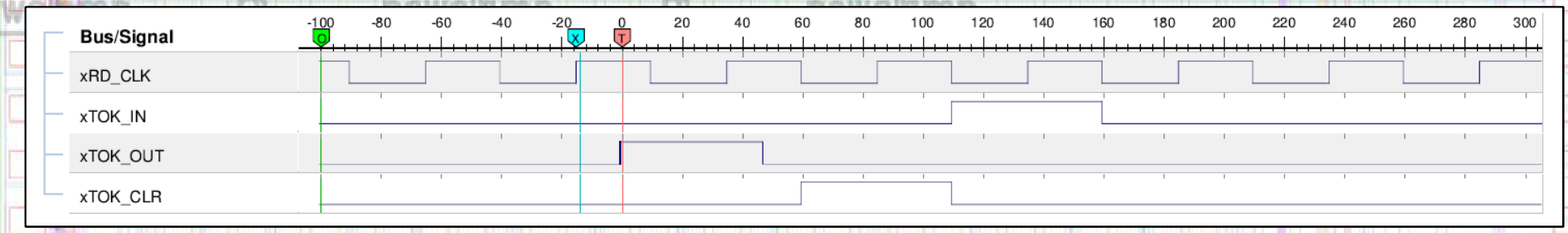
The sampling cell



- The sampling cell works correctly for its design Vpol of 0.4V.
- For lower voltages the dynamic is subsequently reduced.
- For higher voltages we see a saturation probably due to the small pad resistance.

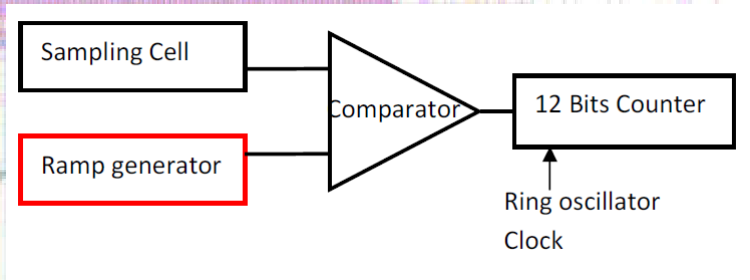


The Token Readout



- The Token is working properly but here again we have loading issues.
- For full speed readout a proper clock and signal buffering has to be done.

The ramp generator



- Never worked.
- Even when applying the ramp externally, it will not couple inside the chip.
- The externally applied ramp is probably not seen on chip to the failure of the analog buffer sending the ramp to all 5 channels.
- The failure of the buffer is probably explained by the fact that its internal resistance is not working.
- A 50 Ohms resistance was indeed placed at the input of two channels in the chip. These 50Ohms were never observed (open).

Sampling speed

- The 40MHz clock was send at the input of the chip and we looked at the time difference at the output.
- The sampling frequency is then given by:

$$\text{Sampling speed} = \frac{\text{Observed Delay}}{256}$$

- We observed a delay of 50ns which gives us a sampling frequency around 5Gs/s.
- This sampling frequency is much smaller than the one expected from post-layout simulation.
- The slow sampling speed observed could be due to capacitive loading of the long line present on chip.

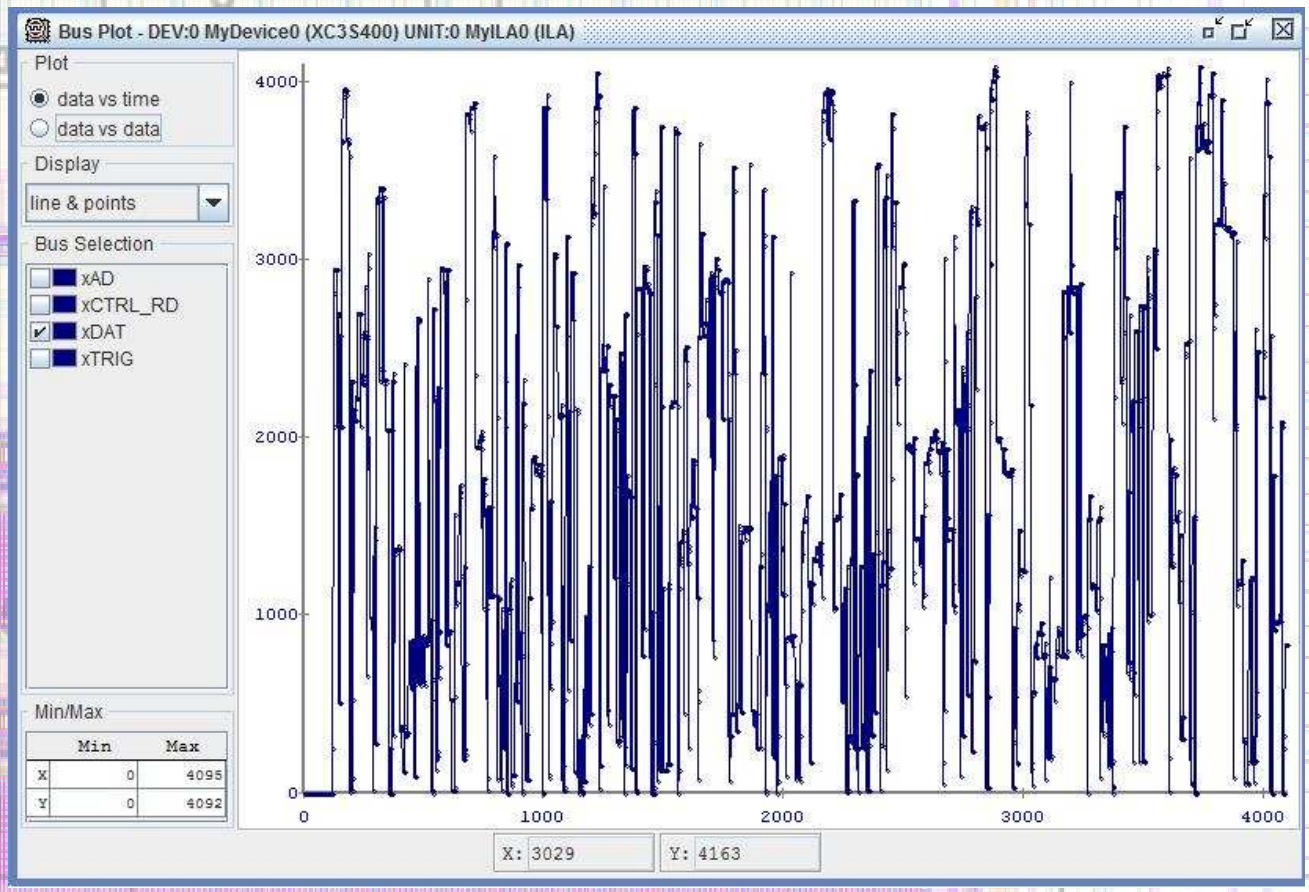
Digitization not working

- A DC voltage of 0 V is set at the input of all the channel.
  The ramp voltage is set at 1.2V.

→ We should see 0 (12bit) at the
output.

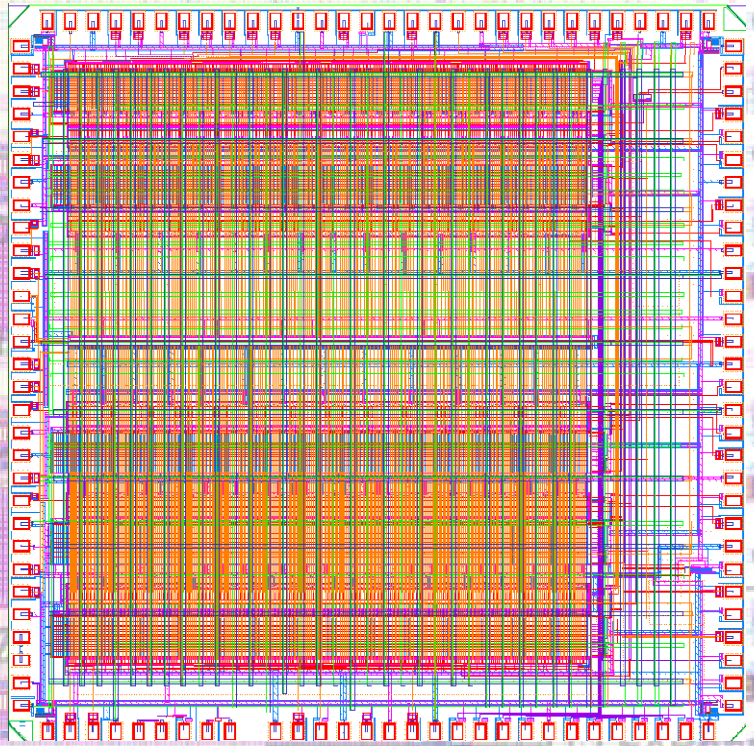
- Instead all the counters are free running (we can see it reading the data two times).

- Ramp generator is not working probably because of its output buffer .

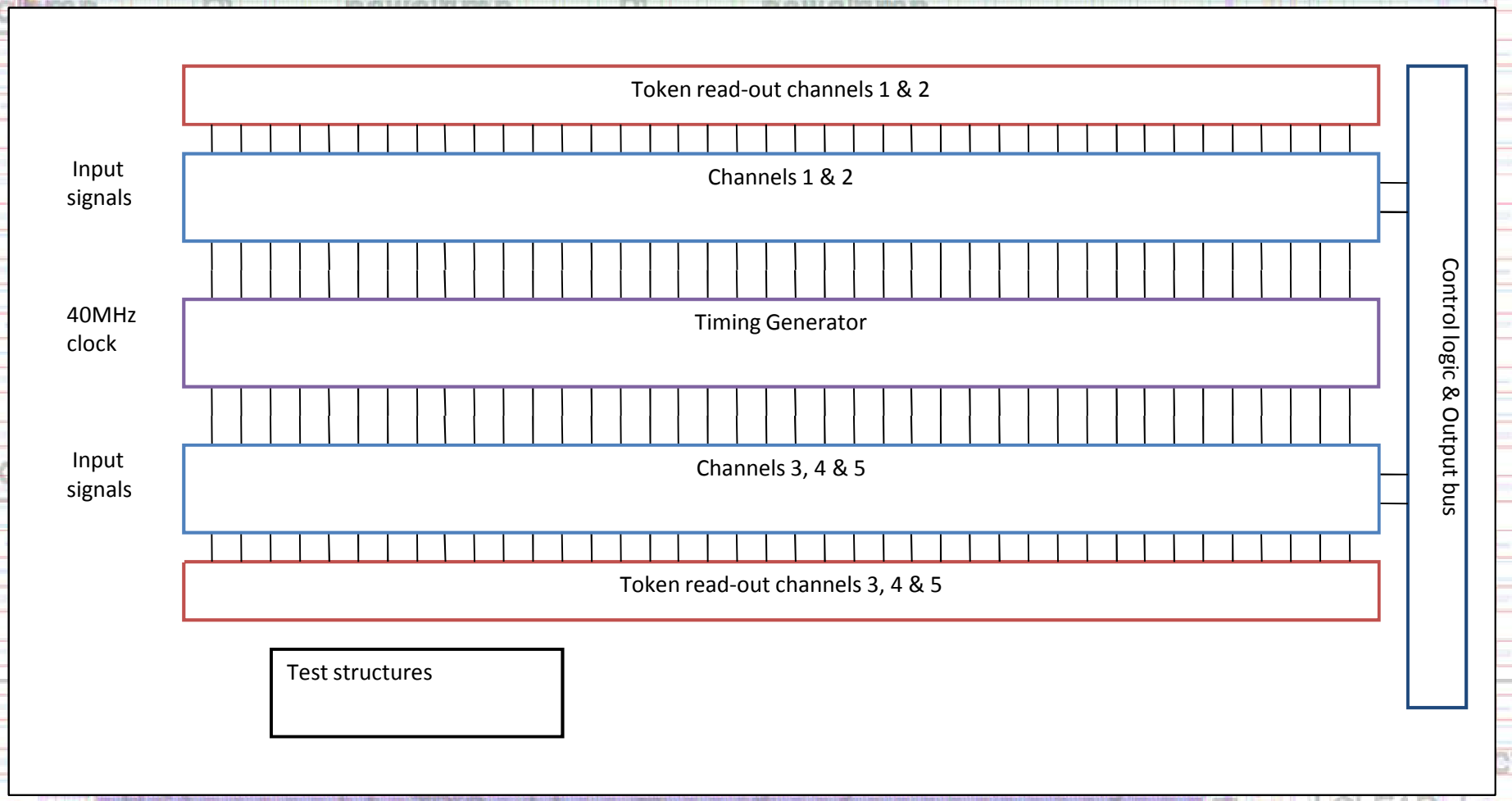


psTDC_V2 Specifications

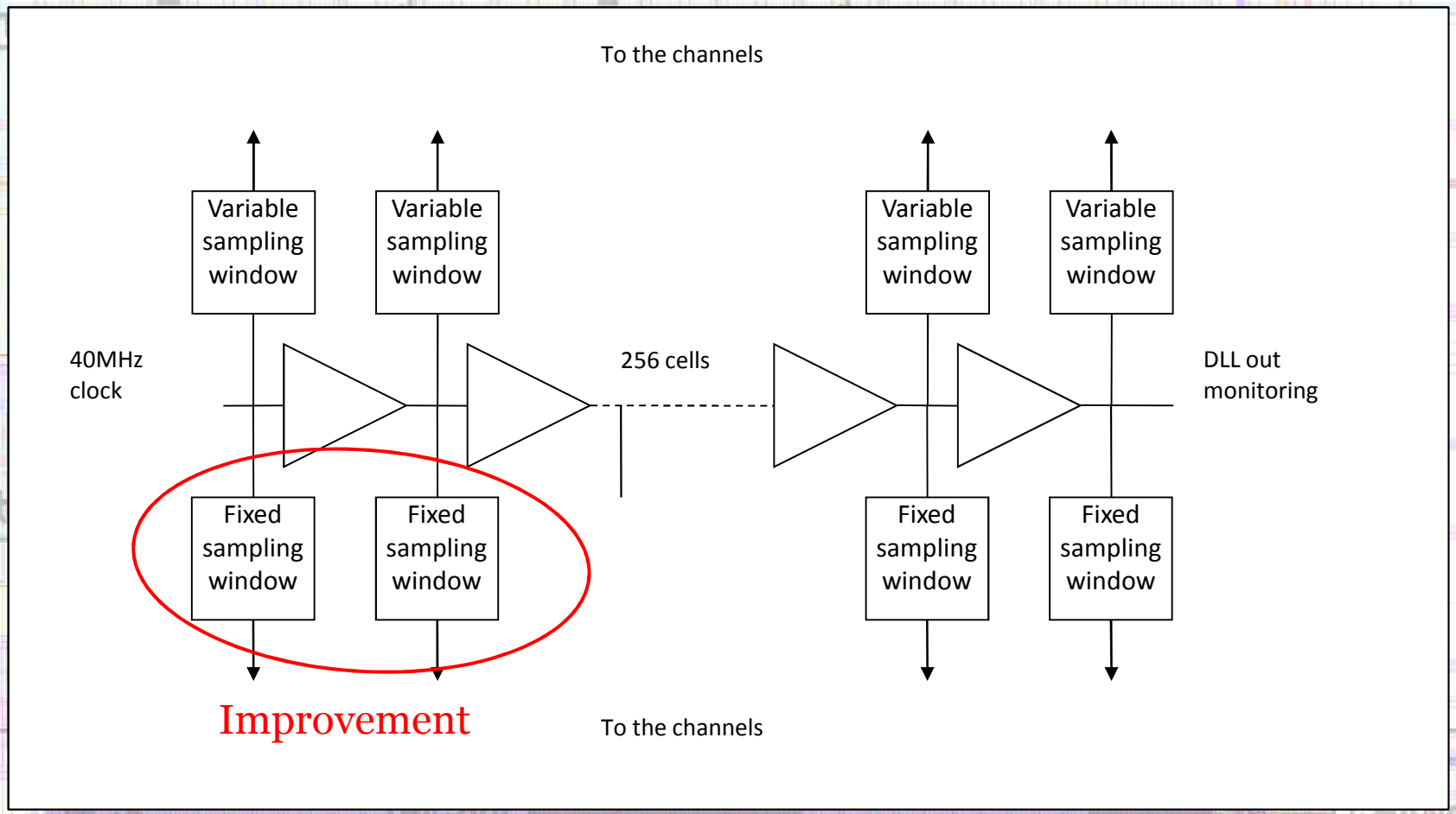
- 15 Gs/sec
- 2 GHz analog input bandwidth
- 4 channels
- 256 cells
- 12 bits
- Improve previous version



Overall presentation : the chip architecture (dual readout)

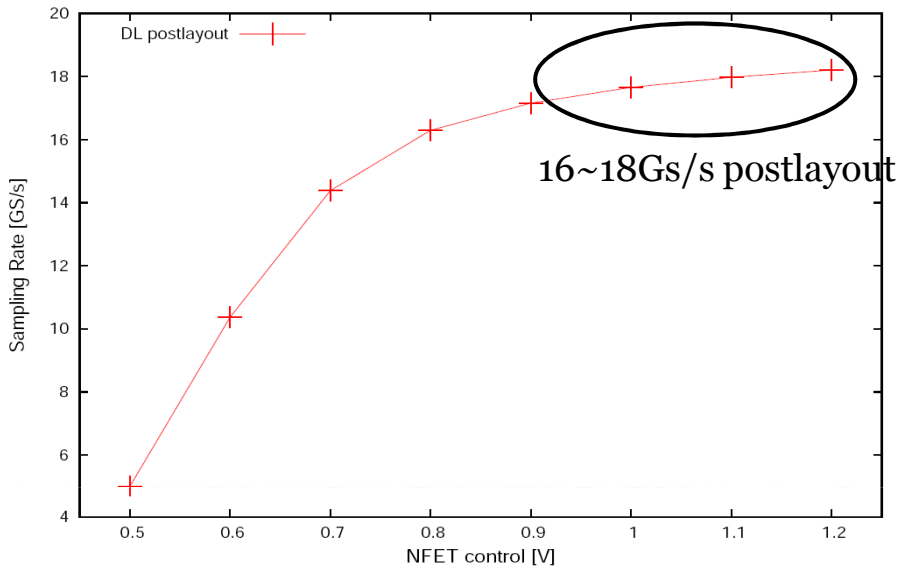


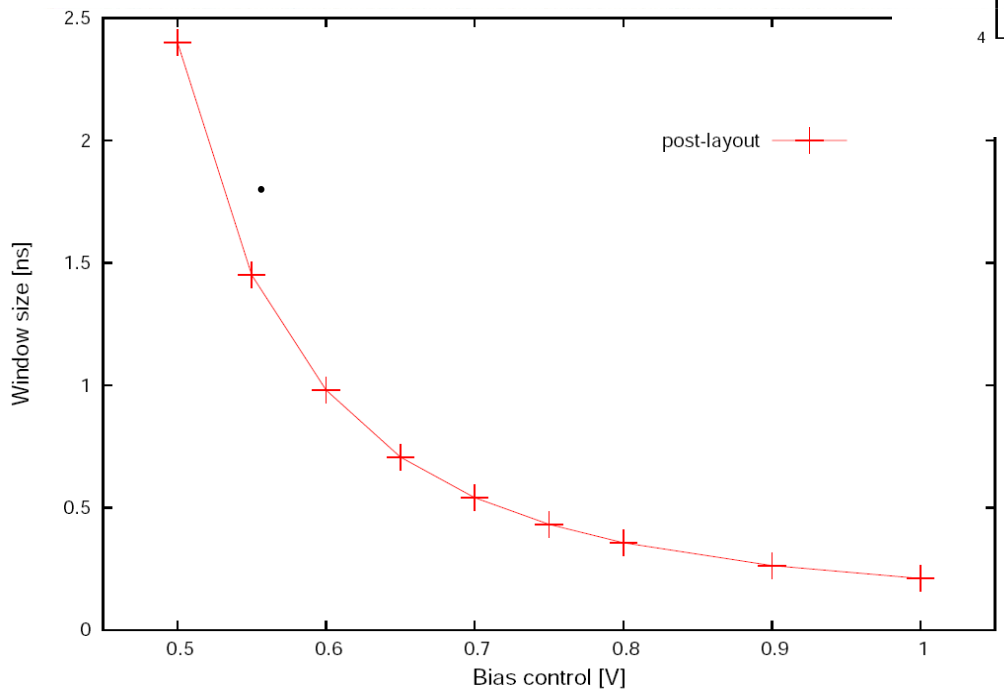
The timing generator: principle



The timing generator

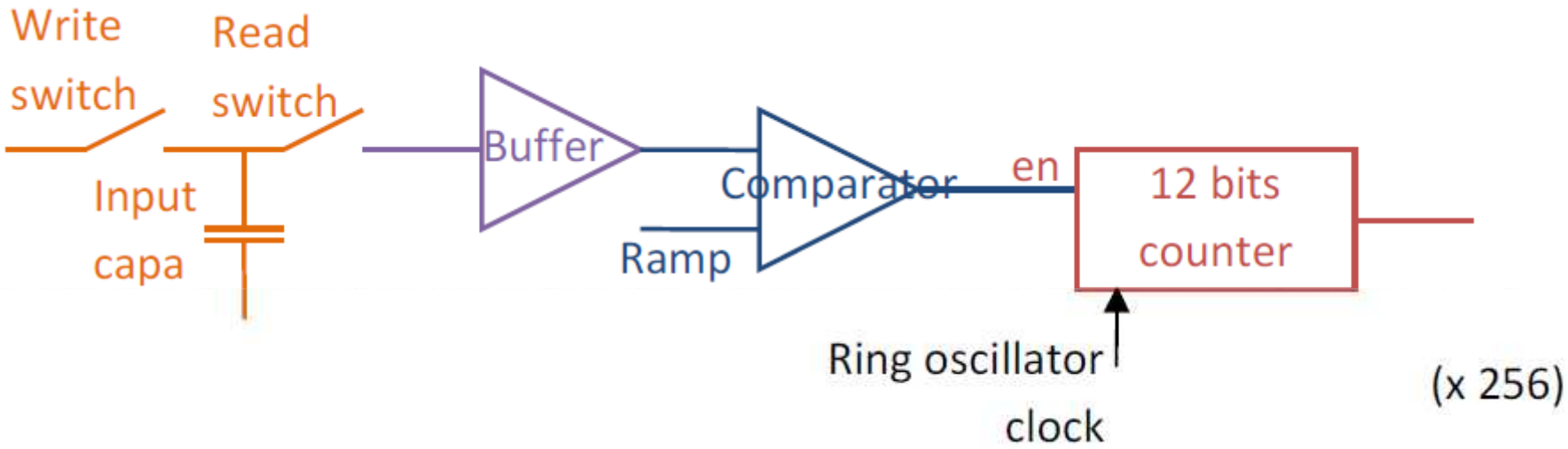
- Same architecture conserved.
- Output of the DLL better buffered and shielded





- Adjustable delay with two voltages. Allow in principle an external phaselock system.
- Fixed and variable window generation (improvement).
- The time range of variable window has been improved in order to resist to the capacitive loads of the lines to the channels.

The channels: principle

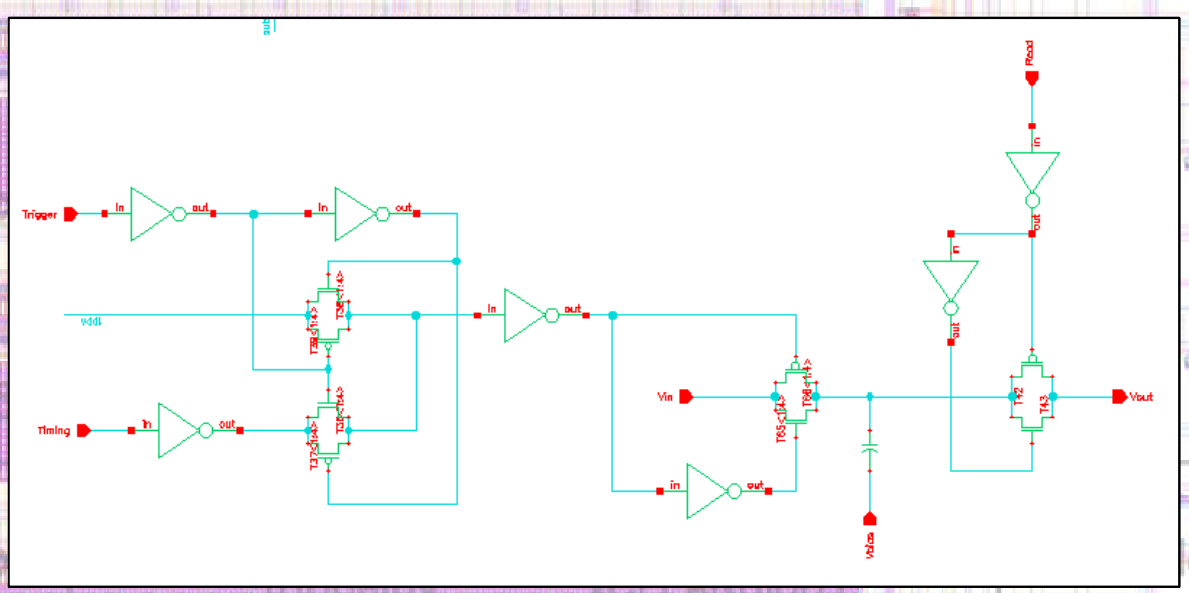


Made of:

- Sampling cell
- Buffer
- Comparator
- 12bits counter

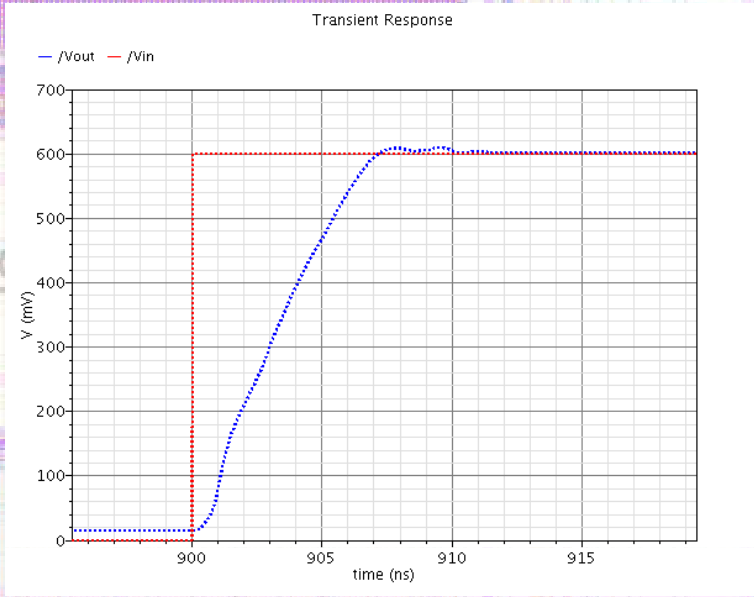
The Sampling cell

- More control logic
- Bigger input capacitance
- Same bandwidth



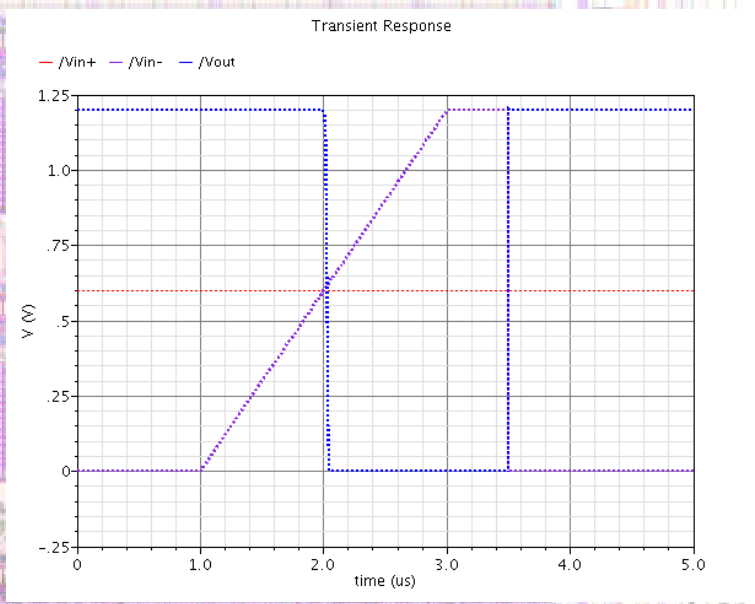
The Buffer

- Better input dynamic
- A bit slower
- Use less current

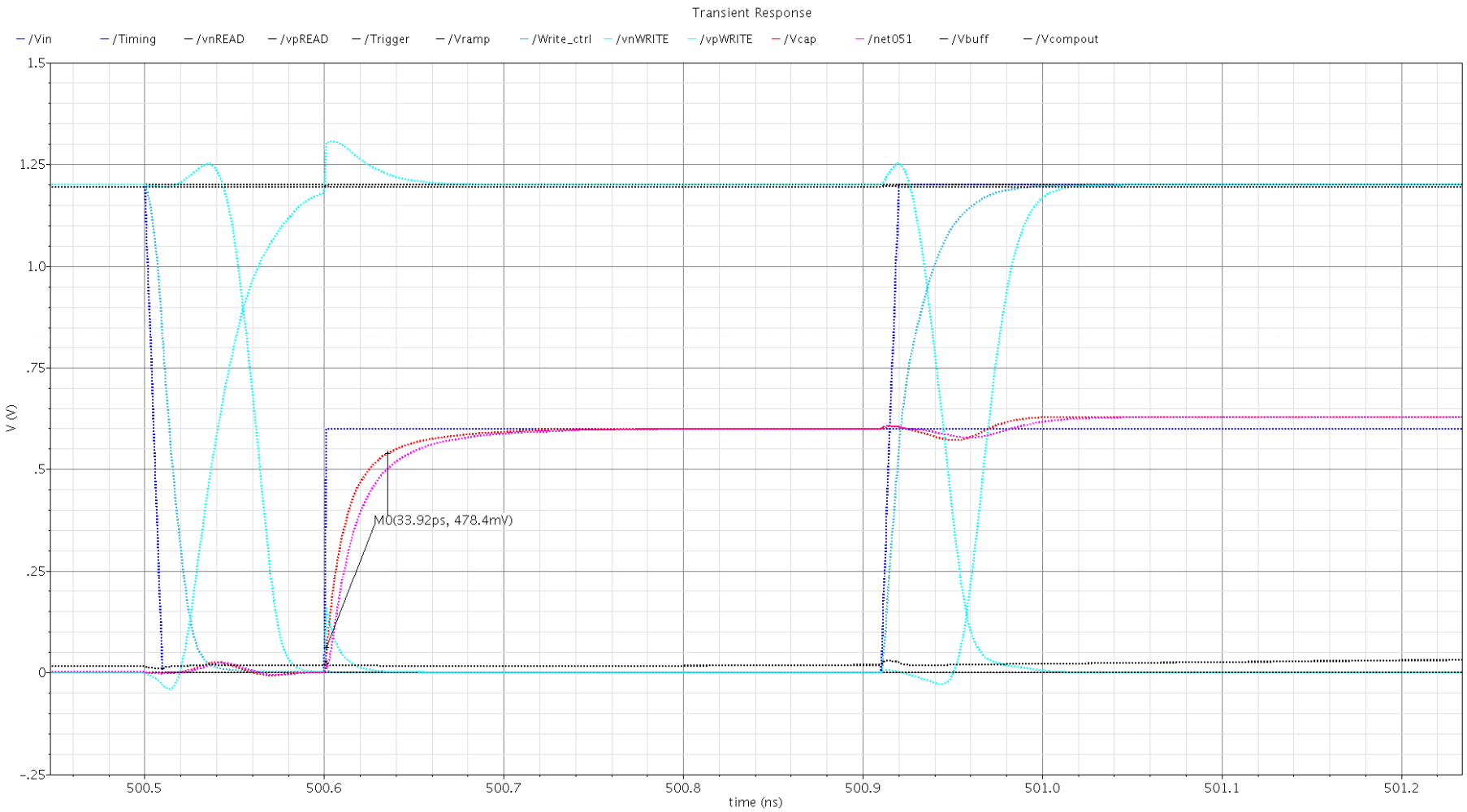


The Comparator

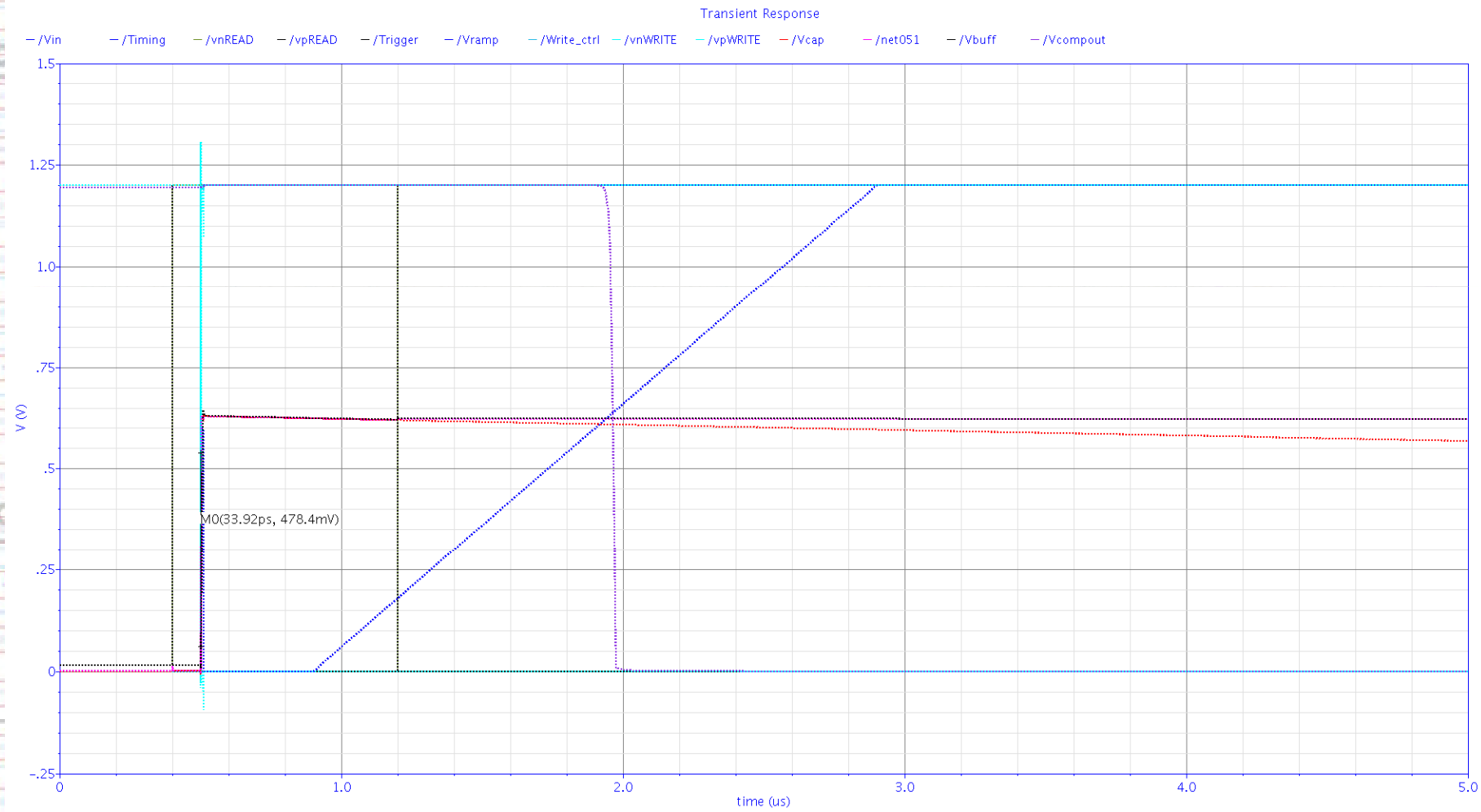
- Same spec
- Use less current



Digitization 1

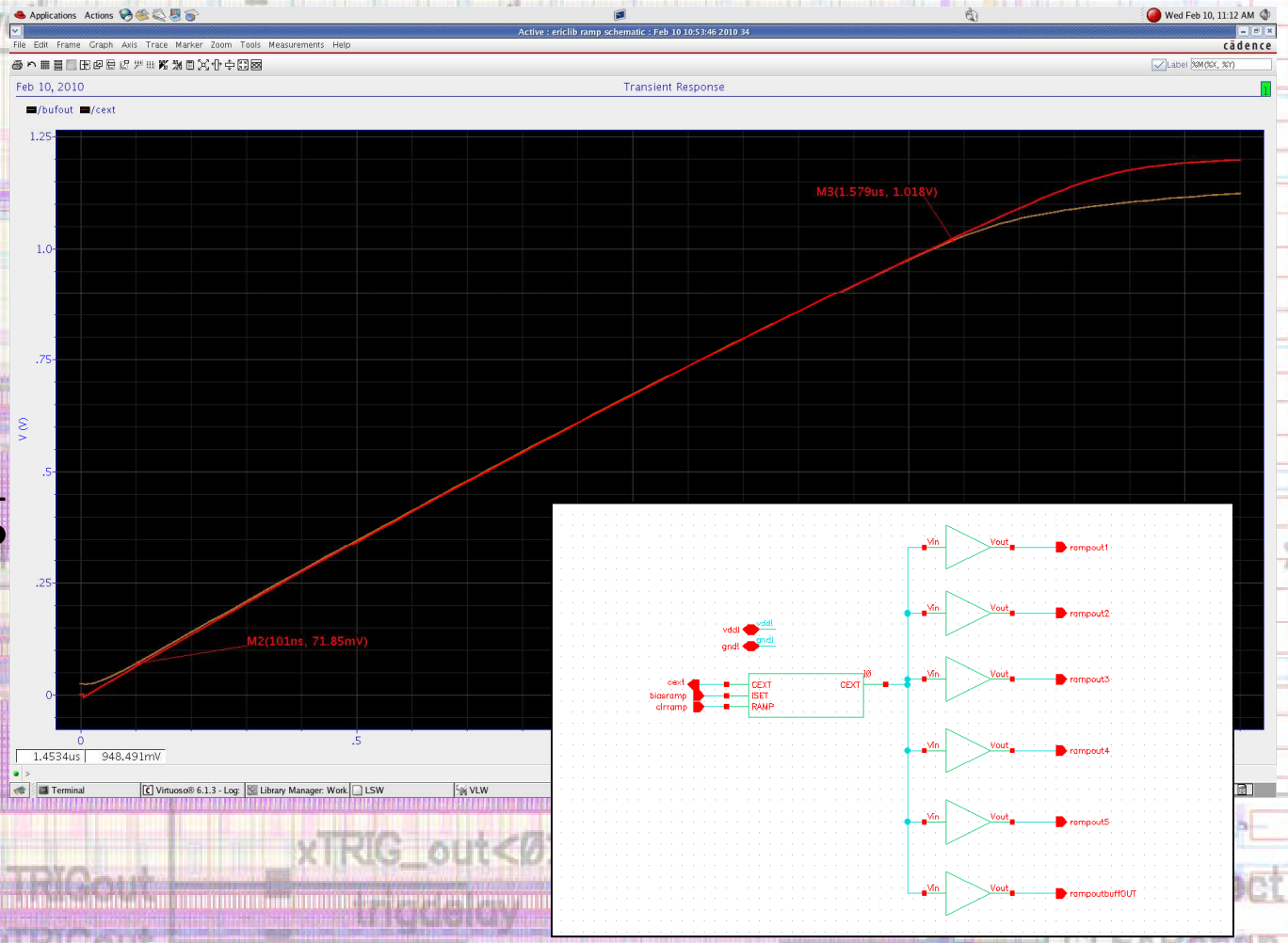


Digitization 2



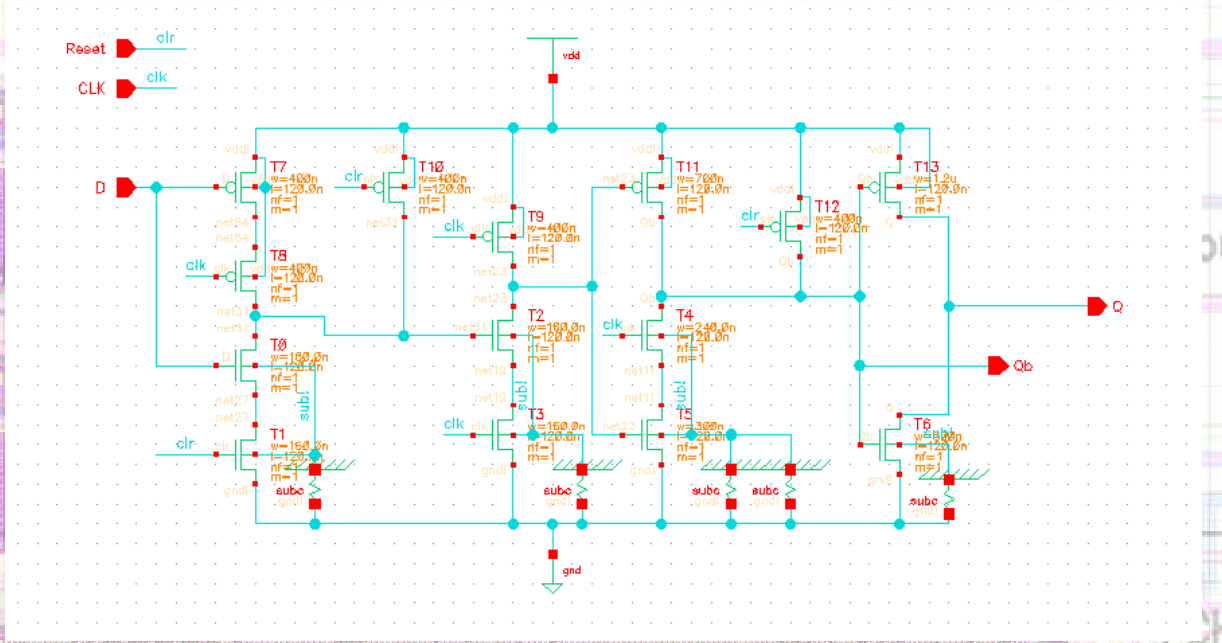
The ramp generator

- Improved range and linearity
- Hopefully fixed the in-chip coupling
- Buffer per channel



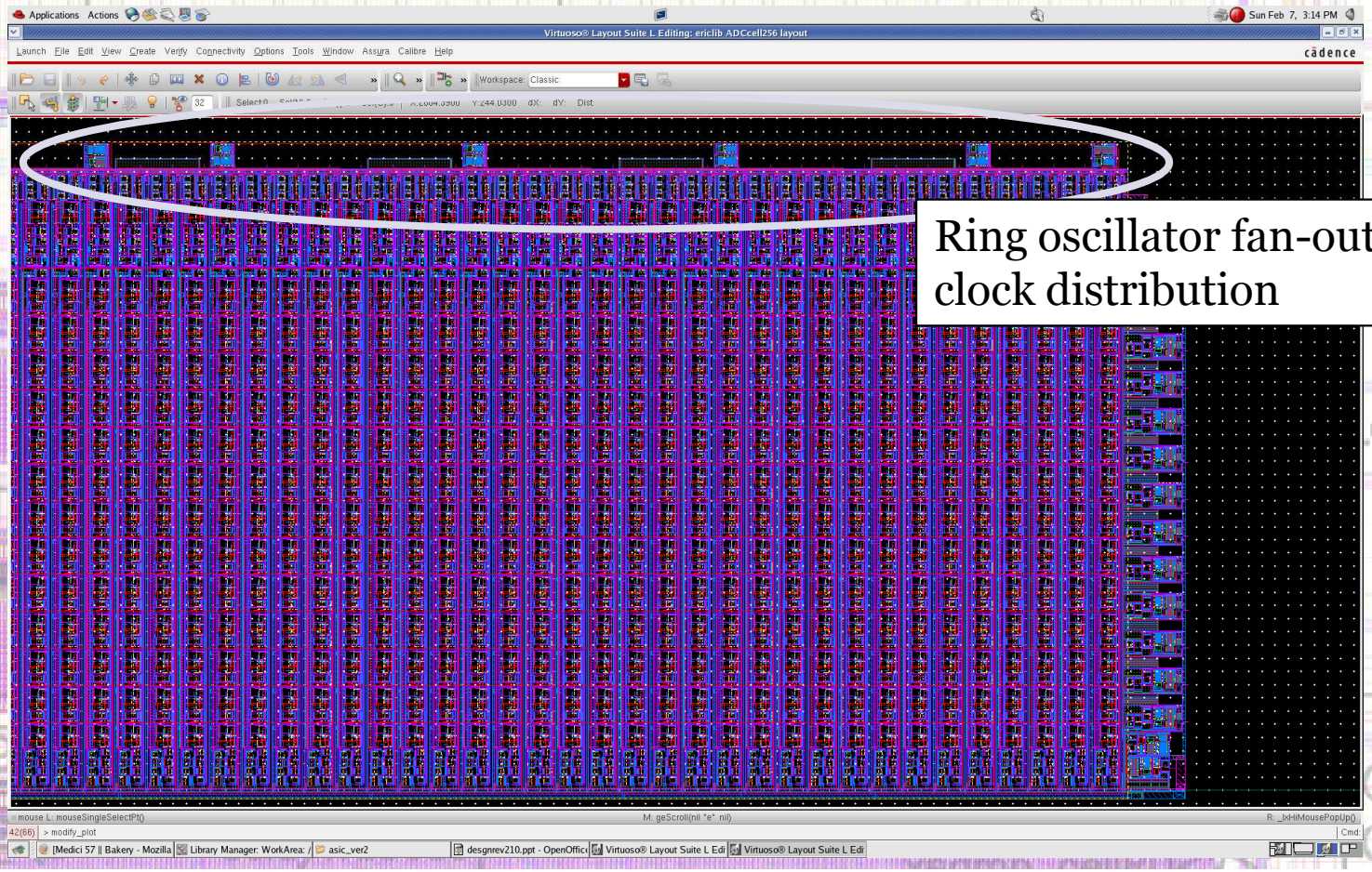
The digital circuitry

- General improvement thanks to a new and faster D-Flipflop.

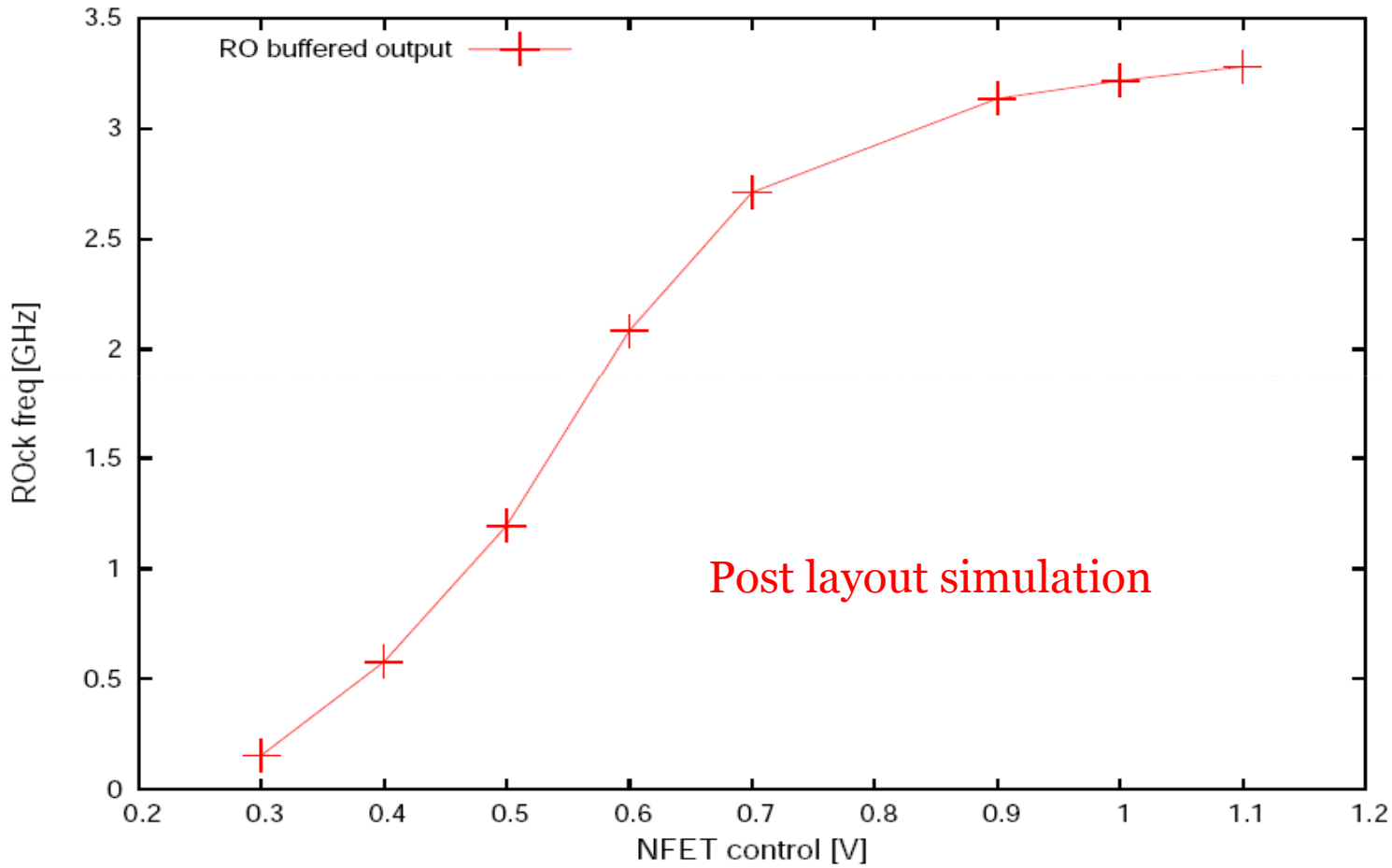


The ring oscillator

- One ring oscillator per channel.
- Monitored by a 12bit counter.
- Frequency adjust by two voltages
- Added a fan-out: better clock distribution



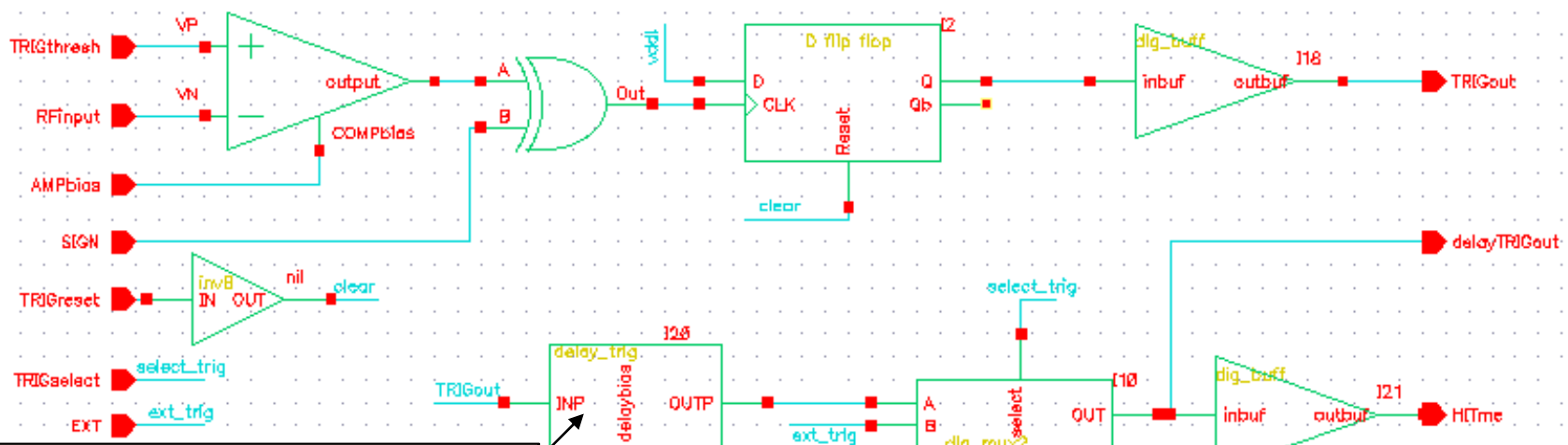
Ring oscillator: simulation results



- buffer used to distribute ROck can drive ~100fF @ 2-3GHz from post-layout simulations
-layout was done such that each buffer drives < 50 fF

The Trigger

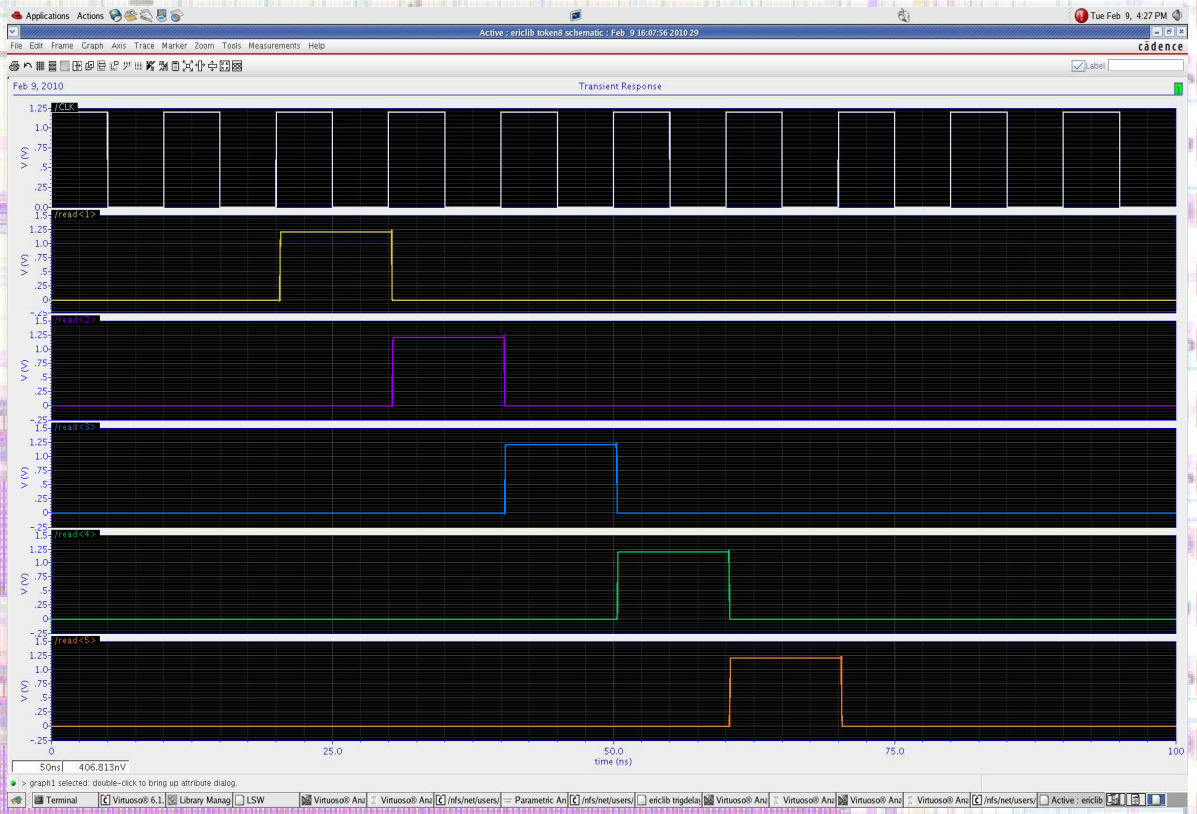
- Positive and negative pulse detection
- Delay before triggering
- Threshold level adjustable
- Bypass possibility



variable delay (~7-20 ns nominal) between firing of trigger and hold signal to sampling cells

The Readout

- Same token principle
- Faster
- Less dead time
- Better buffering
- Possible to select channels and block of 64 cells
- Debugging possible via analog input and output



Debugging

- Fifth channel for sampling window observation
- Test structure: comparator and buffer
- Option for channel analog monitoring
- Resistance test structure
- More monitoring: ring oscillator, DLLout, ramp
- More bypassing

Summary of digital improvements on 4-channel, 0.13um sampling chip

- Improved ADC clock fanout
- Digitization @2GHz takes 2 us for 12 bit
- Serial readout of one quarter (64 cells) of sampling depth. Avoid reading out large amount of pedestal. Readout time for one block of one channel = 1.6us
- Internal trigger with external option. Set trigger threshold for each chan. with analog voltage.
- Digital input/output pads equipped with digital drivers. Especially important for getting signal off chip. ESD protection done properly using double diodes from library. Power clamp designed that creates a discharge pass from vdd to gnd in ESD event.
- Basically same structure. Post layout sim says 16-18 GS/s at best. Window control to sampling cells changed to fixed window (8 delay units-depends on sampling rate) and variable window (400ps-1.5ns), each controlling 2 channels.

Chip design

- Better layouting
- Was extensively simulated (weeks) before and after layout.
- Better ESD protection
- Tools are well known

Expect the chip in one or two month for testing