Status of the 4-channel 0.13-micron Sampling ASIC

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and

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Argonne National Laboratory

Outline

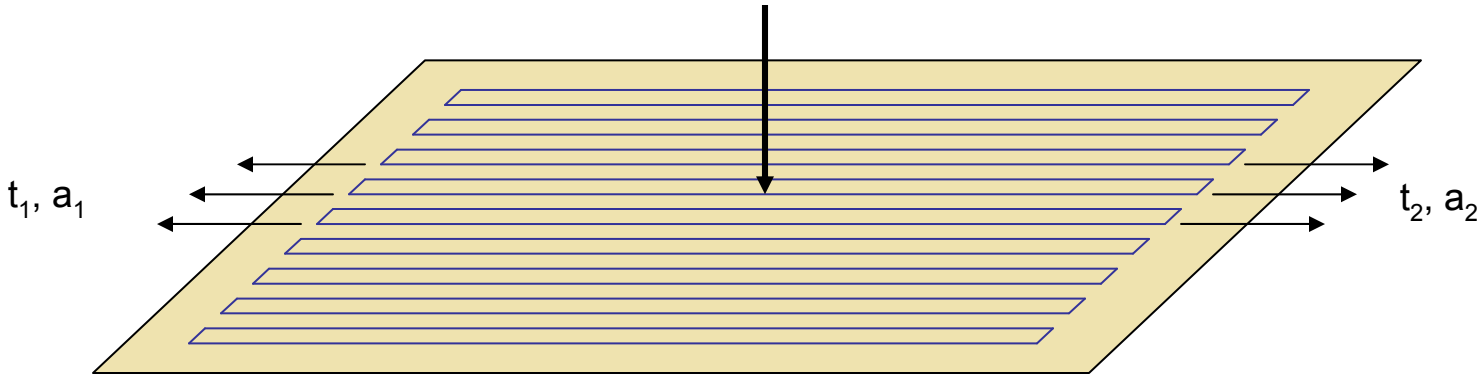
- Context, motivation
- 4-channel chip
- Next chip

Pico-second Timing: Two-dimension and Time

- Pico-second timing provides :

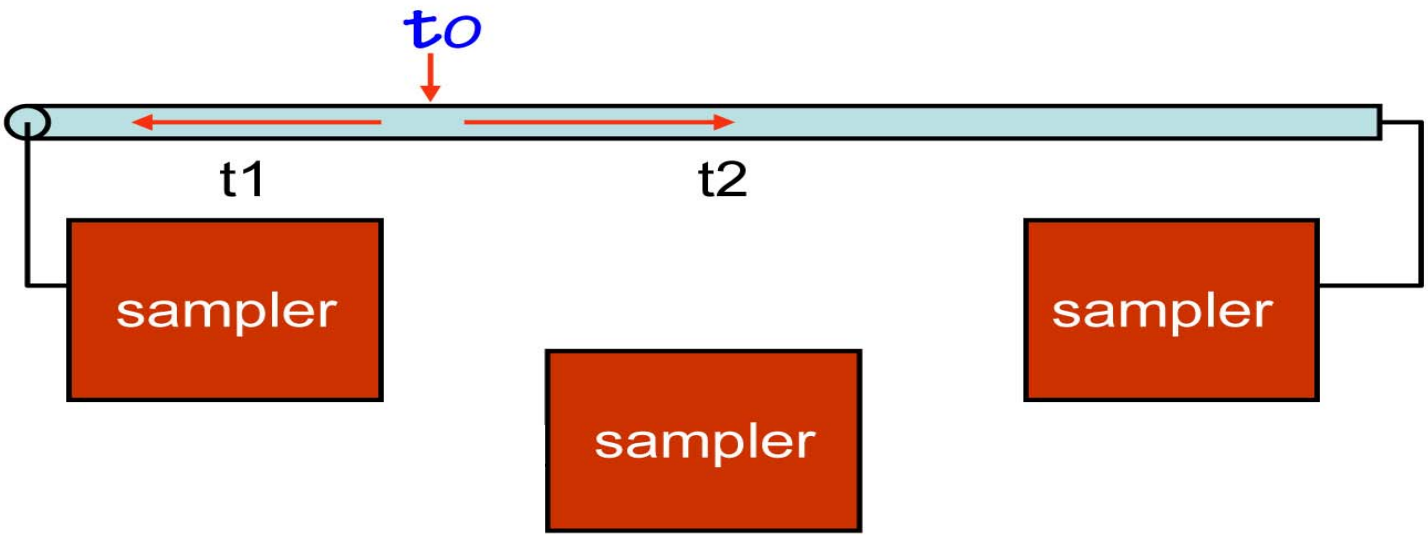
  - **Fast timing**
  - **Two dimensions with transmission lines readout down to 100 microns**
    Transverse coordinate from centroids

    Less electronics channels for large area sensors



$\frac{1}{2}(t_1 + t_2)$ = time
$v(t_1 - t_2)$ = longitudinal position
$\Sigma \alpha_i a_i / \Sigma \alpha_i$ = transverse position

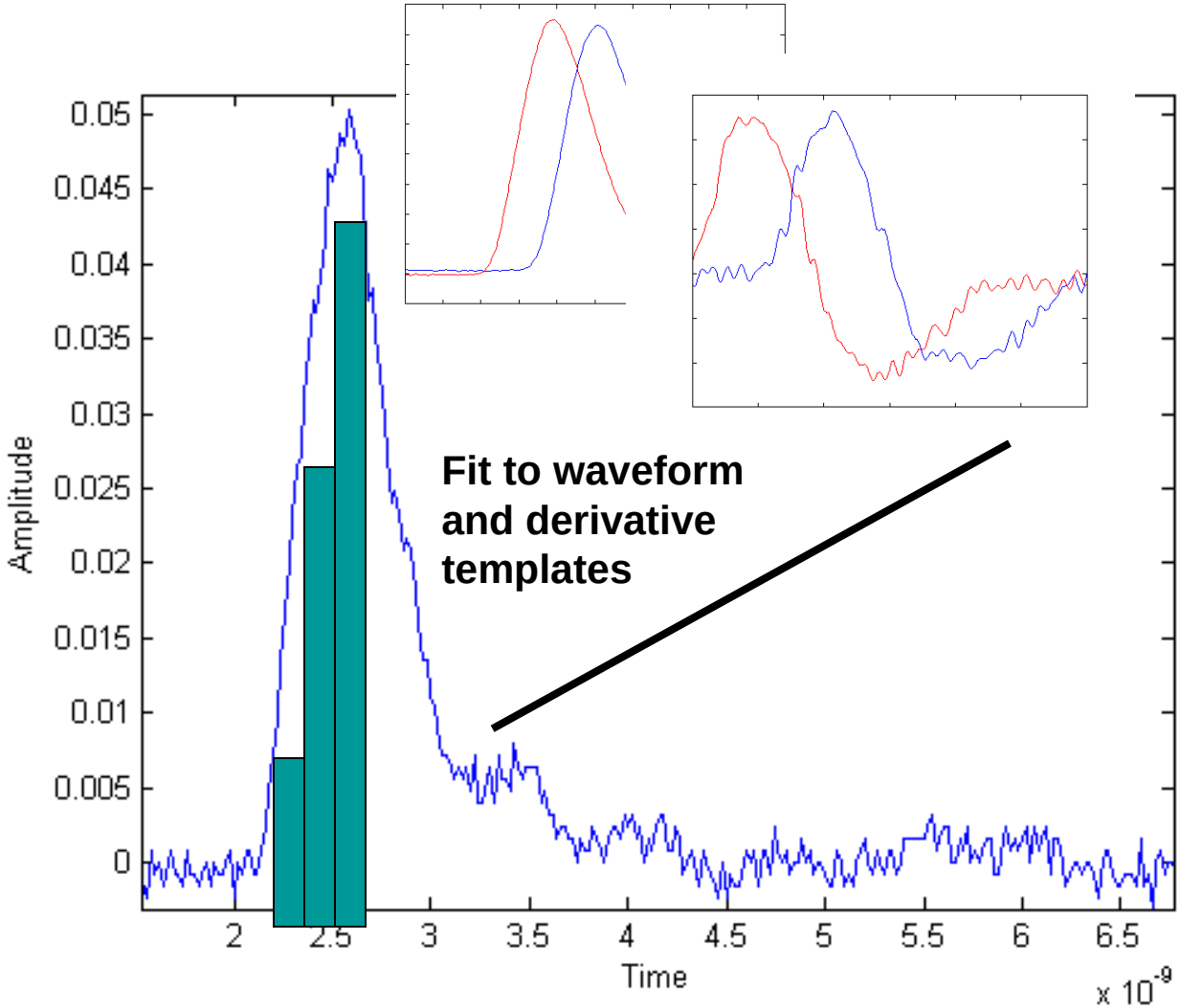
MCP Delay line readout

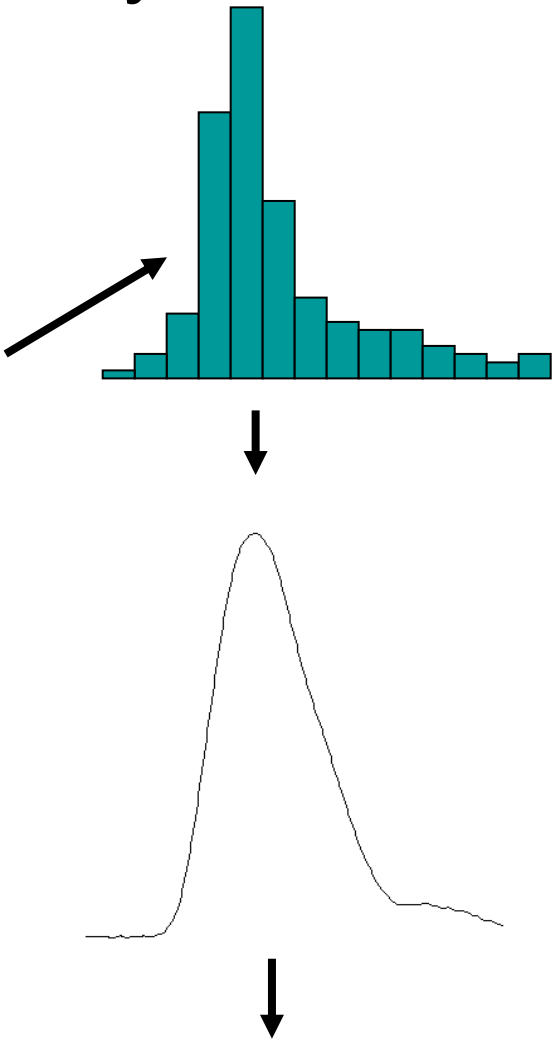


CMOS sampling chips digitize waveforms to extract timing and charge information:

- ps timing at two ends: 1D
- Centroids 2D
- fine timing t

Fast timing: Waveform Analysis

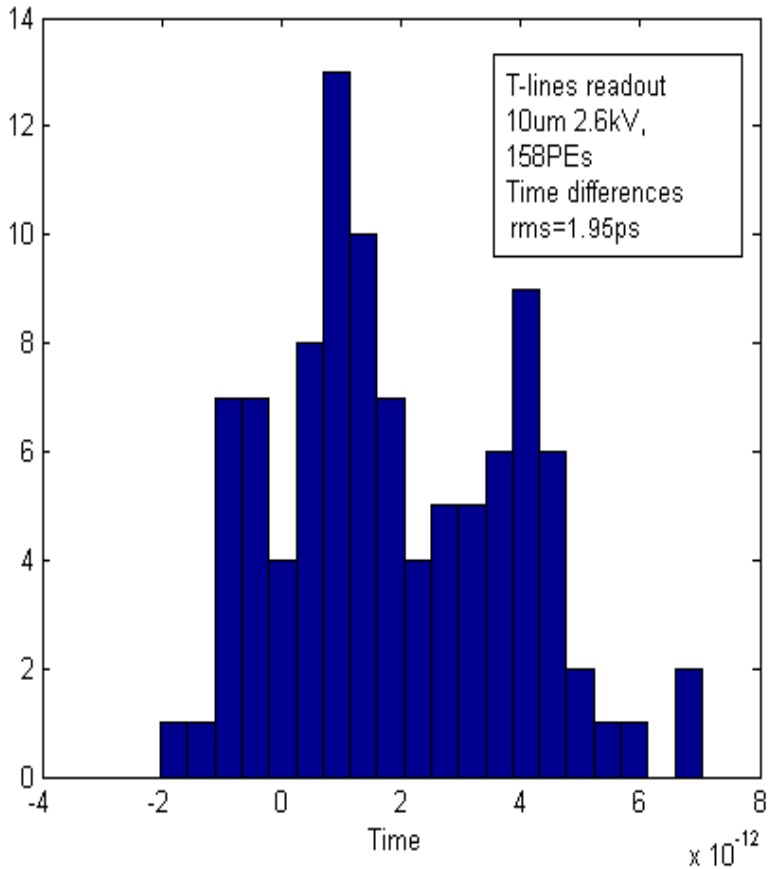




Psec Timing and Charge

Position resolution along a T-line

With Ed May
ANL 1/2009



Position resolution (velocity=8.25ps/mm) :

50PEs	**4.26ps**	**213μm**
158PEs	**1.95ps**	**97μm**

Sampling chips

Motivation:

Pulse sampling and digitization on Large Area Photo-Detectors

Store the full detector information in digital ok if:

- Detector + electronics noise >> quantization noise (LSB/√12)
- Sampling frequency > 2 x max signal frequency (Shannon-Nyquist)

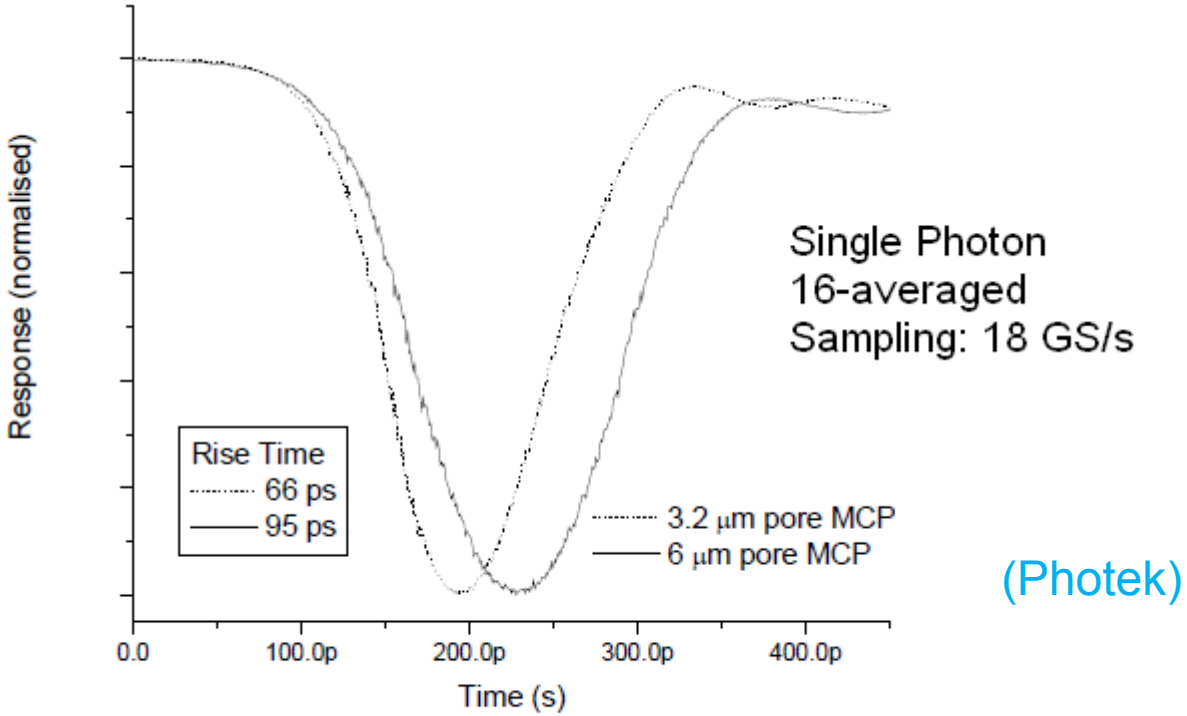
Best approach:

Digitize on the fly if sampling frequency - precision ok
No deadtime due to A/D conversion

State of the art:

8-bit 1GHz
10-bit 300 MHz
16-bit 160 MHz

Micro-Channel Plate signals



(Photek)

Time response curves for two models of PMT110 with different MCP pore diameters.

Sampled Micro-Channel Plate Signals Digital oscilloscope, 18GS/s
Signal bandwidth is 5GHz Sampling frequency > 10 GS/s

Micro-Channel Plate Readout

Noise is typically 1mV (detector+system)

If LSB set to 1mV for a 1V dynamic range,
Needs a 10-bit ADC at 10GS/s

There is no !

Analog Sampling chips:

Store analog samples at > 10 GS/s using Switched Capacitor Arrays
Digitize afterwards with a “slow” ADC

Penalty: Deadtime

Sampling Chips

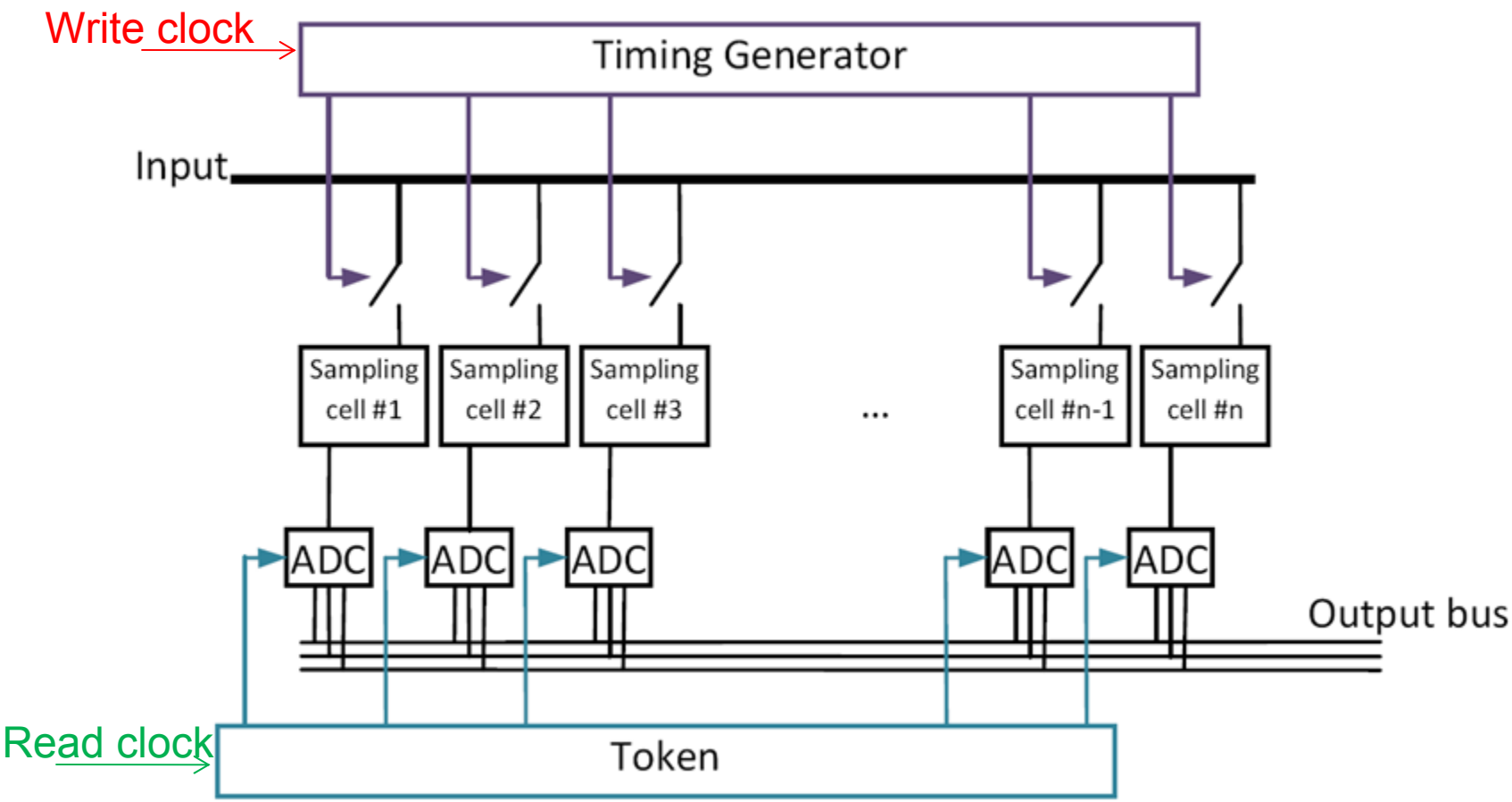
State of the art:

	Sampling GHz	Bandwidth GHz	Dyn. range bits	Depth	PLL	ADC bits	Trigger
G. Varner (Hawaii)	6	1.0	10	1024	no	12	experience
S. Ritt (PSI)	6	.8	11.5	256	3.9ps		no
D. Breton (Orsay) + E. Delagnes (Saclay)	2.5	.3	13.4	250	20ps	no	no

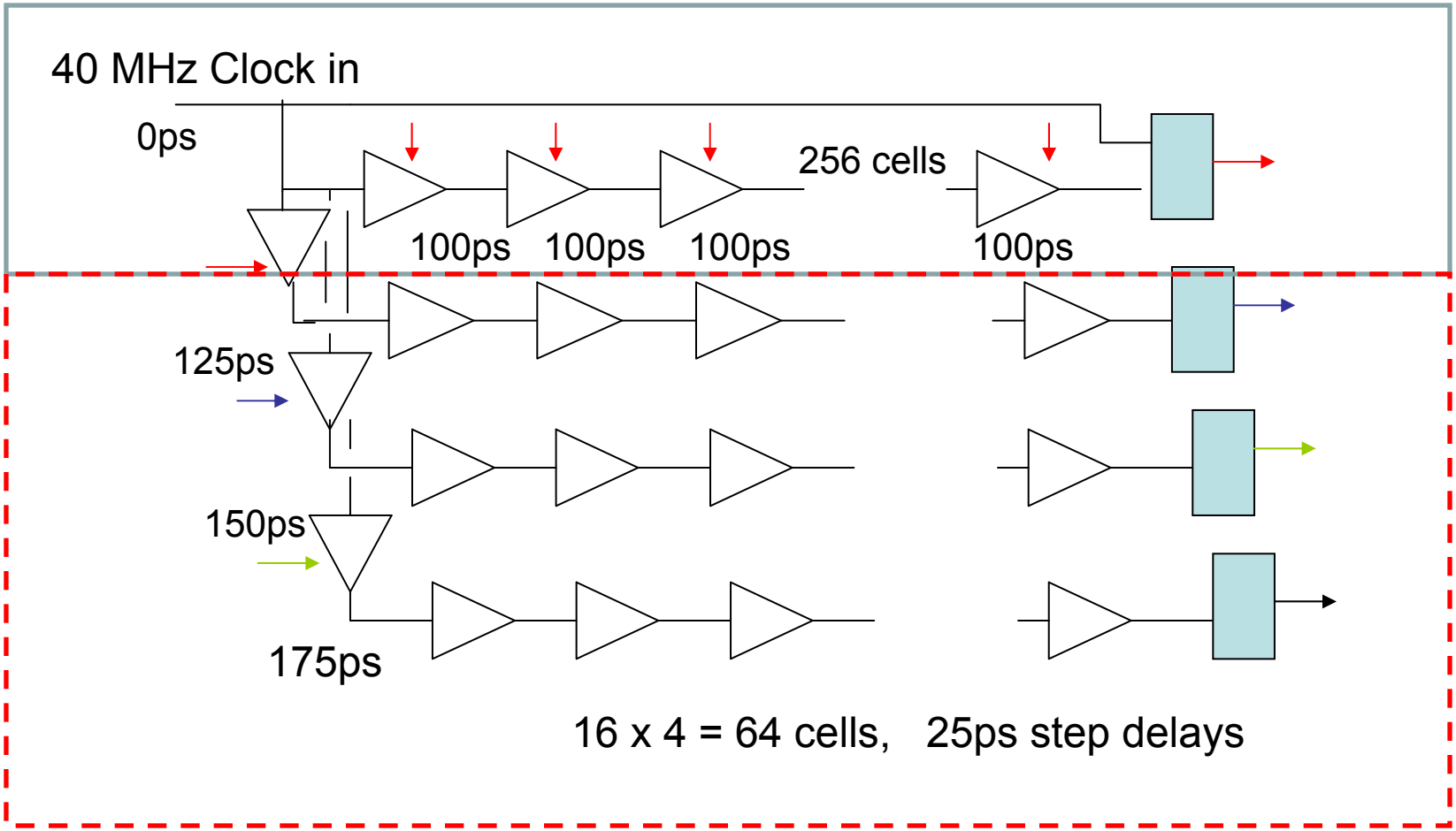
Deep sub-micron ASICs CMOS processes allow today:

Sampling 10-20 GHz
Bandwidth > 1 GHz
Dyn. Range 8-10bit

Block-Diagram



10 (40) GHz Timing generator



Present 4-channel 130nm sampling chip functions

- Prototype chip in 130nm CMOS technology (IBM 8RF-DM)

- **4-channel sampling, >10GSa/s**
- **1-2 GHz analog bandwidth, 50 Ohms**
- **40-80 MHz clock**
- **256 cells (<100ps/cell, 12.5-25ns range)**
- **Free running delays (no PLL)**
- **Sampling window 200ps-2ns**
- **Dynamic range .7V**
- **On-chip parallel 12-bit ADC (2 μs min conversion time)**
- **Free running delays (No PLL)**
- **Linearity < 1% on the full dynamic range**
- **Read clock up to 200 MHz (one cell/period)**
- **One reference channel (sampling window)**
- **1.2V power supply**
- **Power < 40 mW/channel**
- **4 x 4 mm^2**
- **120 I/Os**

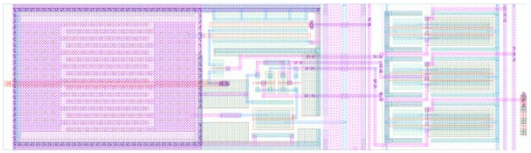
Chicago-Hawai'i-Orsay

Sent July 25th to be received Oct 21st

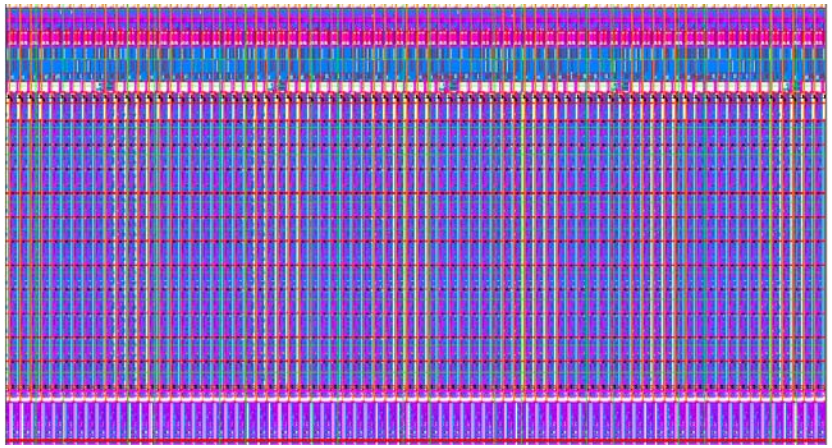
4-channel prototype chip

- First ASIC sent to foundry July 28th
- 130nm technology from IBM through MOSIS
- >10 GHz sampling, >1.5 GHz analog bandwidth
  >8-bit precision
- Expected next Wednesday

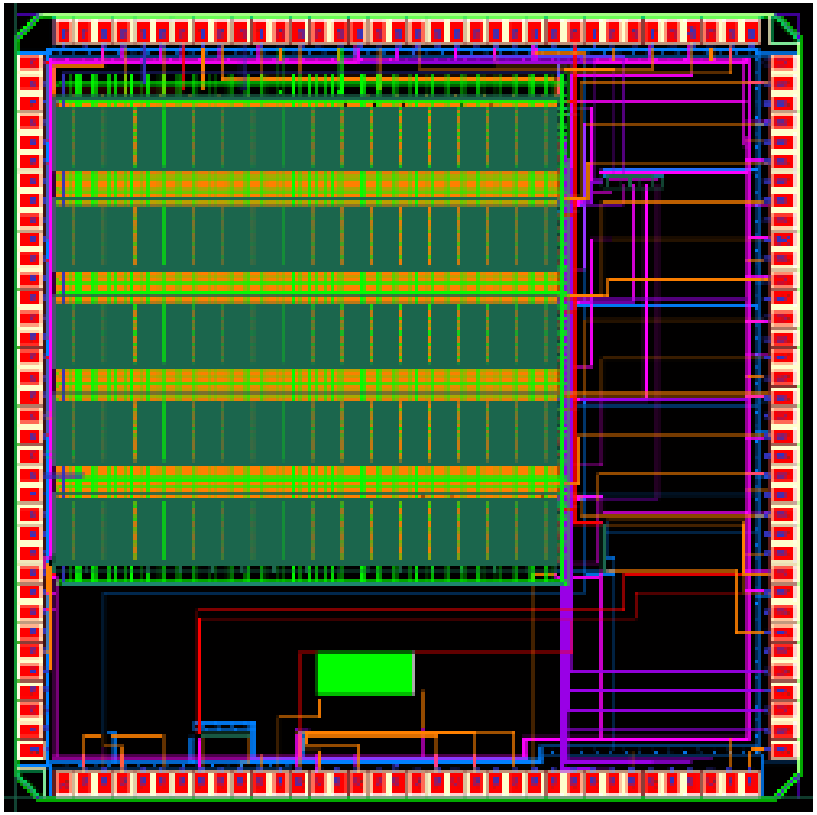
Sampling chip layout



One sampling cell

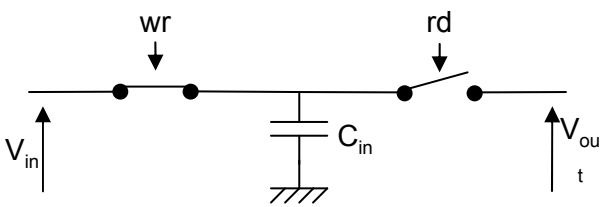


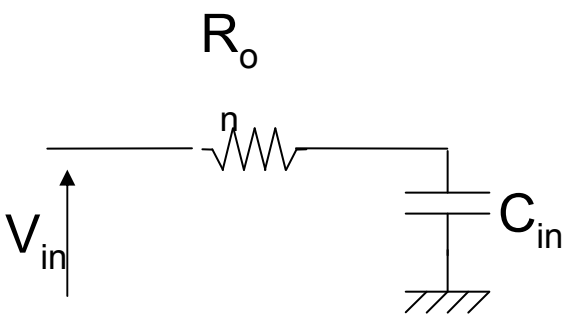
One channel



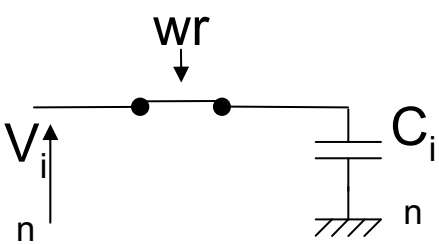
CMOS 130nm IBM 4 x 4 mm^2

Storage cell design (Herve Grabas)





Principle



Write state

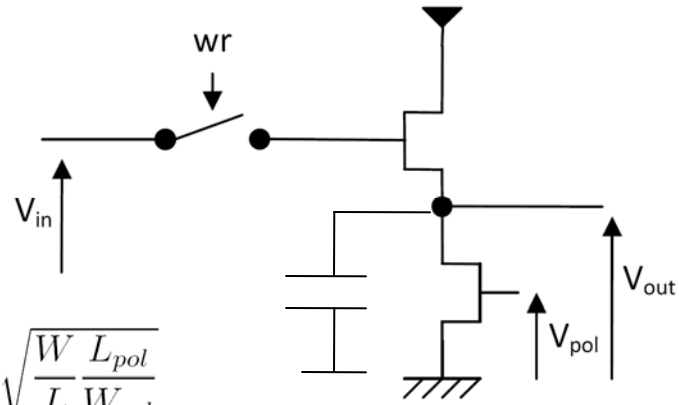
analog bandwidth is $1/(2\pi RC)$

R and C minimum, but limited by the stray capacitor of the switch, and the leakage currents of the switch in the open state.

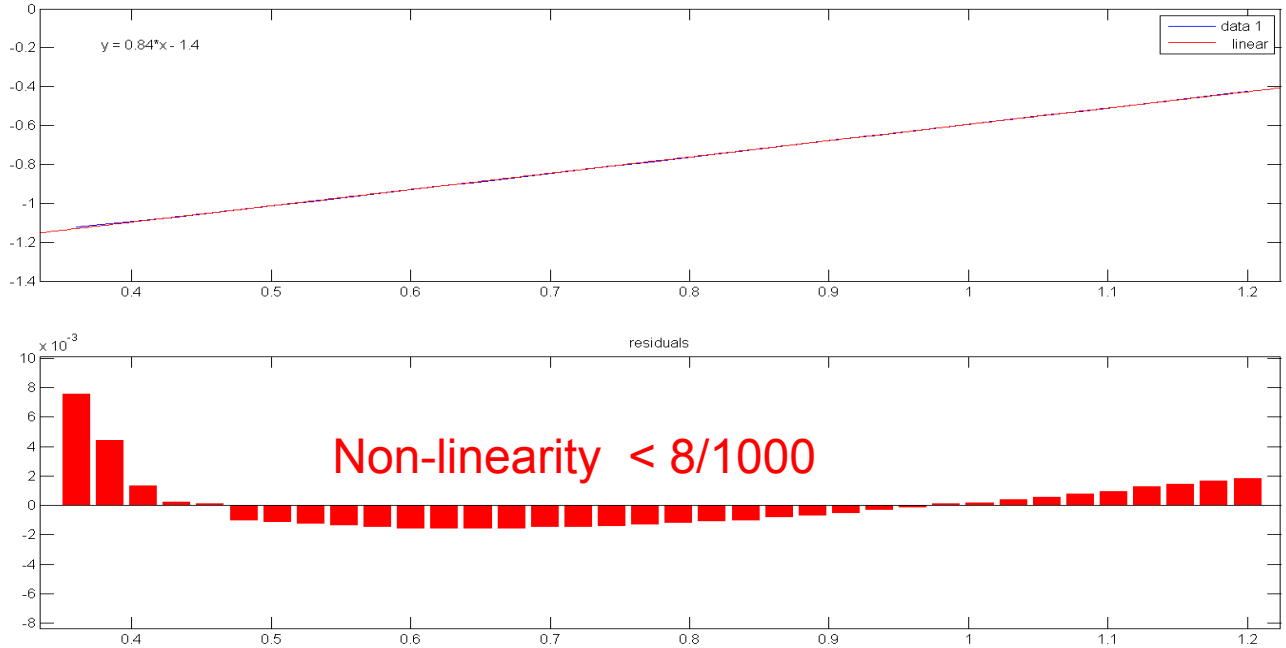
R=1.5kΩ, C = 40 fF BW=2.6 GHz (1.6 with parasitics)

Storage cell design

The gate of the source follower transistor is part of the sampling capacitor

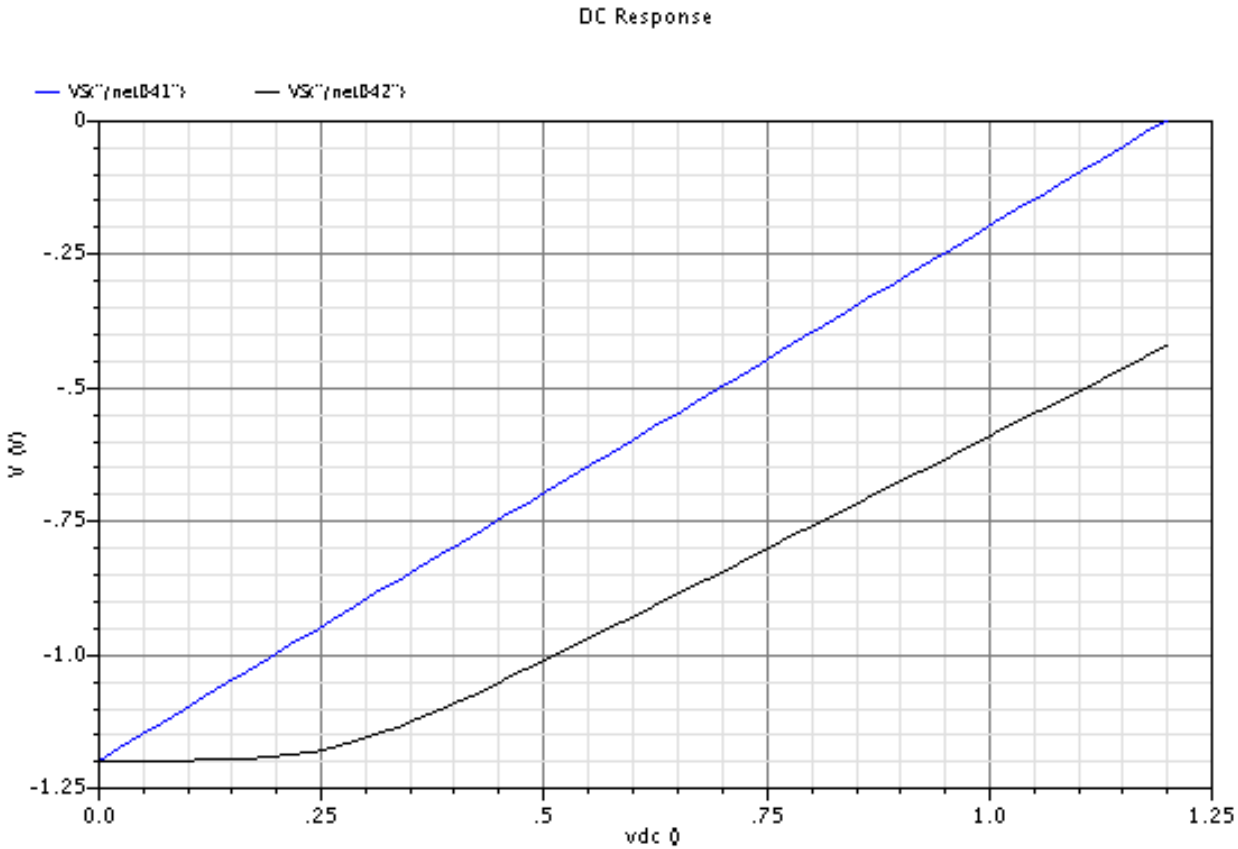


$$V_{out} = Vin - V_T - (V_{pol} - V_T)\sqrt{\frac{W}{L}\frac{L_{pol}}{W_{pol}}}$$



Herve Grabas

DC Transfer function (SPICE)



Input (blue) Output(black)

Herve Grabas

Tests (see Larry Ruckman and Eric Oberla's talks)

DC tests

- DC power vs biases,
- Ring oscillator, ADC ramp, Token passing, Comparator, Sampling cell

AC tests

- Chip on board (wire-bonding)
- DACs,
- FPGA,
- USB interface (in the FPGA),
- Fast analog pulser
- F/w and s/w: load FPGA, program and trigger pulser, control DACs, Read digital data, manage results,

Functional and parametric tests:

- Sampling cell output vs input and sampling window,
- Step response, sine wave response, analog bandwidth
- Max sampling rate
- Leakages (voltage droop),
- Resolution
- Crosstalk
- Linearities, dynamic range,
- Readout speed.

Next chip

- Measure and understand the first version (see Eric Oberla's talk) to be delivered Oct 21st.

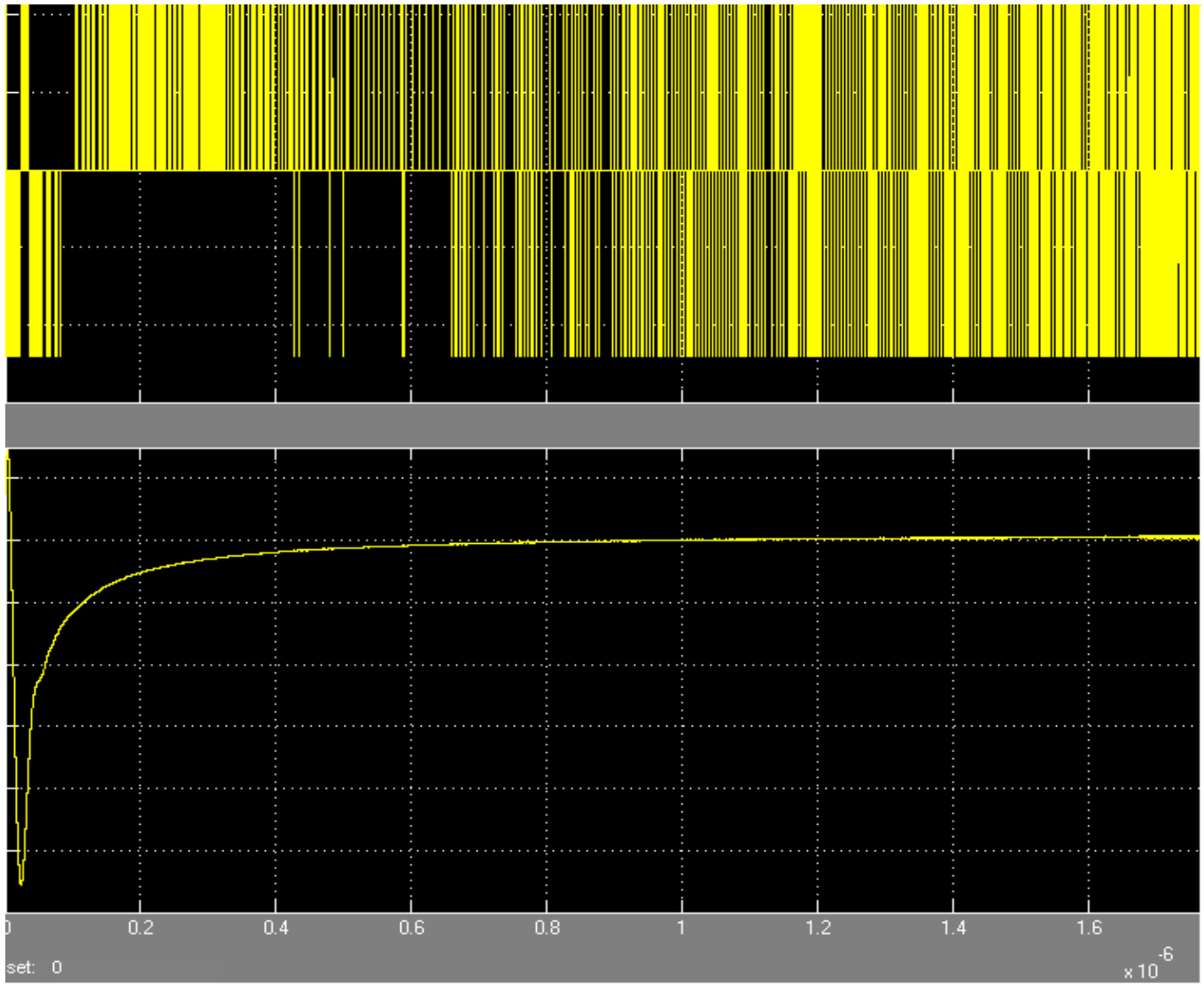
- Include:

  - Input trigger discriminator
  - Phase lock (T, supply, process insensitivity)
  - Increase write clock frequency from 40 to 160 MHz
  - Improve analog bandwidth 1.5 to 2GHz
  - Improve sampling frequency 10 to 20 GS/s

- Next 130nm CMOS runs at MOSIS: Feb 1st, May 10th ?

Phase lock 2GHz PLL

Phase corrections



Time

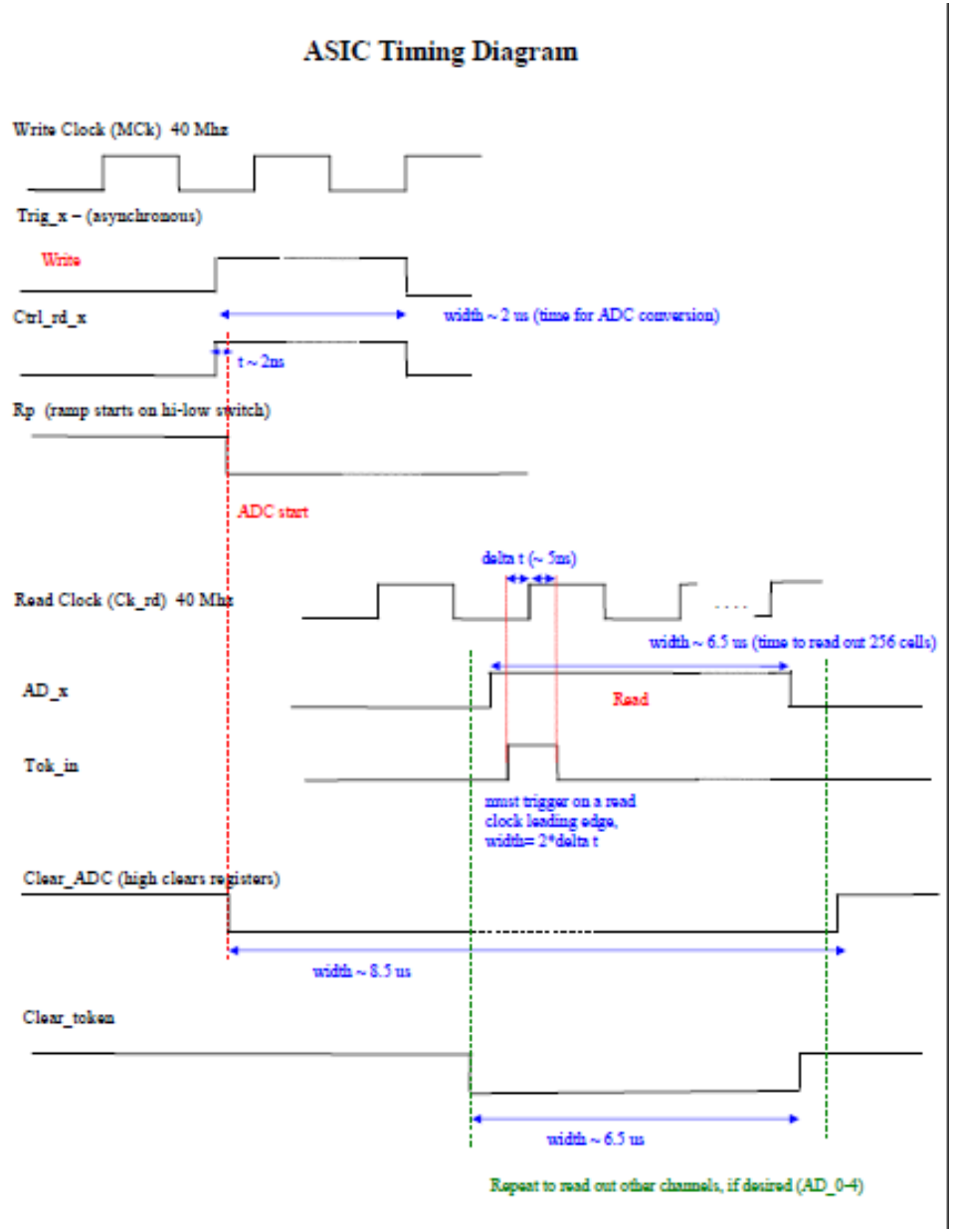
Summary

- 130nm chip sent to MOSIS in July
- To be received next week
- Next chip:
  Try to improve performance from first chip test results

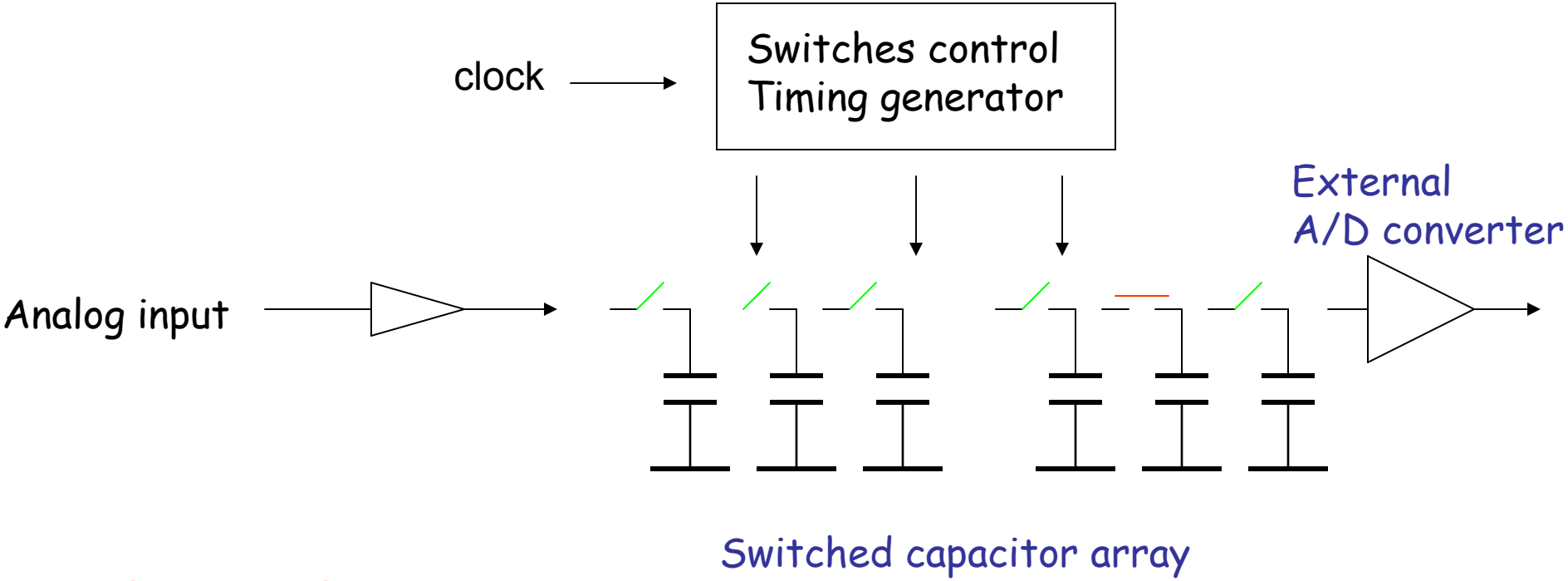
Extra slides

Sampling chip timing

Eric Oberla



Sampling chips

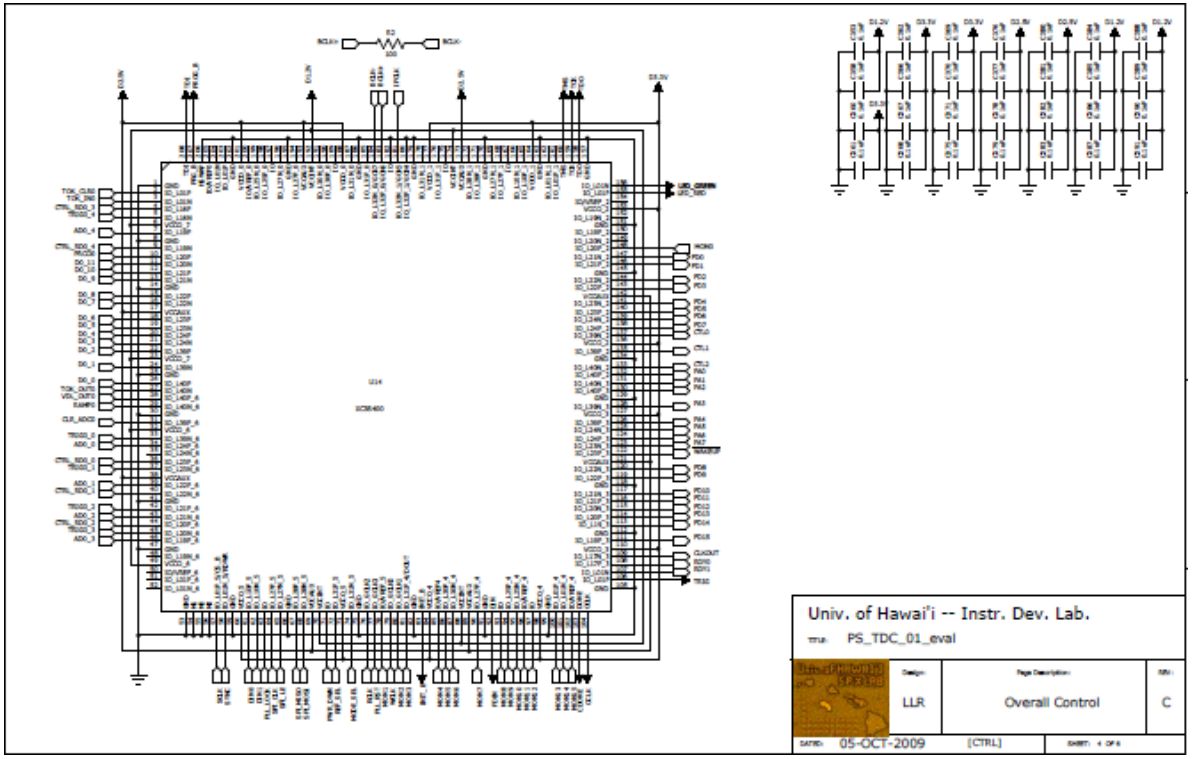


- Sampling frequency
- Analog bandwidth
- Analog dynamic range
- Depth
- Readout frequency
- Maximum hold time

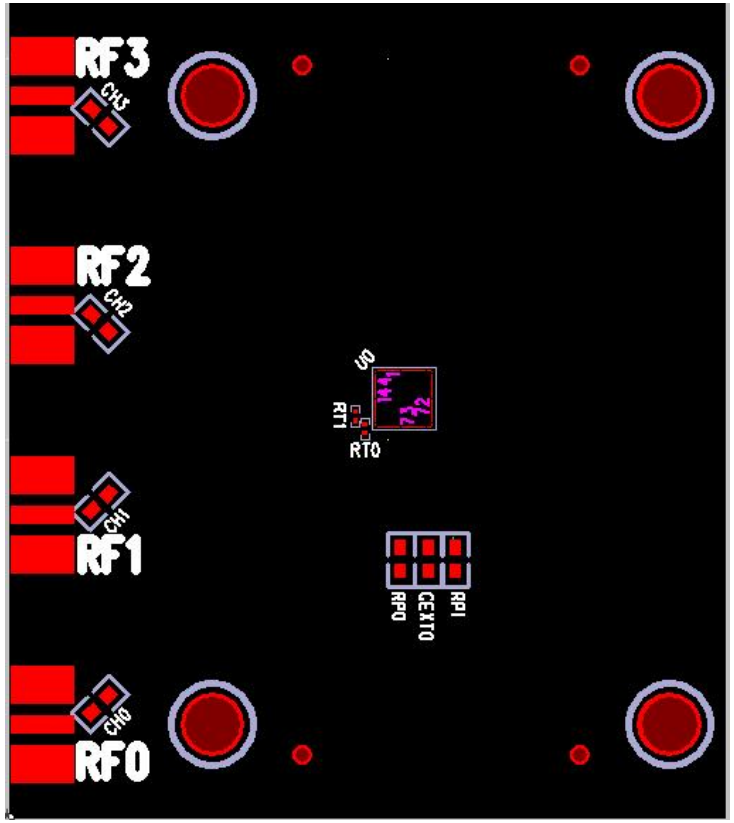
AC test card

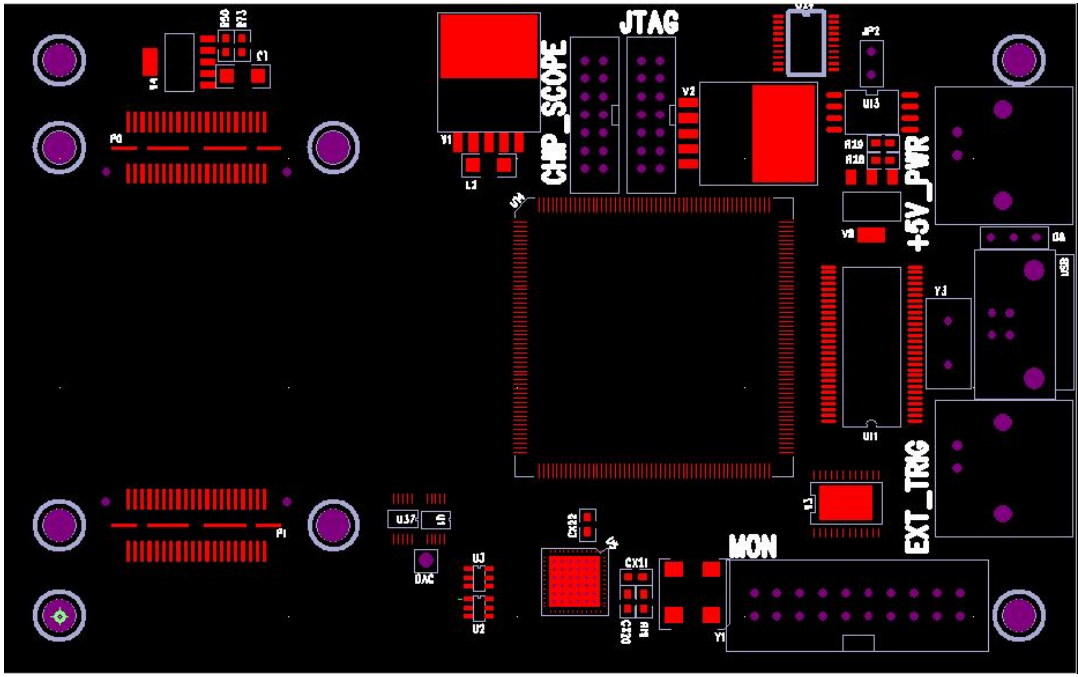
The firmware is completely written.
Here's the report from compiling it.
==========
This firmware includes:
- USB interface
- PLL CTRL
- PS_TDC_01 ASIC readout [3x RAMS]
- Chipscope [11x RAMS =
4096 samples deep by 43 bits wide]
- Basic CTRL_loop for (VG2P,VG2N)
and (VCP,VCN) [2x RAMS]

Larry Ruckman, Hawai'i



AC test card





AC tests Digital card (FPGA)

AC tests analog card
All 50 Ω matched

Larry Ruckman, Hawai'i