Status of Testing Activities in Hawai'i

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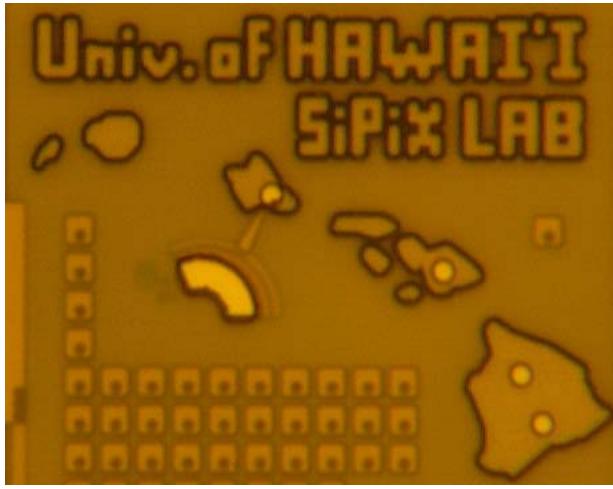
Larry Ruckman,
Gary Varner



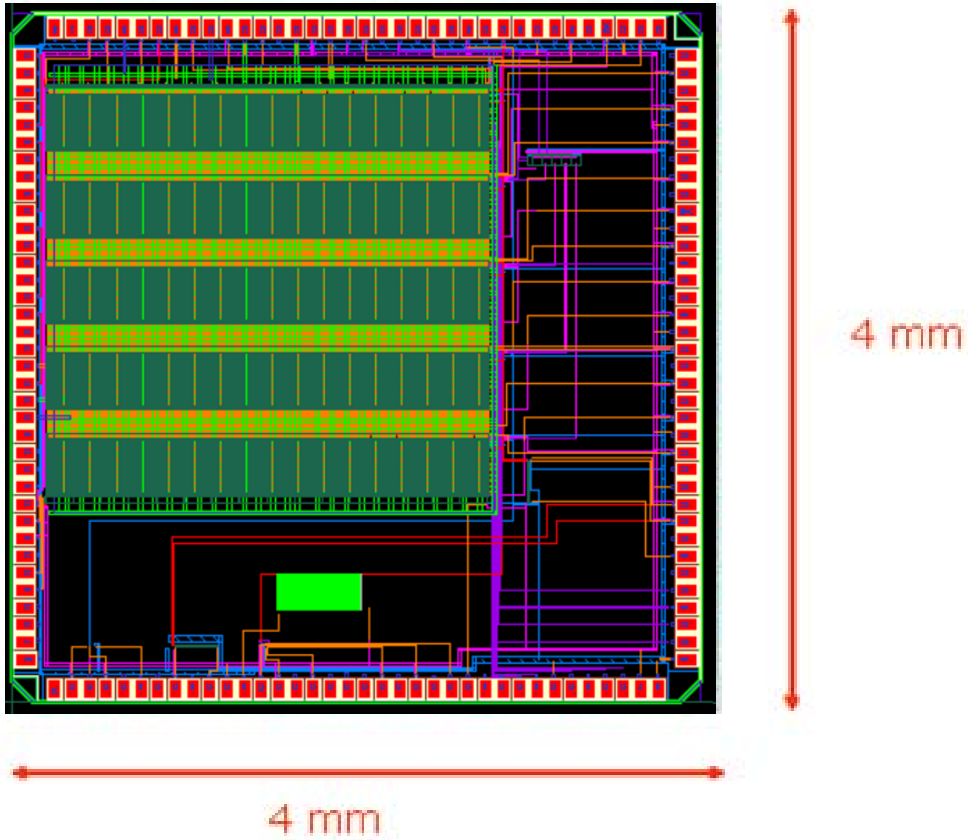
Feb. 25, 2009

psTDC1 – another “oscilloscope on a chip”

Specifications

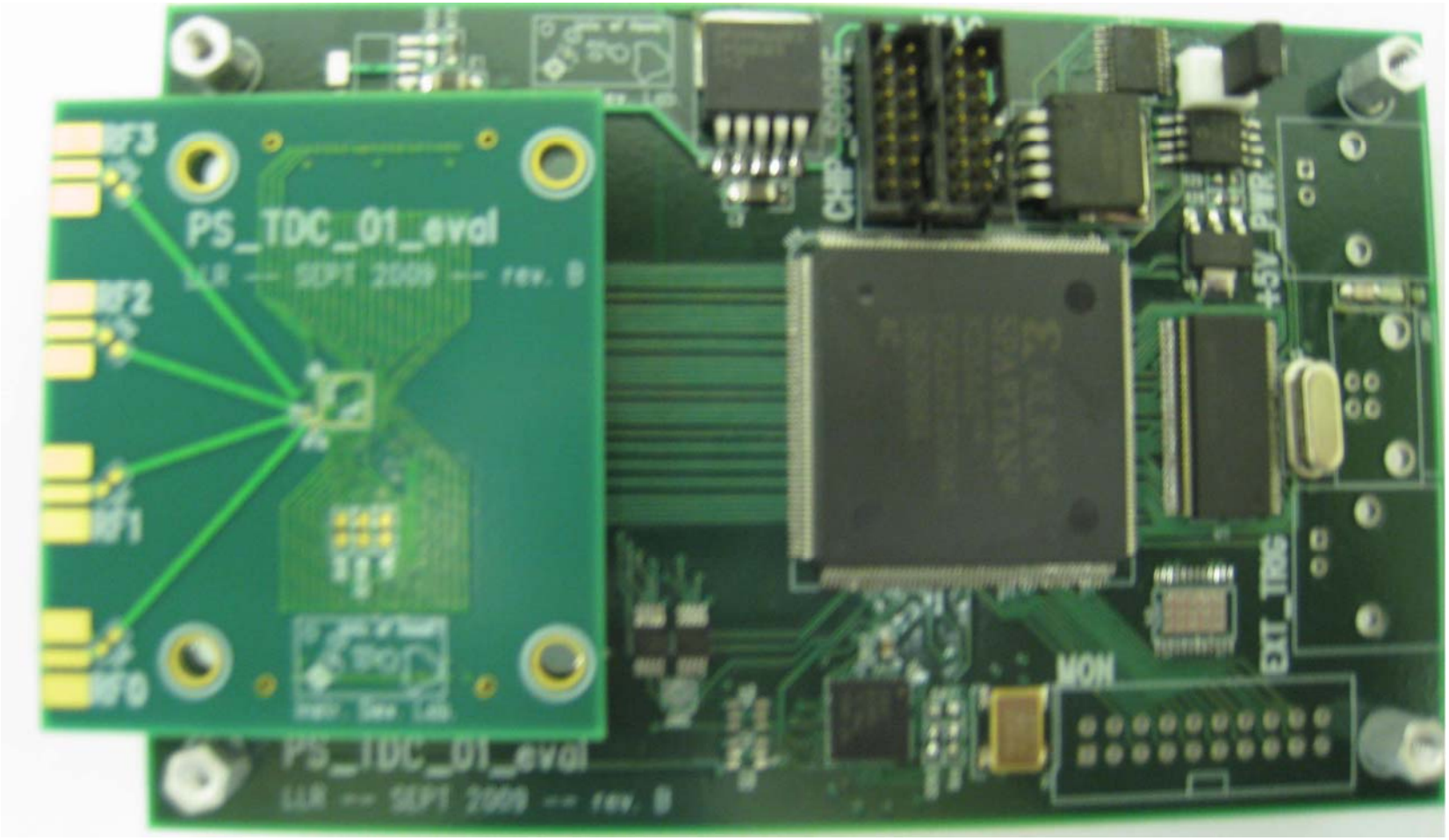
- 10-15 GSa/s
- >= 2GHz analog bandwidth
- 256 sample cells
- 4 channels
- separate timing channel
- on-chip conversion
- IBM 130nm CMOS process
- 25.6μs readout
- 40mW/channel
- Direct interface (stud-bond) to microstrip board

Chip Layout



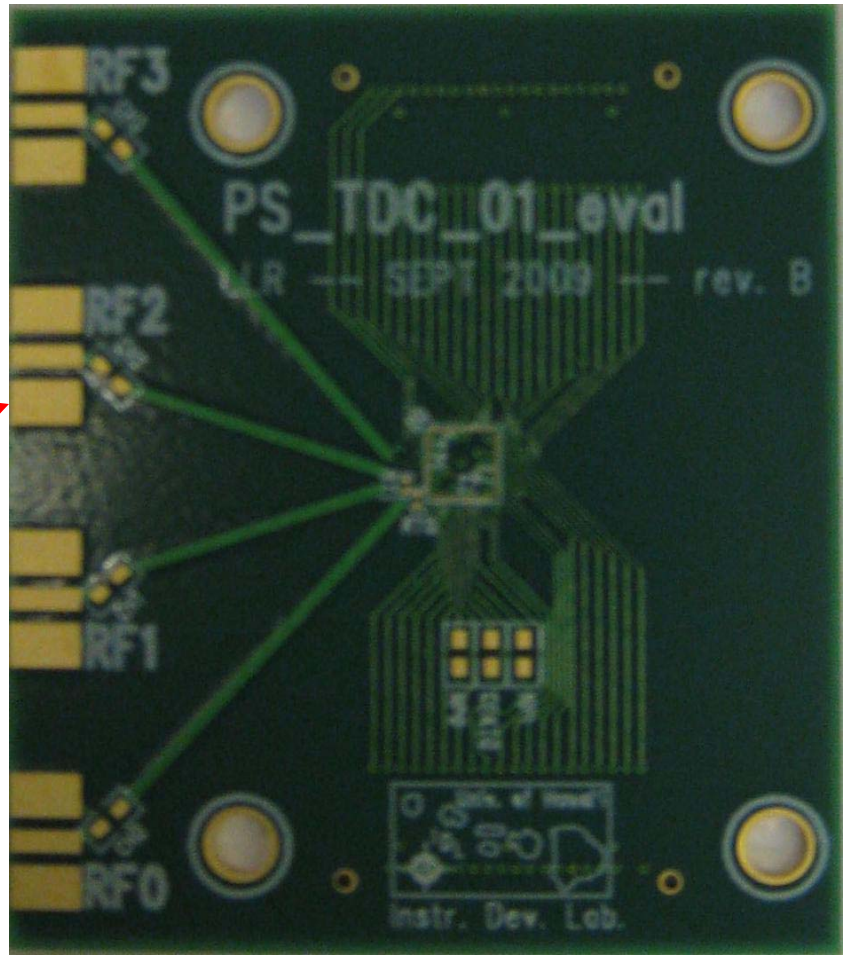
U.S Department of Energy | Argonne National Laboratory | The University of Chicago | Office of Science Department of Energy | University of Hawai'i Manoa

Analog/Digital PCB **Combo**



ASIC Evaluation Card (Analog) [A.K.A. “AC card”]

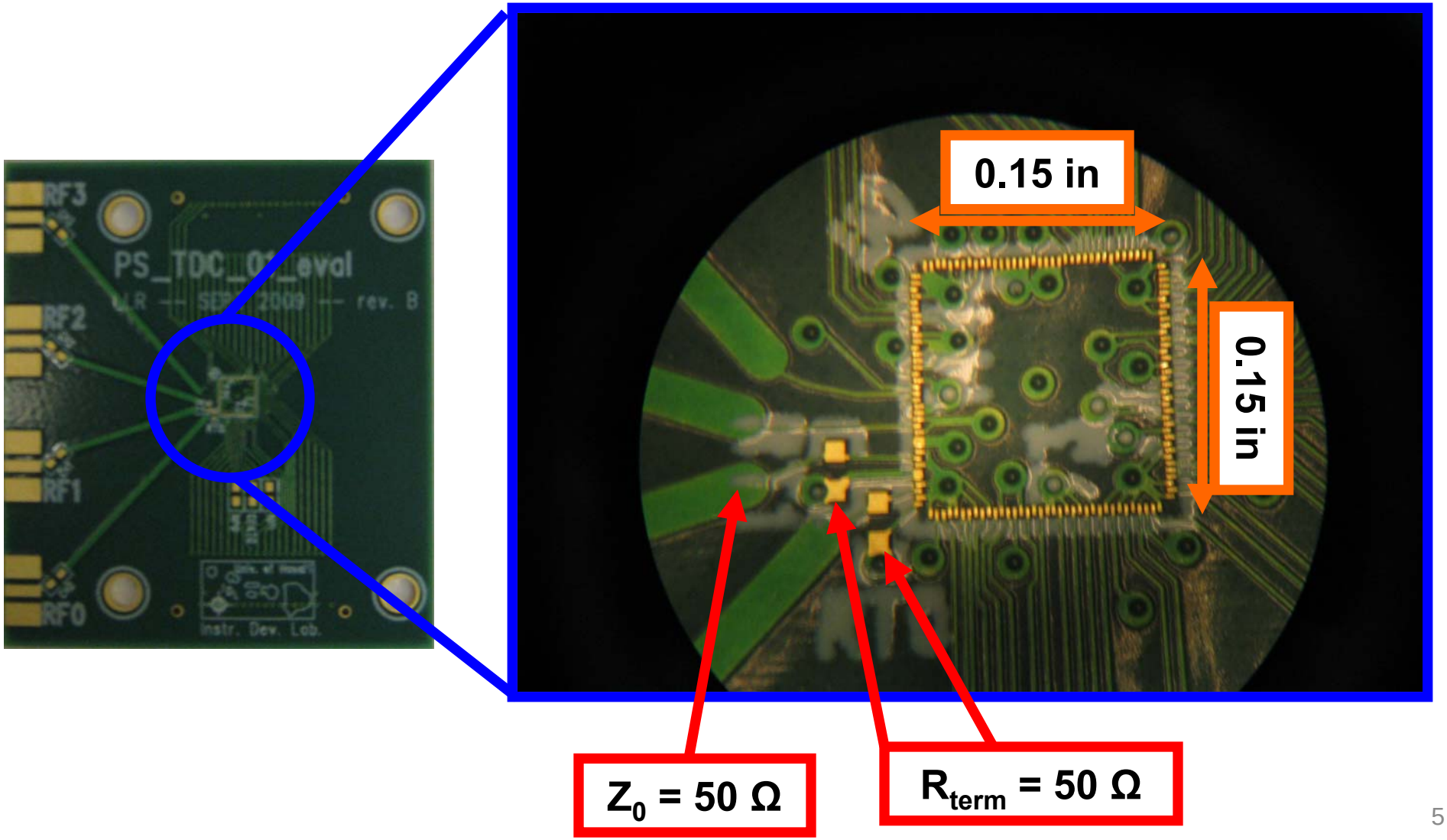
- 1.9 mil (48.26 micron) trace/spacing
  - laser etching
- Fairly $$$ PCB fabrication
- 4x SMA input
- 2x high density Samtec connectors
- Pluggable Mezzanine card
- NP-175 dielectric



2.5 in

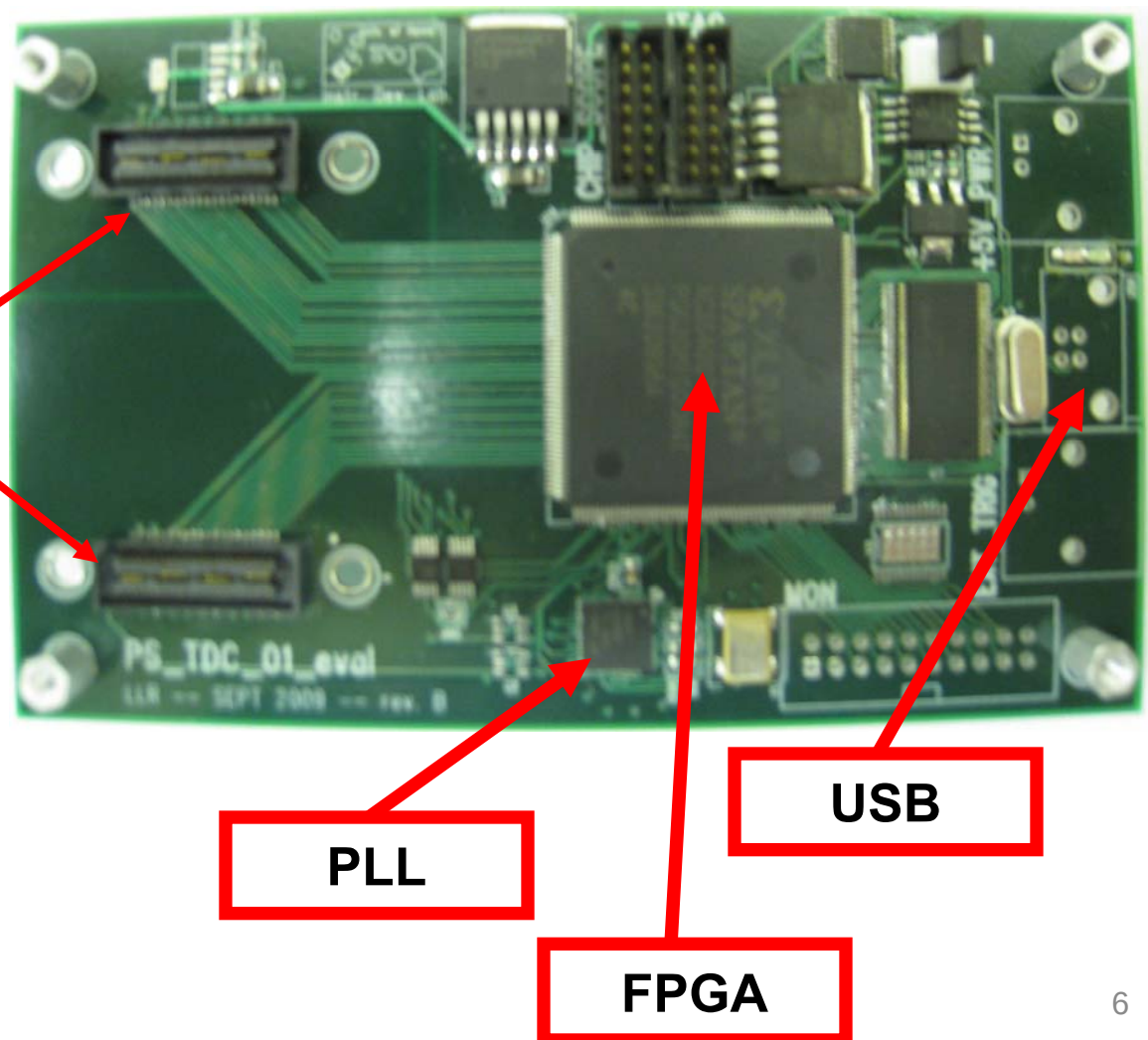
1.9 in

Flip Chip Decal (Zoomed In)



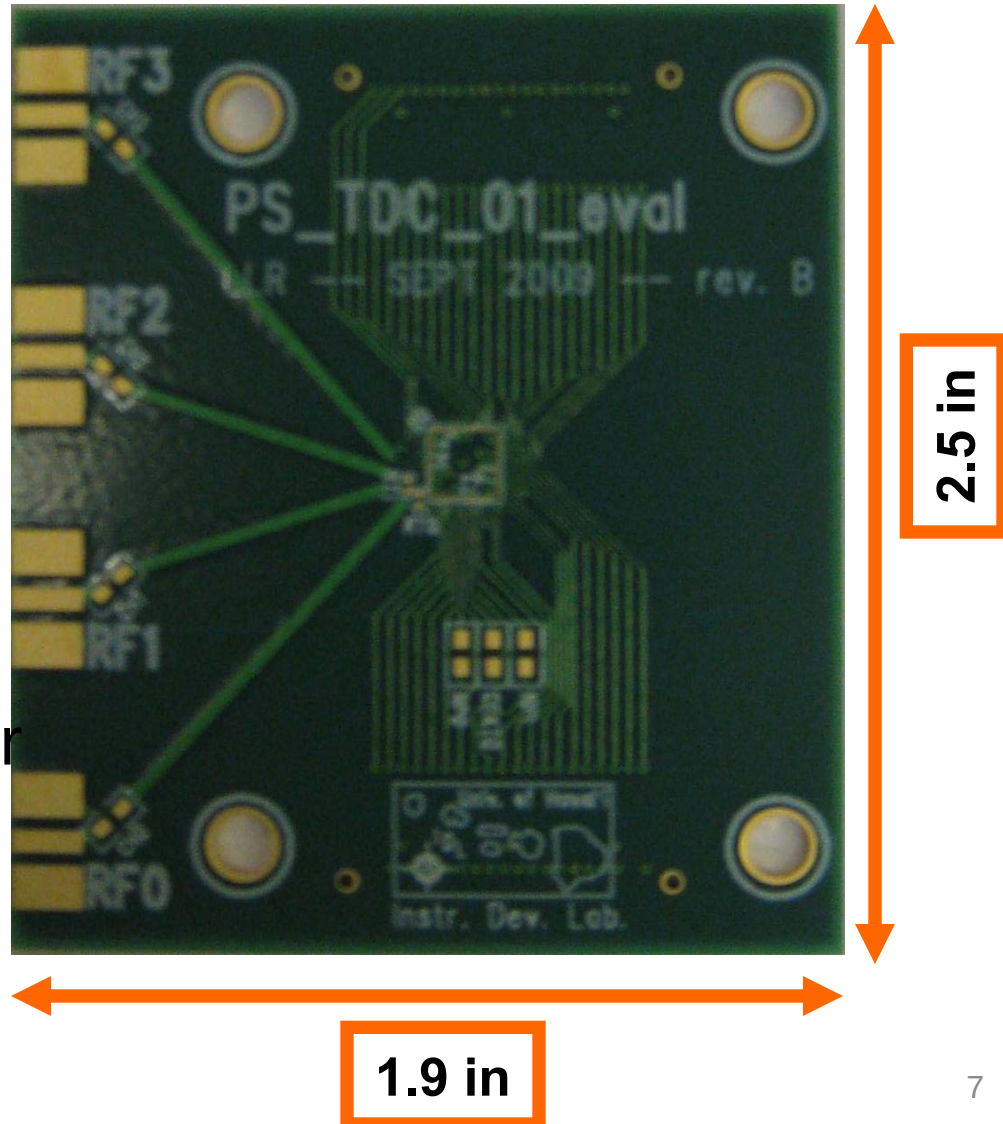
ASIC Evaluation Card (Digital)

- 6 mil trace/spacing
- Very cheap PCB fabrication
  - low risk
- 2x high density Samtec connectors
- Analog card's base board
- USB 2.0 interface



ASIC Evaluation Card (Analog)

- 5x ASIC were bump bonded by CVInc
- All 5x ASICs had at least one or more shorts between bonds
- Many lessons learned
  - Use wider pad pitch
  - Have test parameters for assembly house
  - Require small bump balls

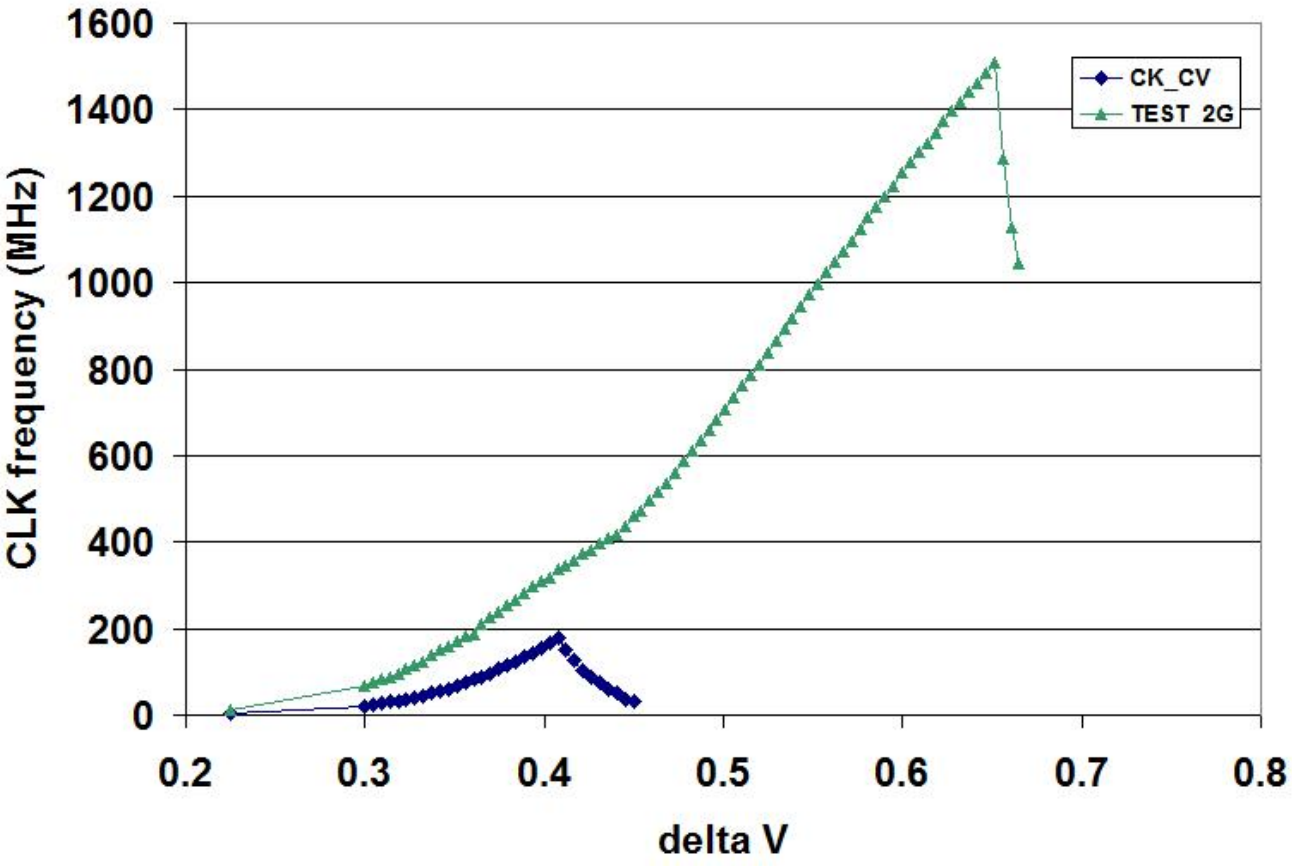


Wired Bonded Version for Hawaii Testing

- Gave up on waiting for good stud bonding
- Packaged the psTDC01 ASIC in Hawaii
- Goal: characterize ADC performance of the ASIC
- Reduced AC perform from wiring bonding, but could continue developing firmware

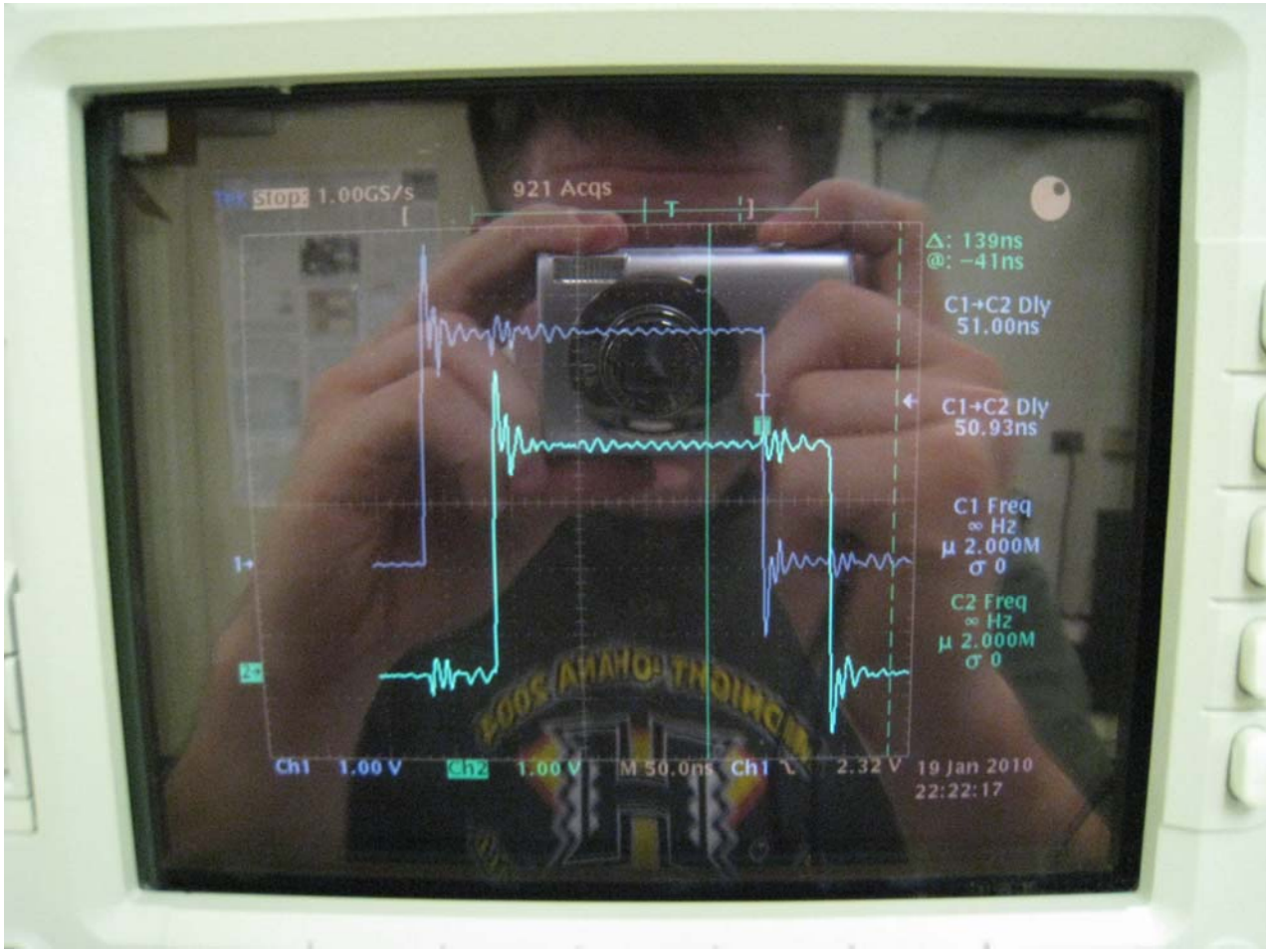
Wilk. Clock Speed

- Test Structure functioned as expected
- Actual Wlk. Clock speed extremely reduce due to lack of digital buffering of the intrinsic capacitive loading



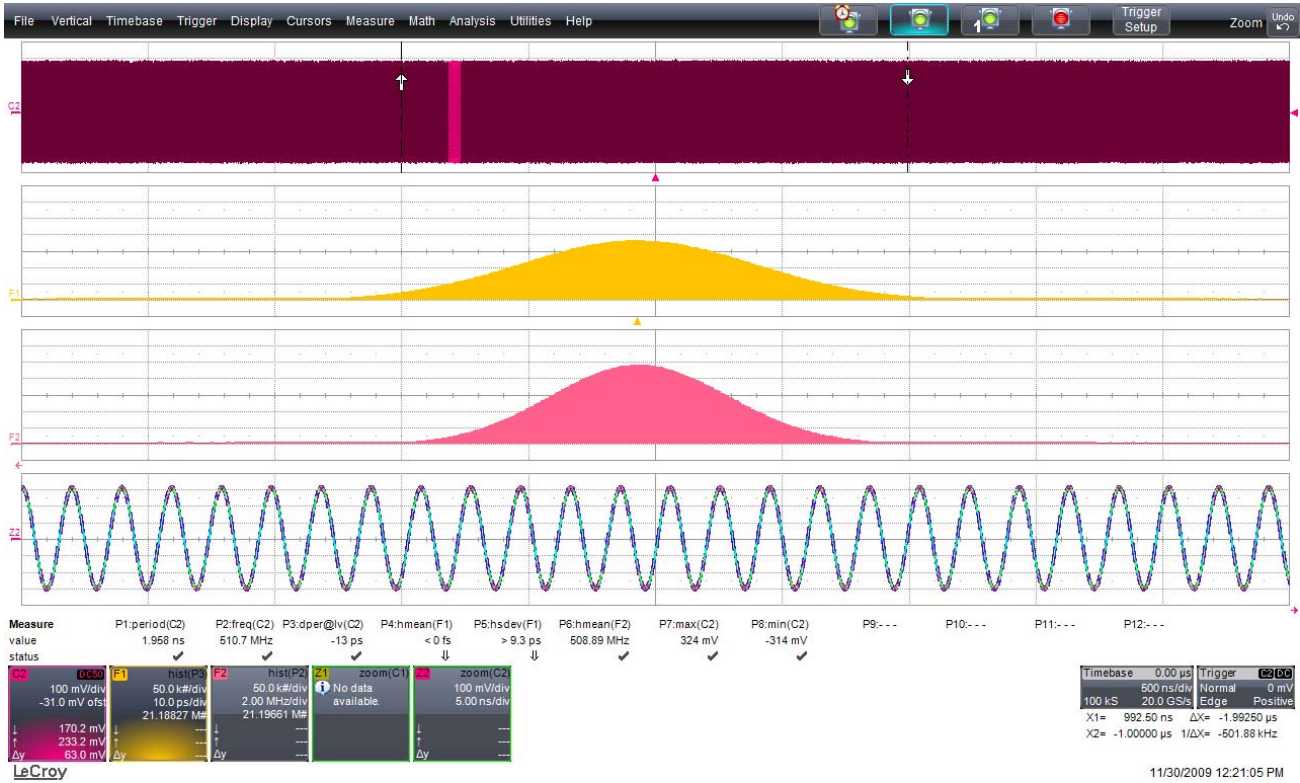
Sampling Speed

- (256 cells/50ns)
  = ~5 GSa/s “MAX”
- This doesn’t account of insertions delays in/out of ASIC
- Need an internal PLL in ASIC or calibrate via waveform data to account for insertion delays



External PLL Clock Cleaner

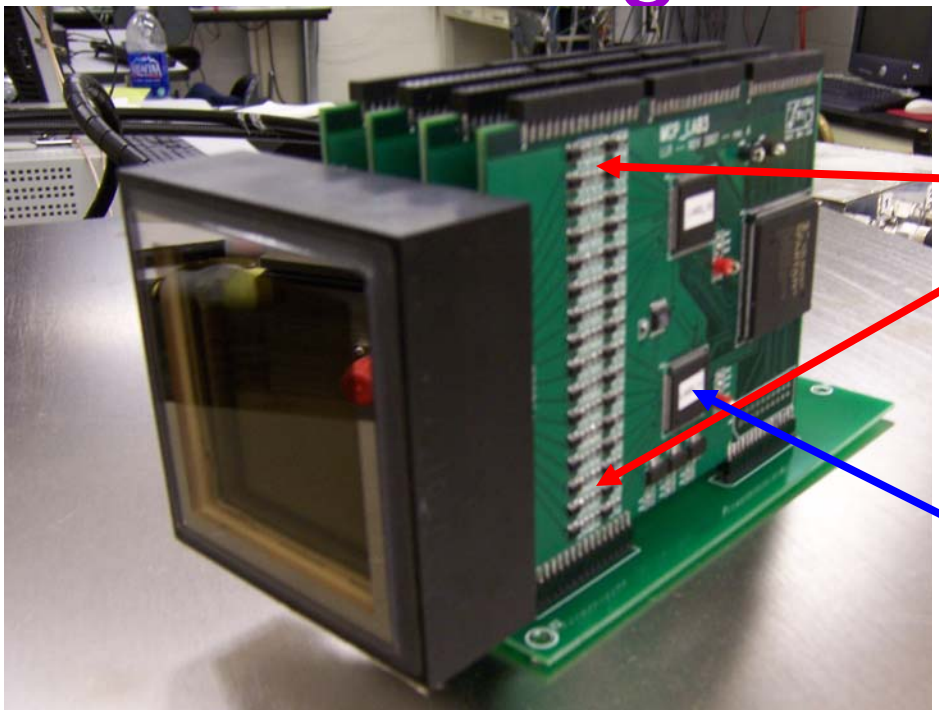
- Tested clock distribution circuit
- ~6-7 ps RMS in noise KEK electronics hut (same as raw 509 MHz used by KEKB)
- Only a simple internal PLL filter was used
- Need to investigate external PLL filtering
- Possible to get <1 ps RMS phase jitter using an external PLL filter (see TI application# SCAA095)



Unable to Digitize with this ASIC

- The artwork for the resistor in the ASIC design was not implemented
- Anything that used a resistor didn’t function as designed
  - Specifically the analog buffer that distributes the Wilk. Ramp
- Thus, without a ramp being driven to the Wilk. ADC cell, digitizing was not possible

For existing MCPs Gain Needed



Amplifiers dominate board space

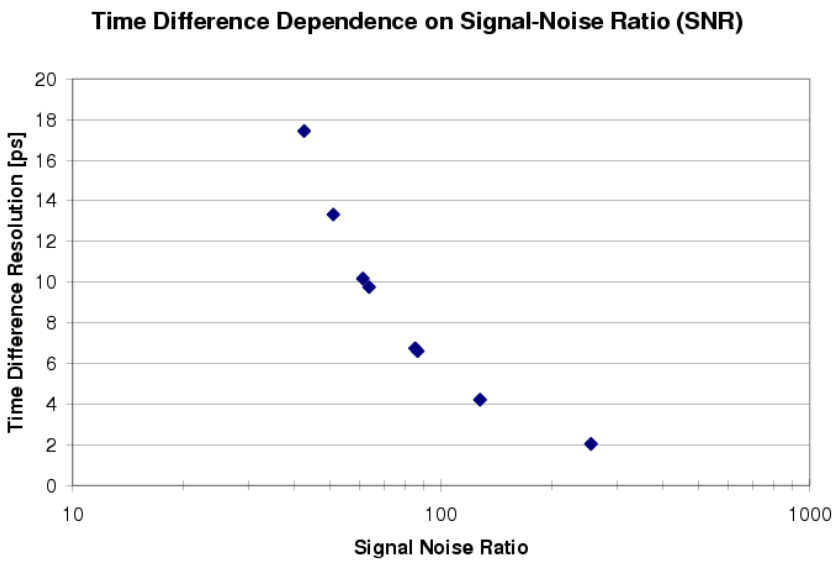
Readout ASIC pair

- What gain needed?
  - At 10^6 gain, each p.e. = 160 fC
  - At $2x10^5$ gain (better for aging), each p.e. = 32 fC
  - In typical MCP pulse, Vpeak = dQ/dt * R = 32uA * R = 32mV * R [kΩ] (6.4mV)

Gain Estimate	
Rterm	1 p.e. peak
50	1mV
1k	20mV
20k	400mV

Reason want good gain

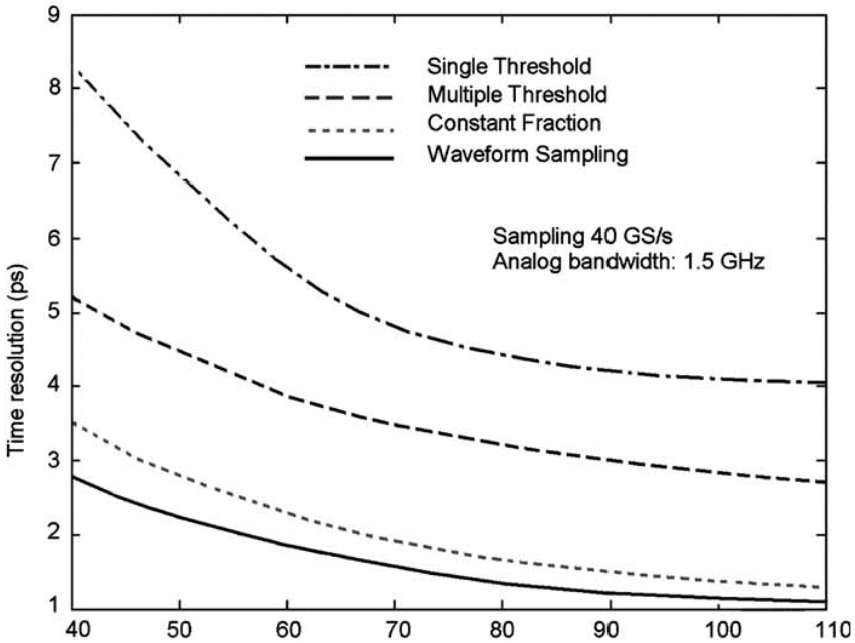
1GHz analog bandwidth, 5GSa/s



G. Varner and L. Ruckman

NIM A**602 (2009) 438-445**.

Simulation includes MCP response



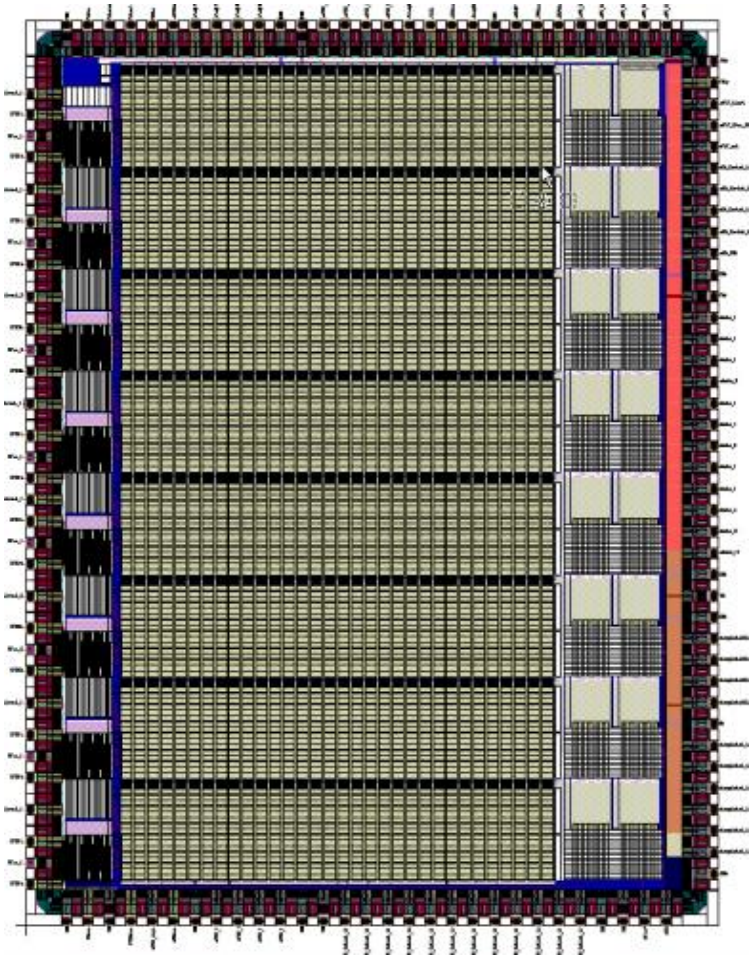
J-F Genat, G. Varner, F. Tang, H. Frisch

NIM A**607 (2009) 387-393**.

An Alternative (existing) ASIC

BLAB3 Specifications

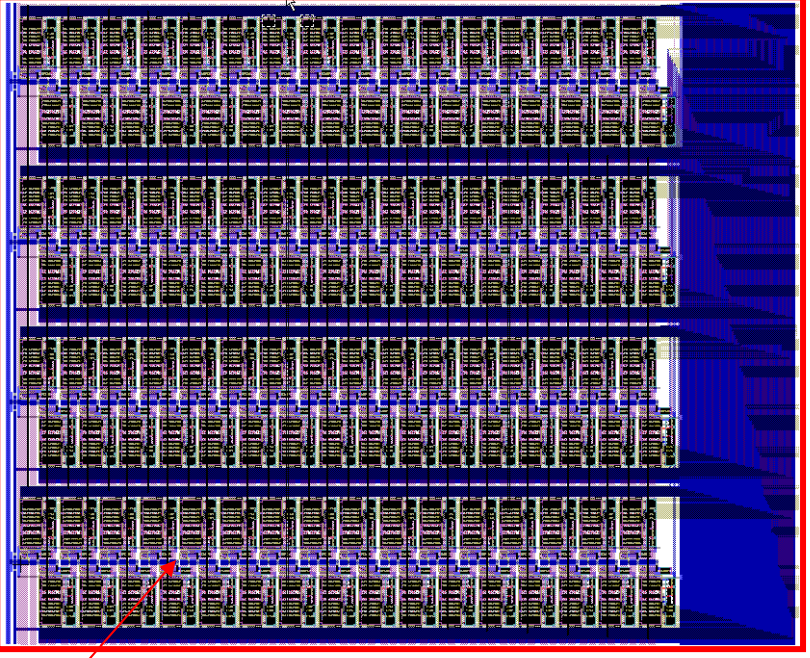
32768	samples/chan (>5us trig latency)
8	channels/BLAB3 ASIC
8	Trigger channels
~9	bits resolution (12[10]-bits logging)
64	samples convert window (~16ns)
4	GSa/s
1	word (RAM) chan, sample readout
1+n*0.02	us to read n samples (of same 64)
30	kHz sustained readout (multibuffer)



TSMC 0.25um

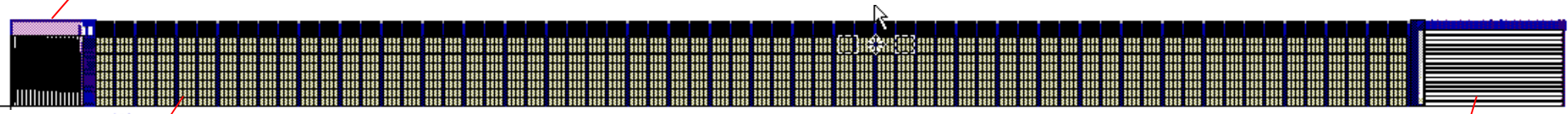
- Time alignment critical
  - Synchronize sampling to accelerator RF clock
  - >5us a must for trigger, since single photon rates high

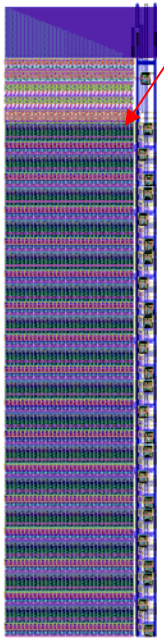
BLAB3
Single Channel



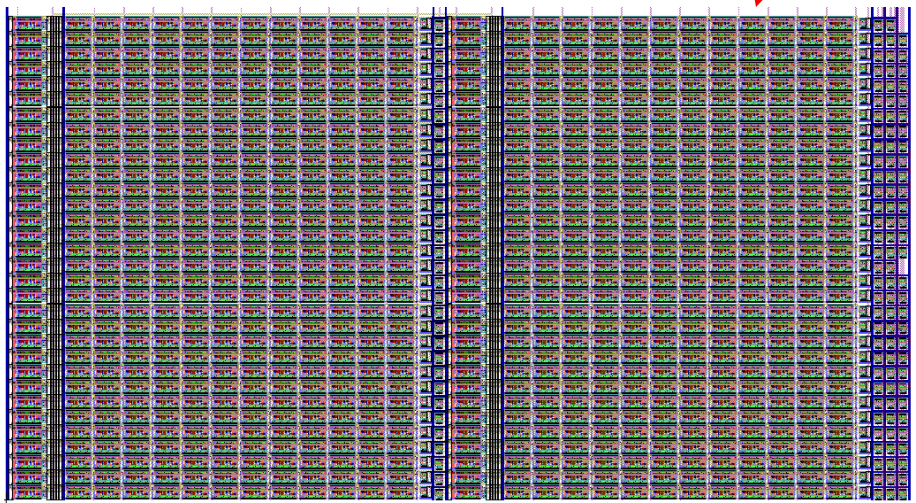
- Sampling: 128 (2x 64) separate transfer lanes

Recording in one set 64, transferring other (“ping-pong”)



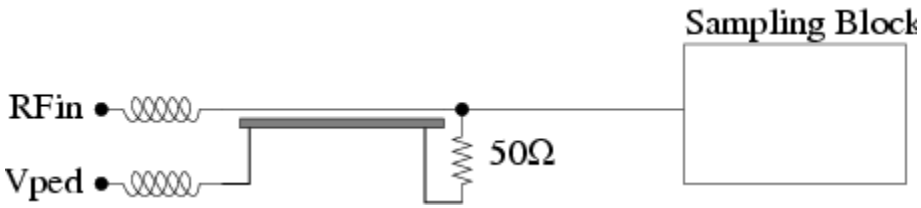


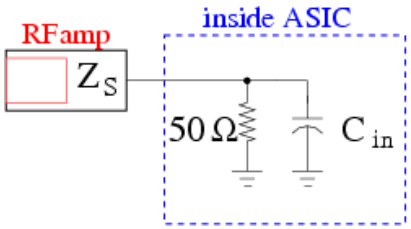
- Storage: 64 x 512 (512 = 8 * 64)

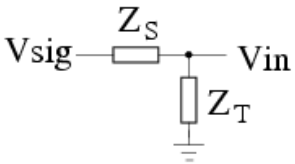


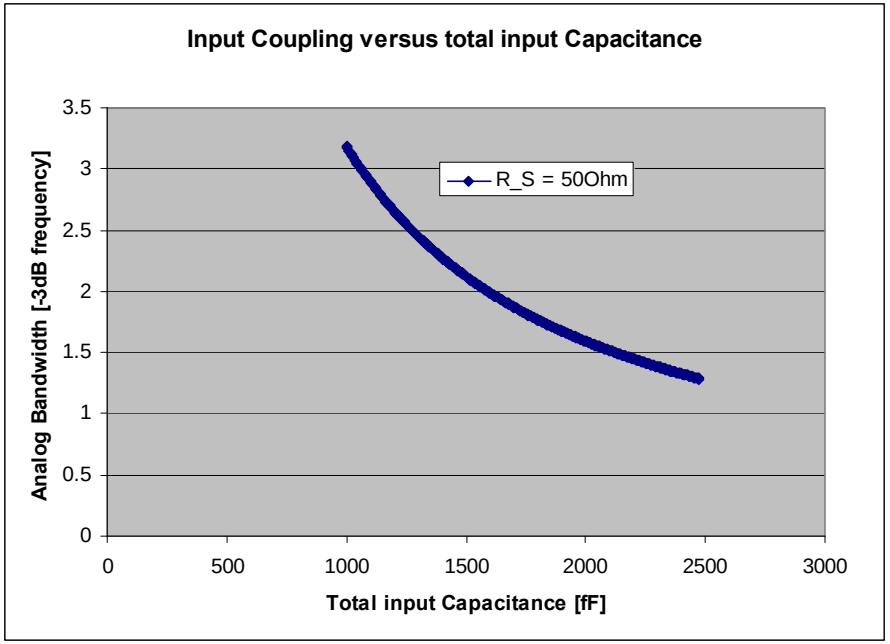
- Wilkinson (32x2): 64 conv/channel

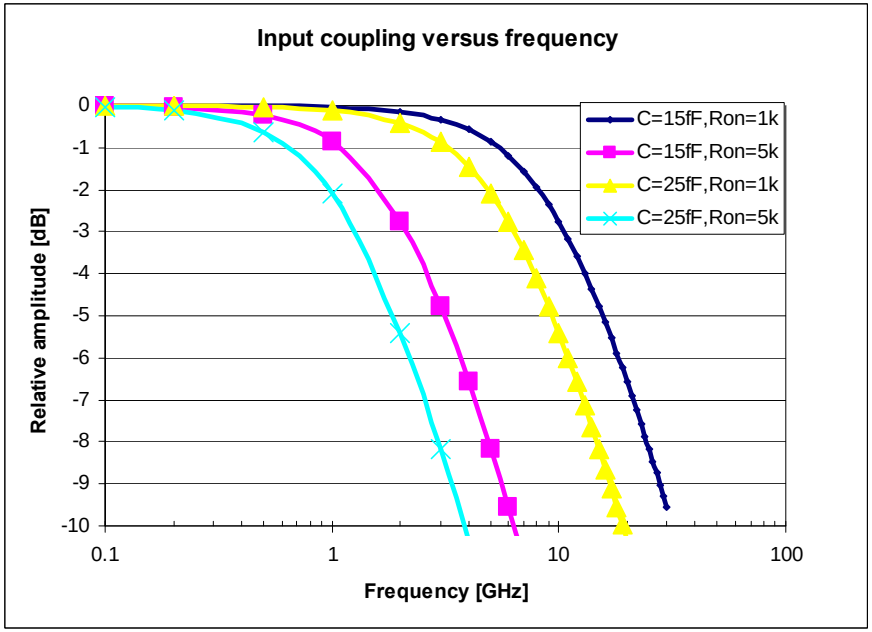
IRS (BLAB3 without amp) Input Coupling





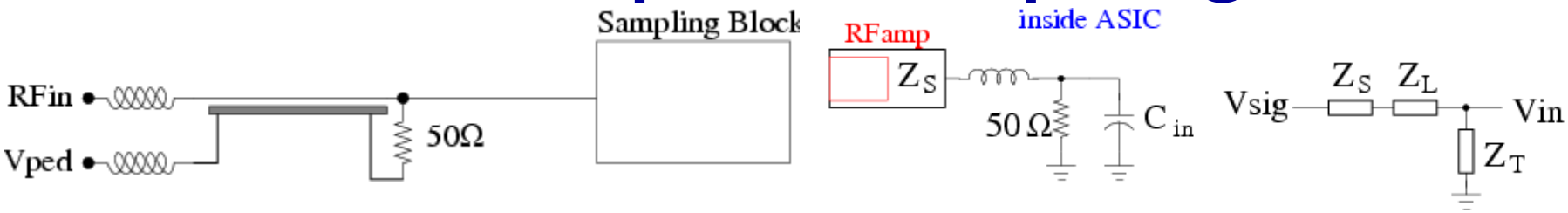


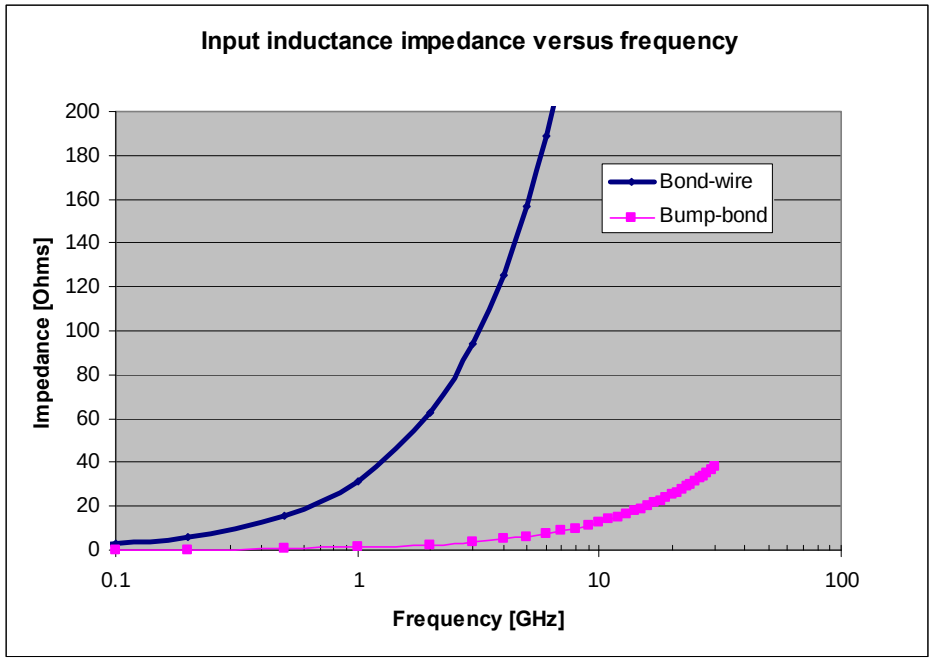


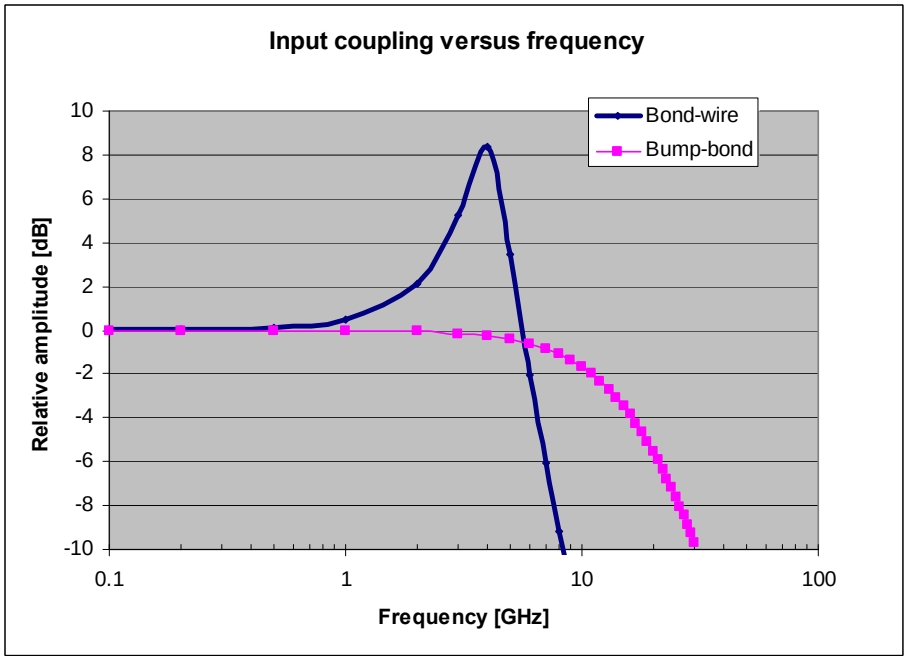


- Input bandwidth depends on 2x terms
  - $f3dB[input] = [2*\pi*Z*C_{tot}]^{-1}$
  - $f3dB[storage] = [2*\pi*R_{on}*C_{store}]^{-1}$

IRS Input Coupling

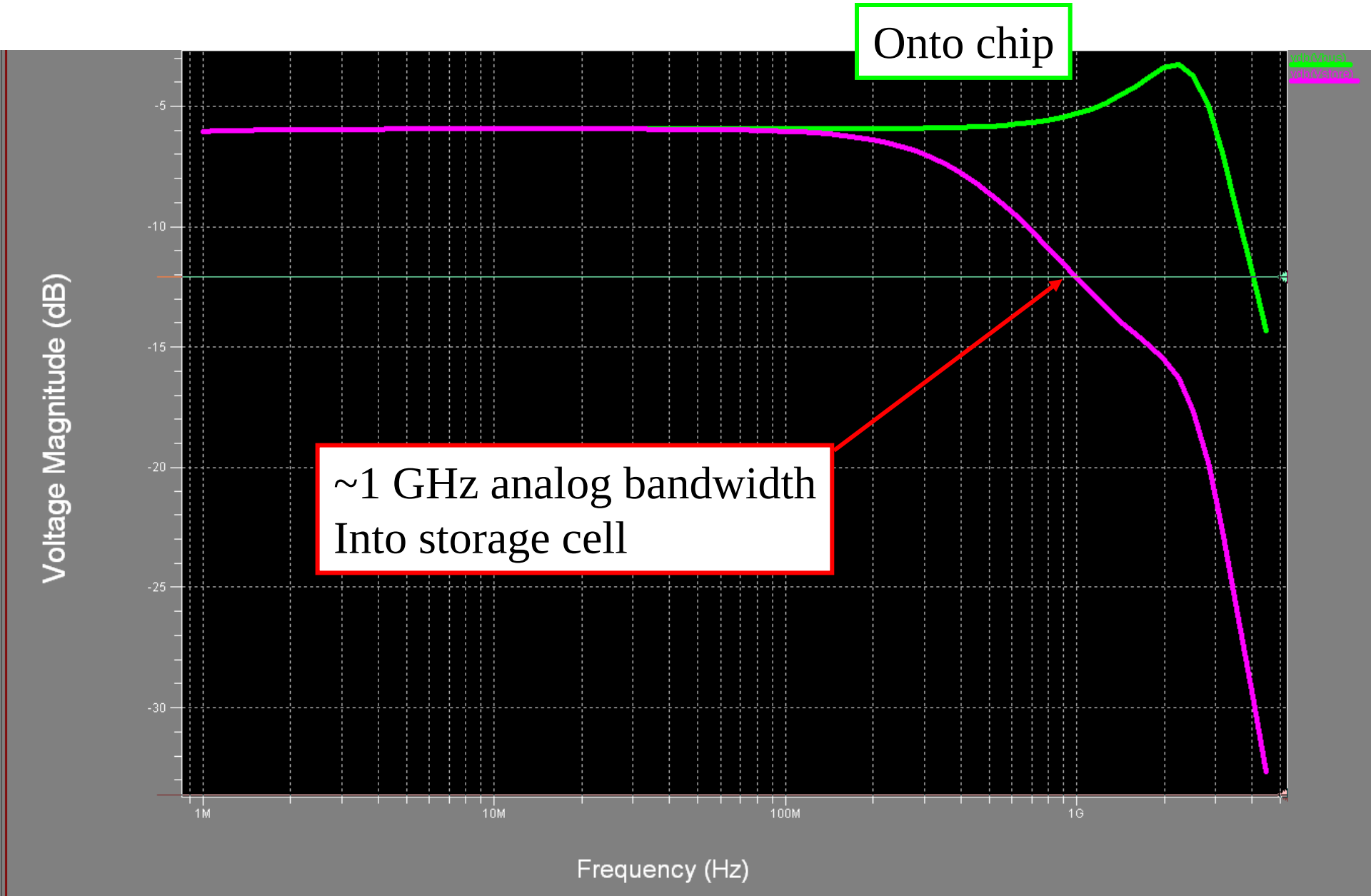




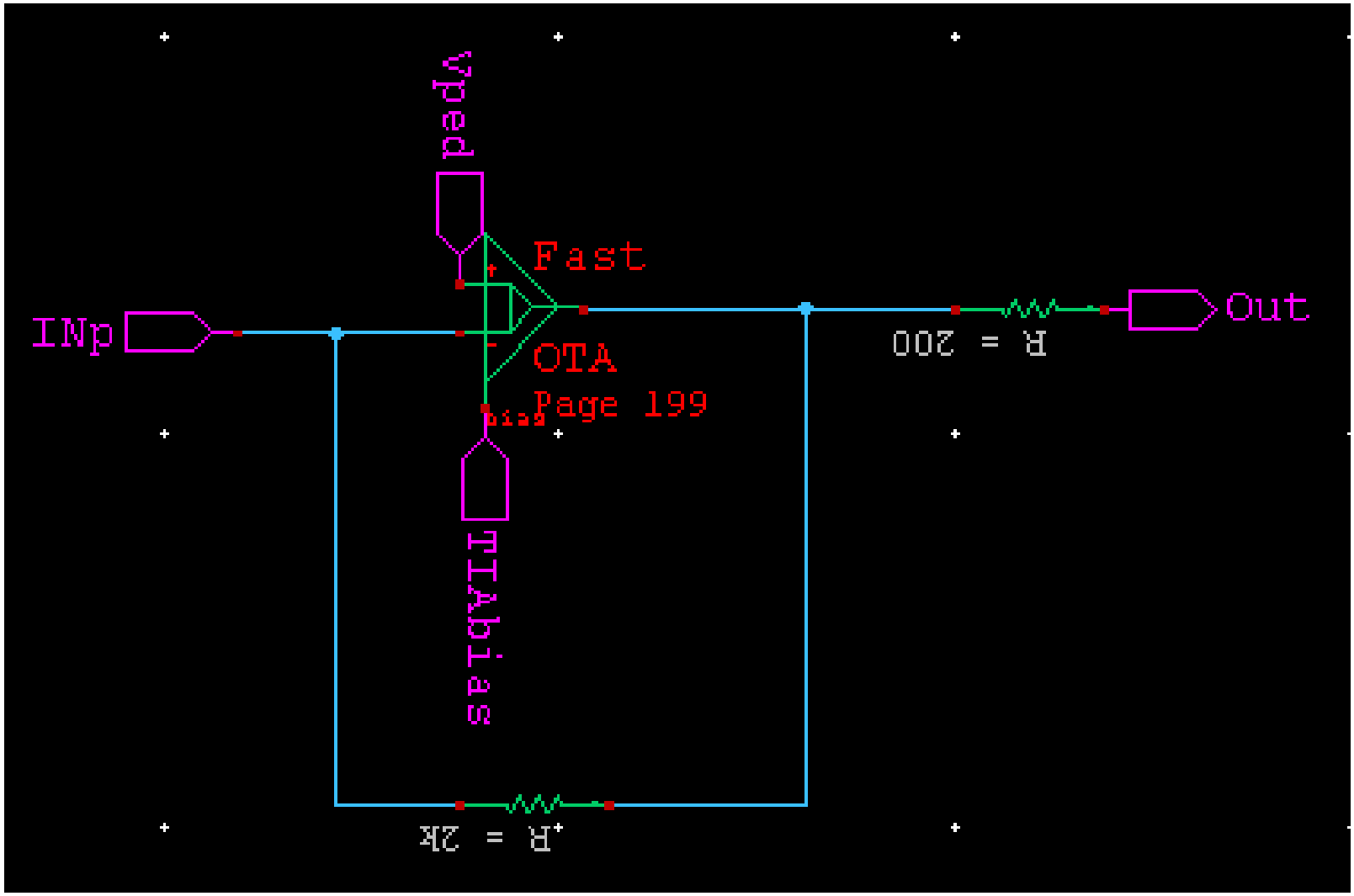


- Role of inductance

Input coupling sim (35fF sample)

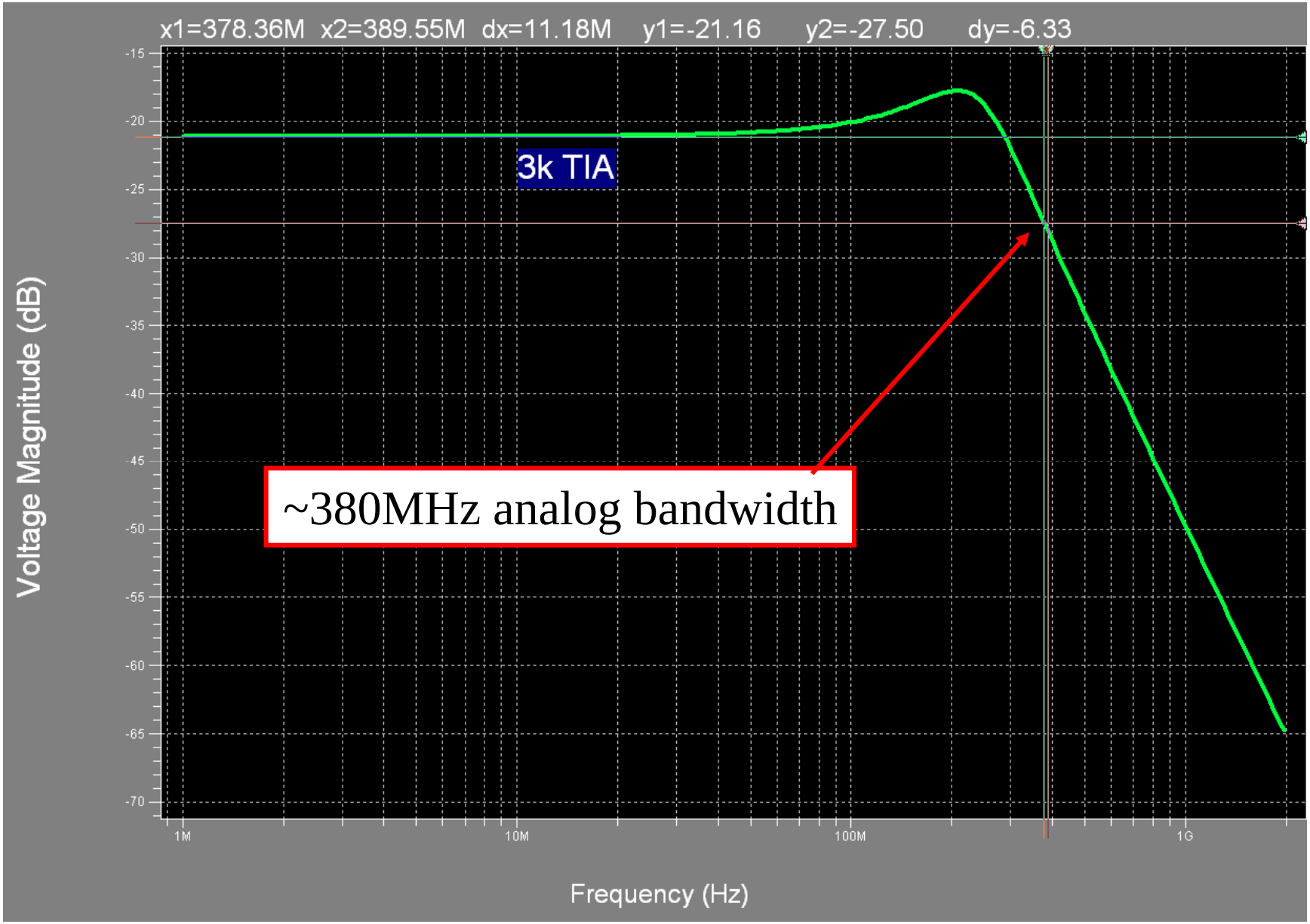


Trans-Impedance Amp



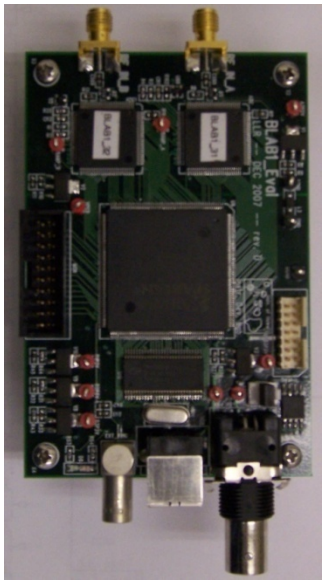
- Basic building block have used before

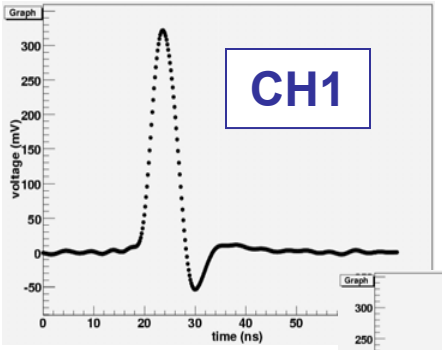
3kΩ TIA Sim

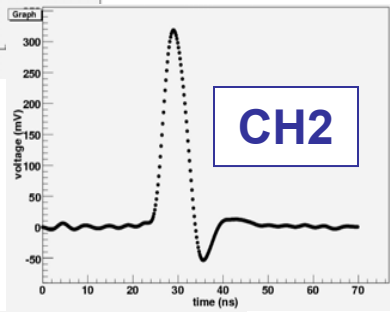

x1=378.36M x2=389.55M dx=11.18M y1=-21.16 y2=-27.50 dy=-6.33
3k TIA
~380MHz analog bandwidth
Voltage Magnitude (dB)
-15
-20
-25
-30
-35
-40
-45
-50
-55
-60
-65
-70
1M
10M
100M
1G
Frequency (Hz)

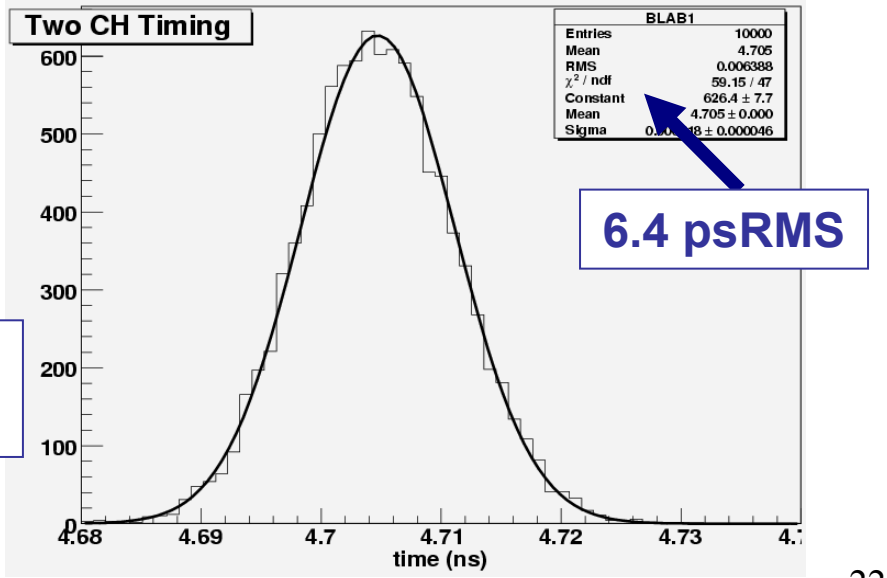
BLAB1 timing performance:

- Comparable performance to best CFD + HPTDC
- Using full samples significantly reduces the impact of noise
- Photodetector limited







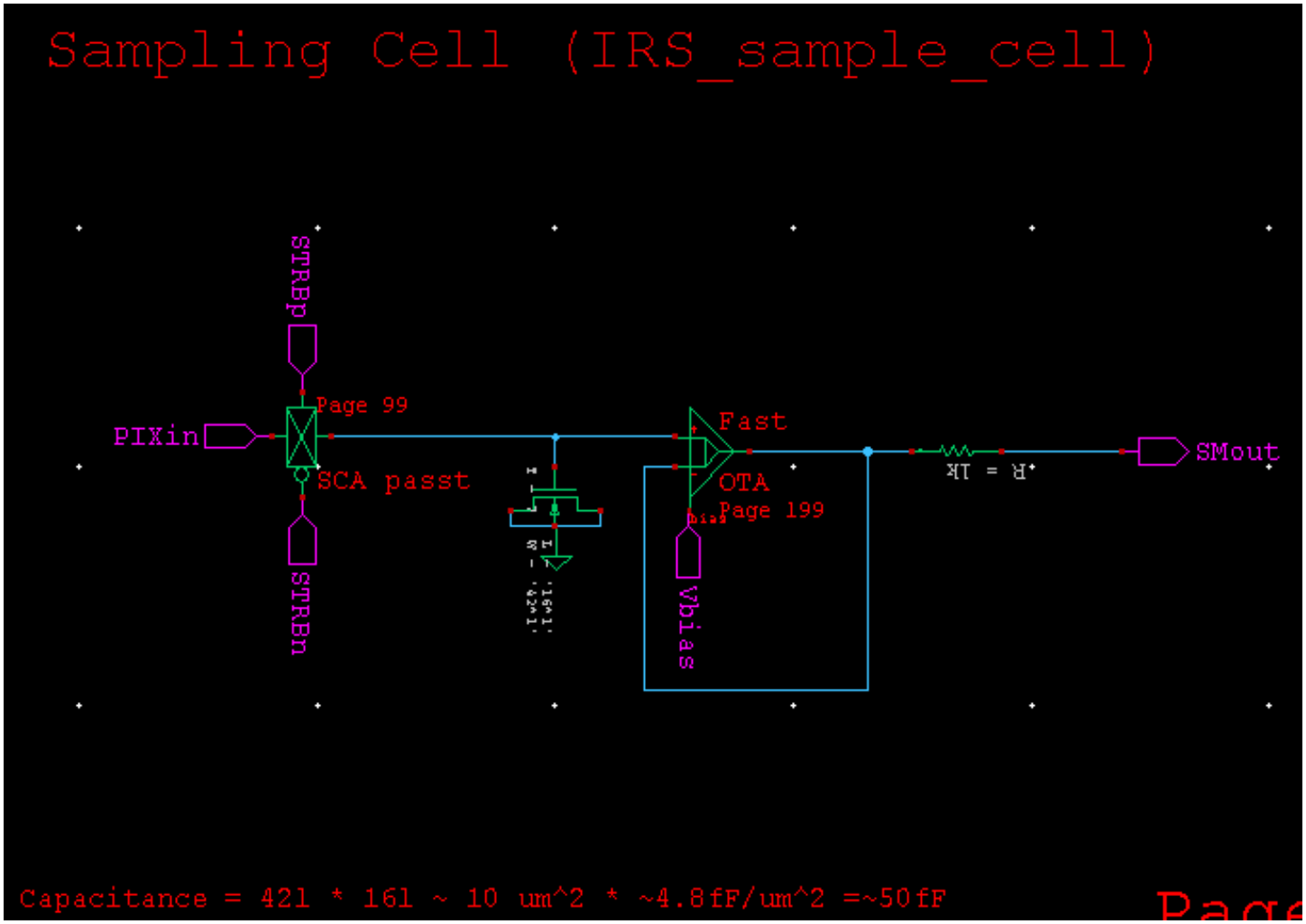


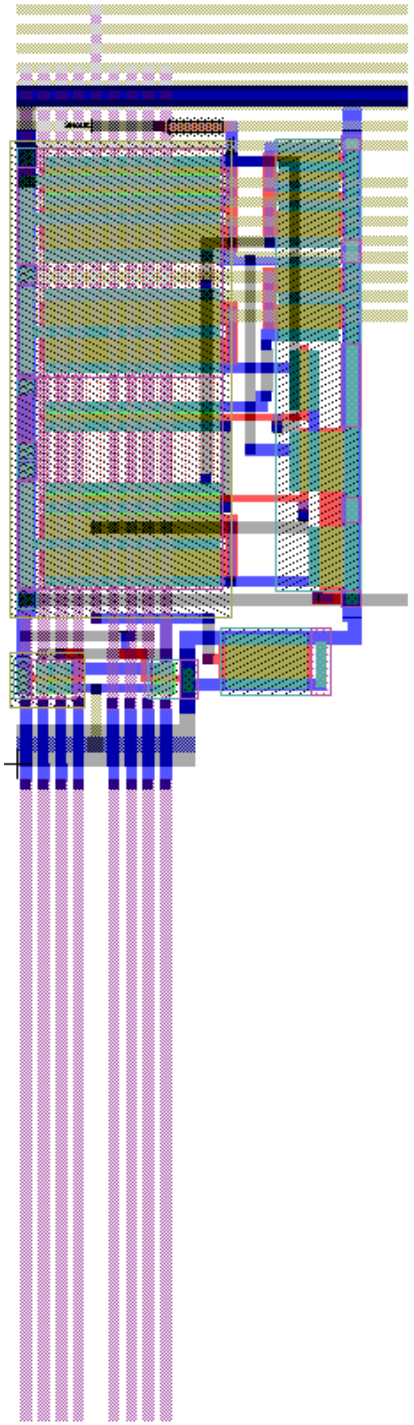
NIM A602 (2009) 438

~4.5 ps per single hit statistically

→ Only 300 MHz ABW

Sample Cell

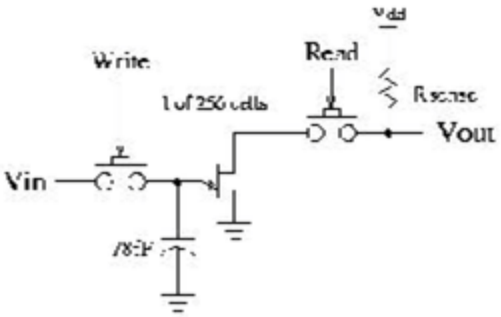




- Main element is buffer amp (OTA)
  - Relatively low current (10's uA) operation possible

Effect of too small a storage Cap

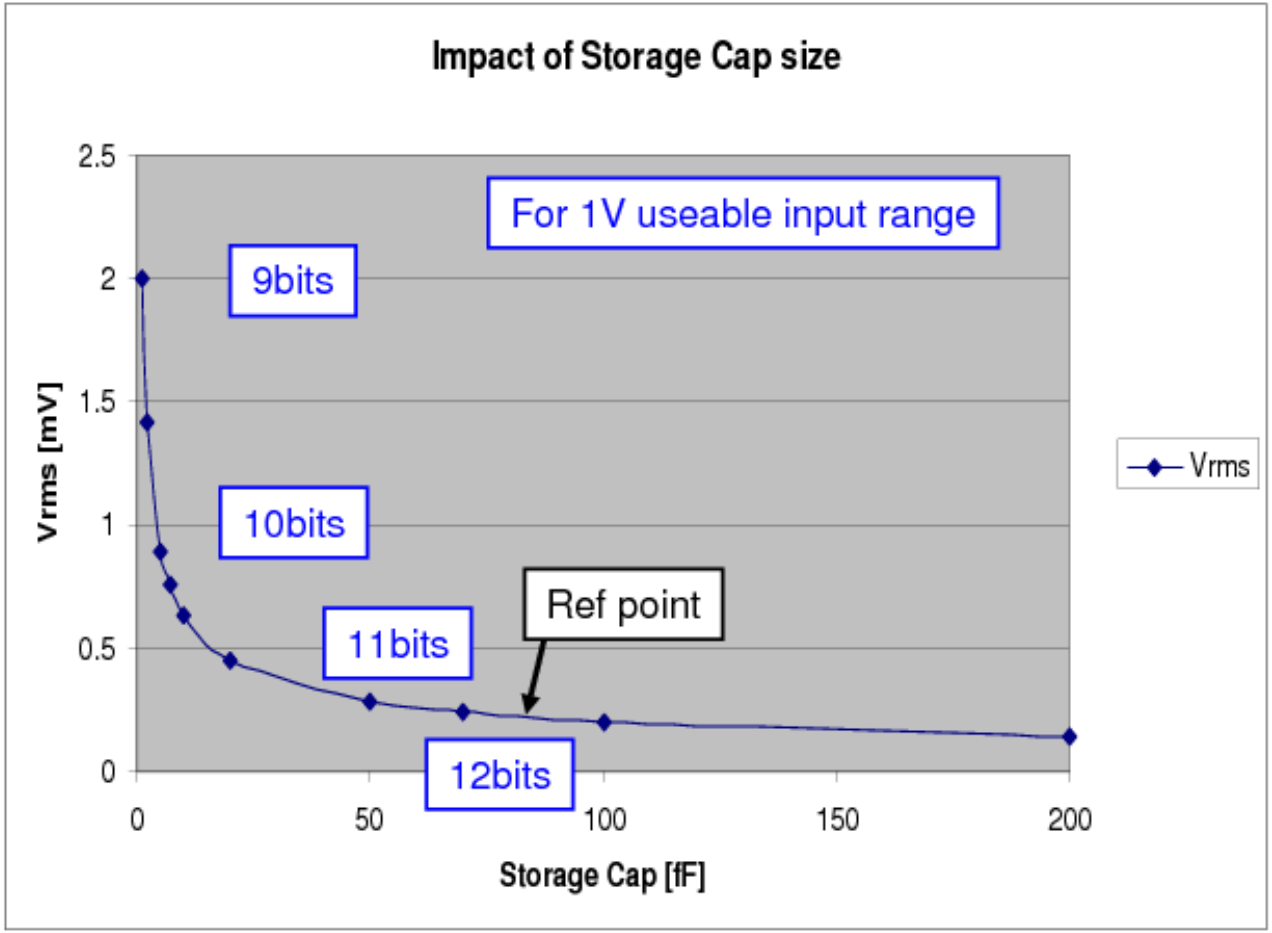
Desire small C for better Input Coupling



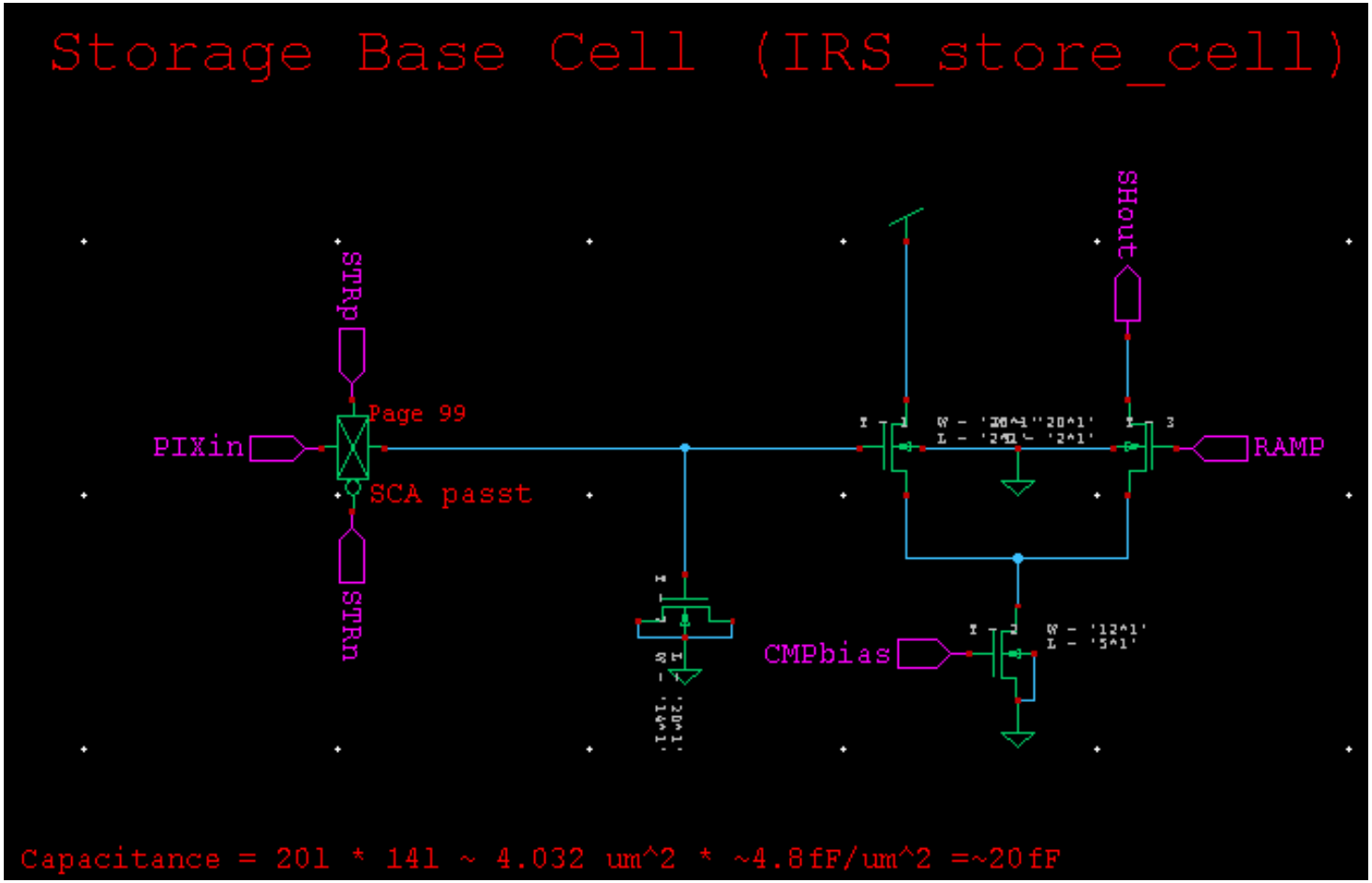
$$v_{rms} = \sqrt{\frac{kT}{C_{store}}} = 0.23mV$$

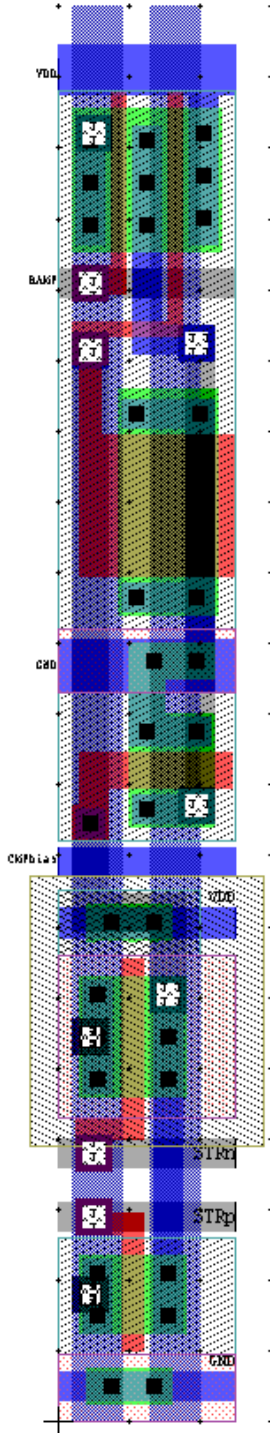
C_{store} = 78fF

Cstore = 35fF



Storage Cell



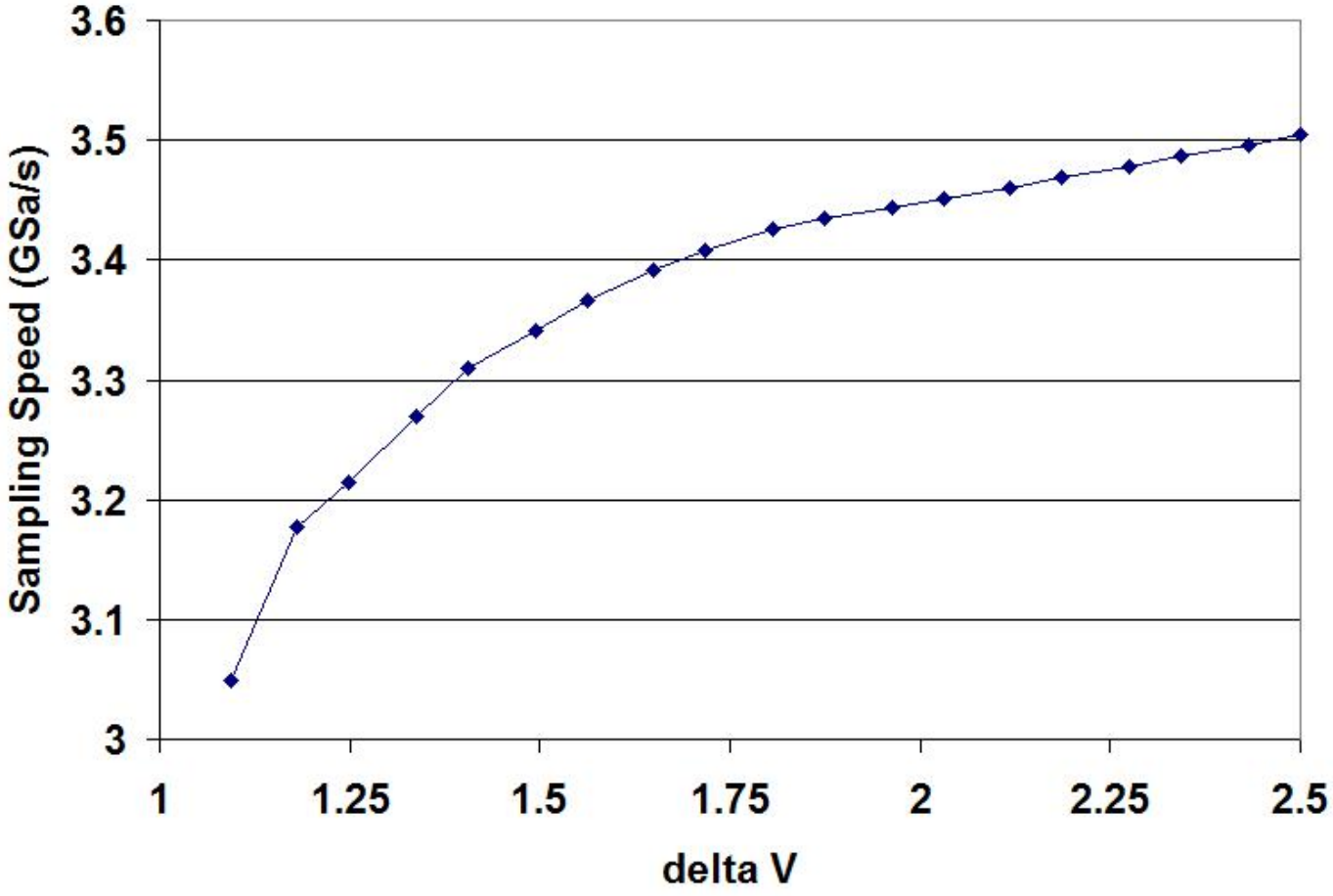


- Diff. Pair as comparator
  - Only power on selected block

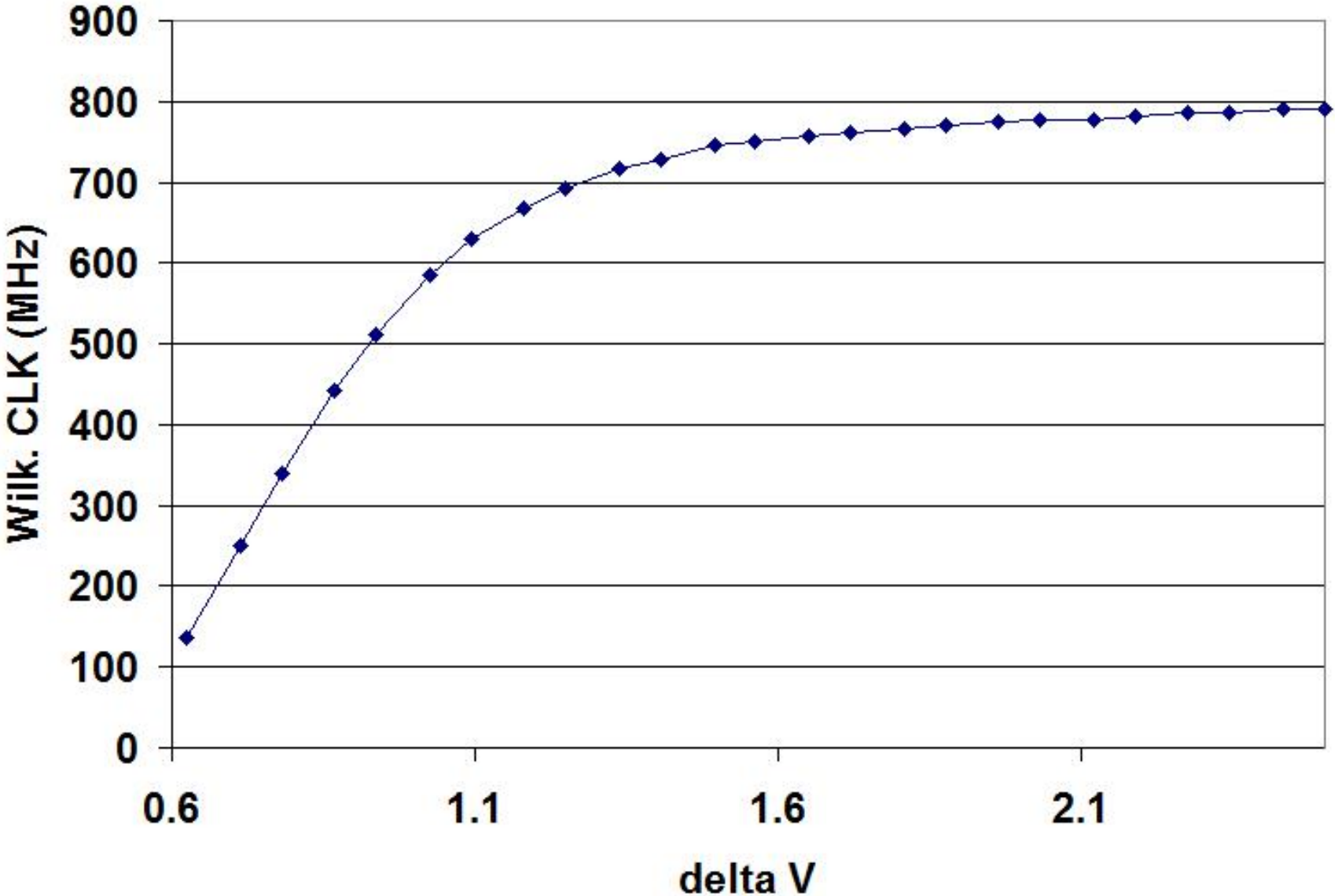
Evaluation Board

BLAB3: Sampling Speed

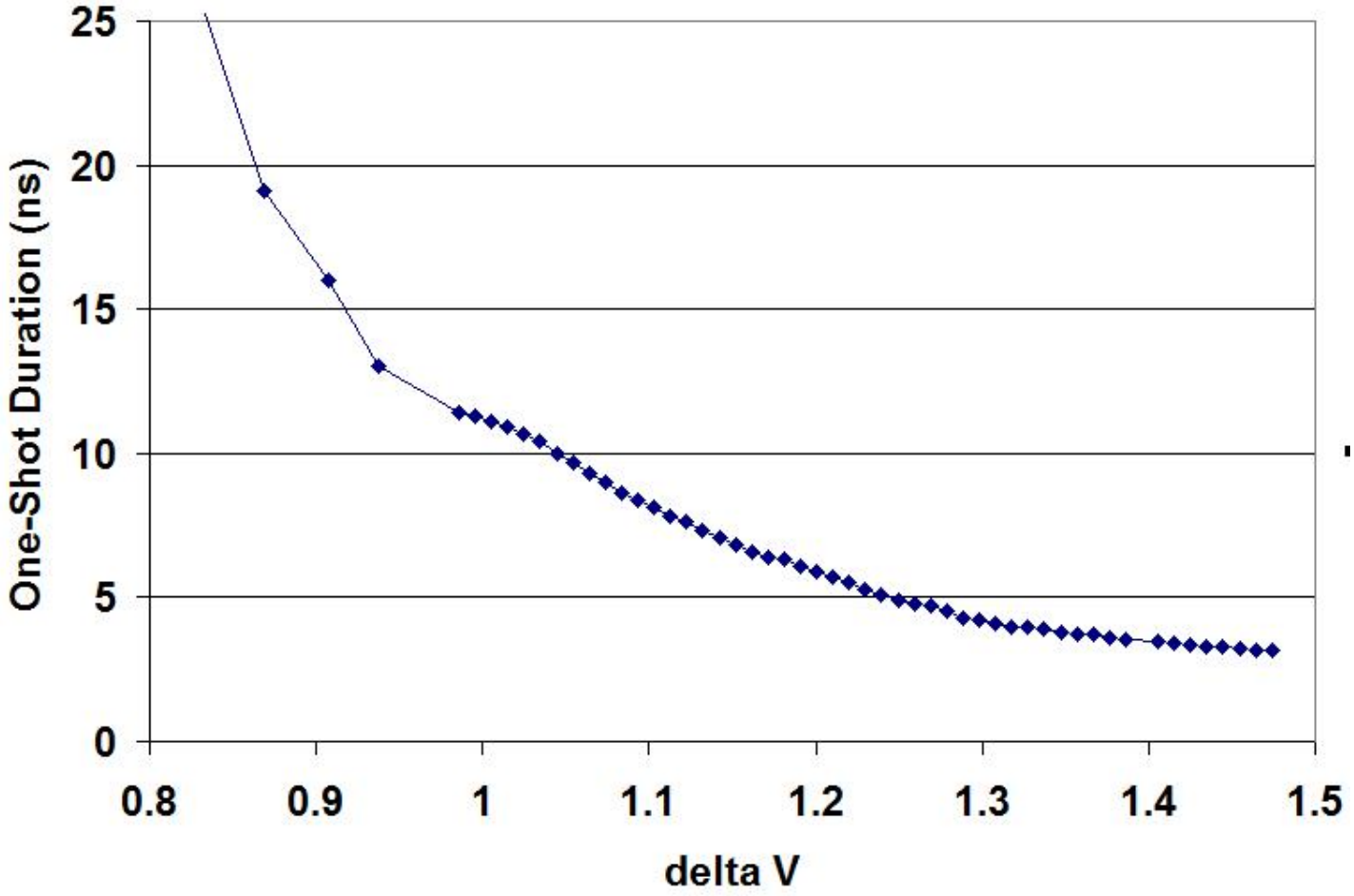
- Simulation shows that we should get up to 4.4 GSa/s
- Right now, not accounting for insertion delays in/out of ASIC



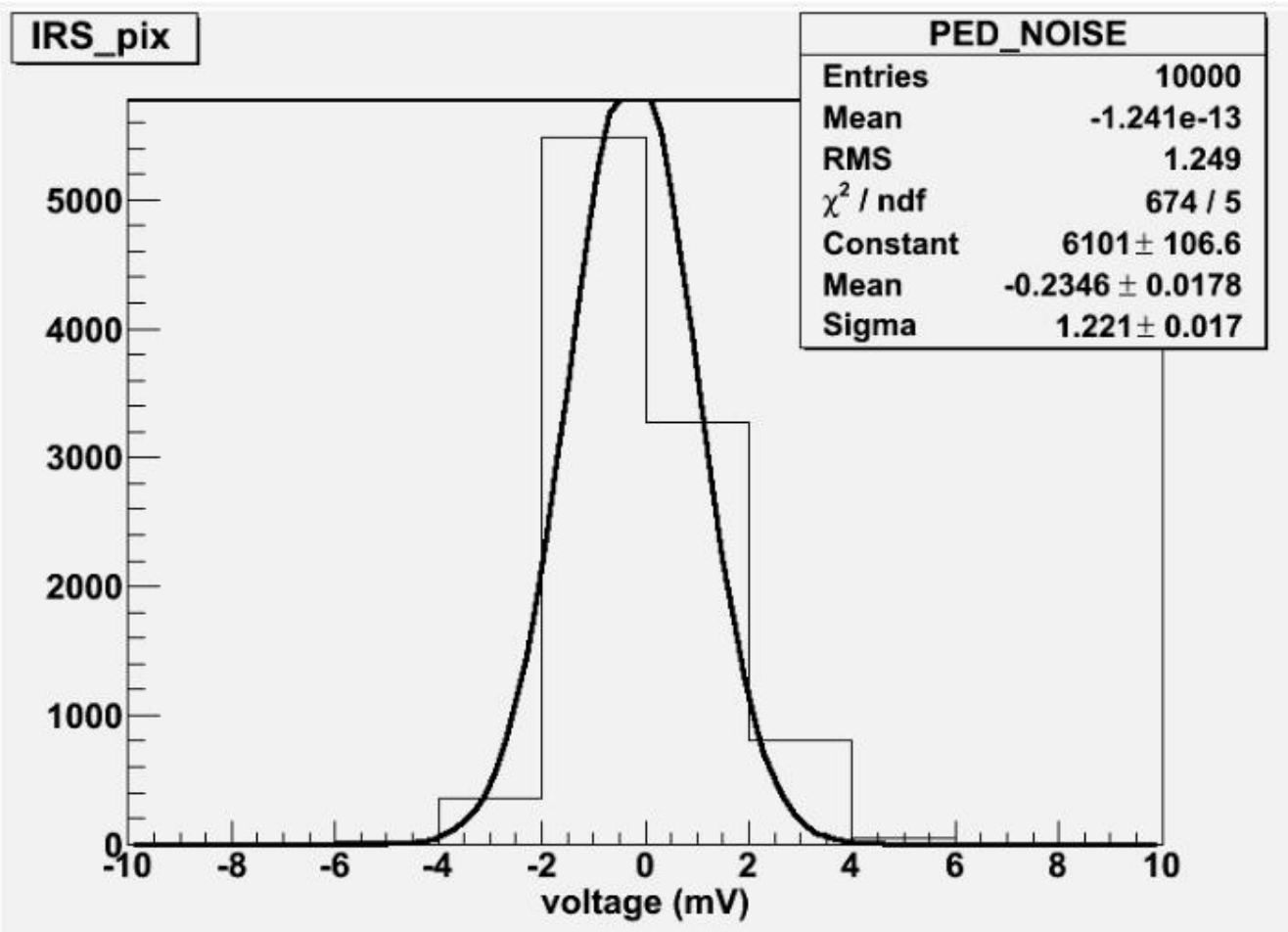
BLAB3 Wilk. Clock Speed



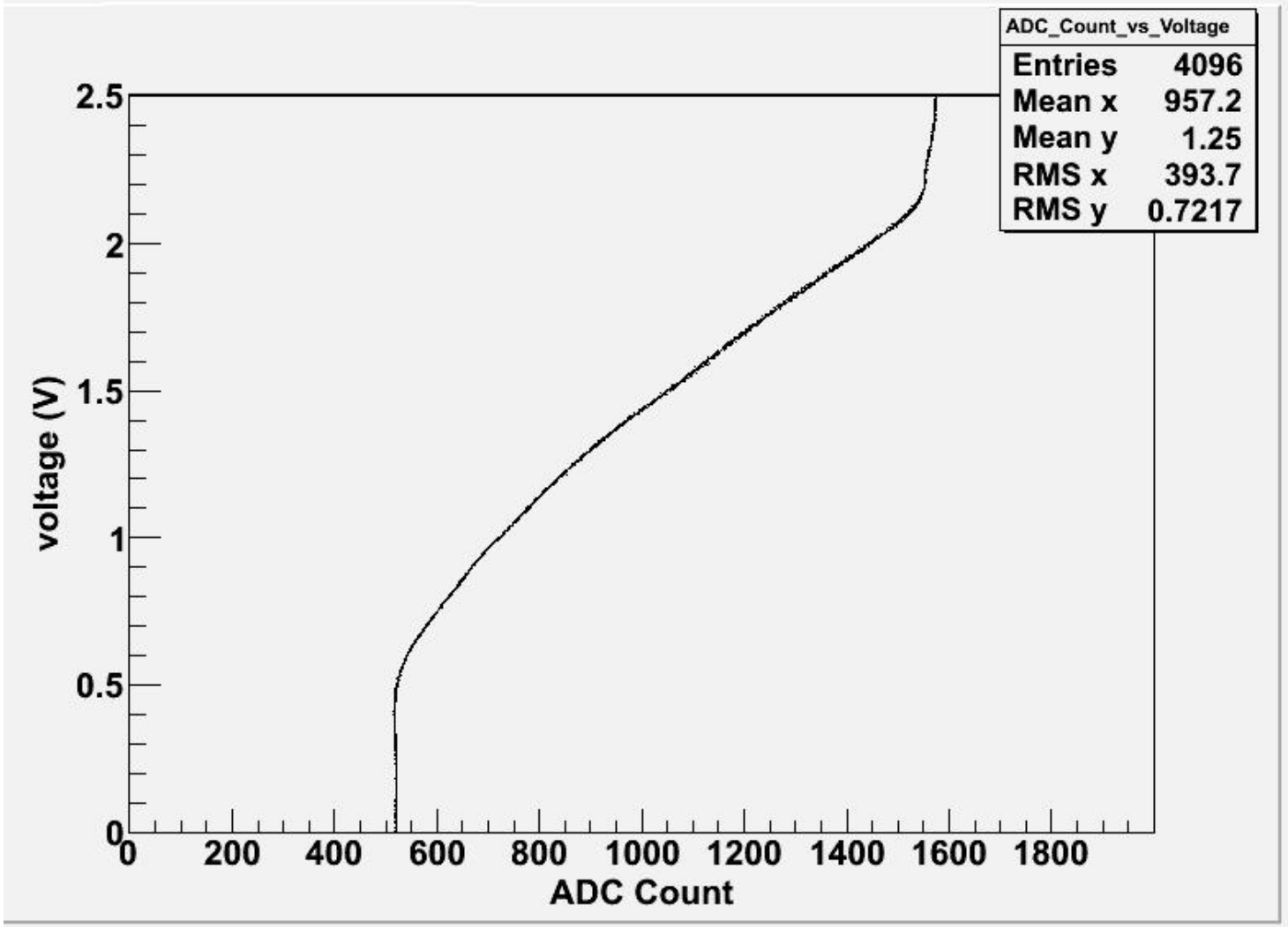
Internal One-Shot Triggering



BLAB3: Digitize Noise (w/ AMPs turned off)



Working on Calibrating Wilk. Cell variations



BLAB3: Future plans

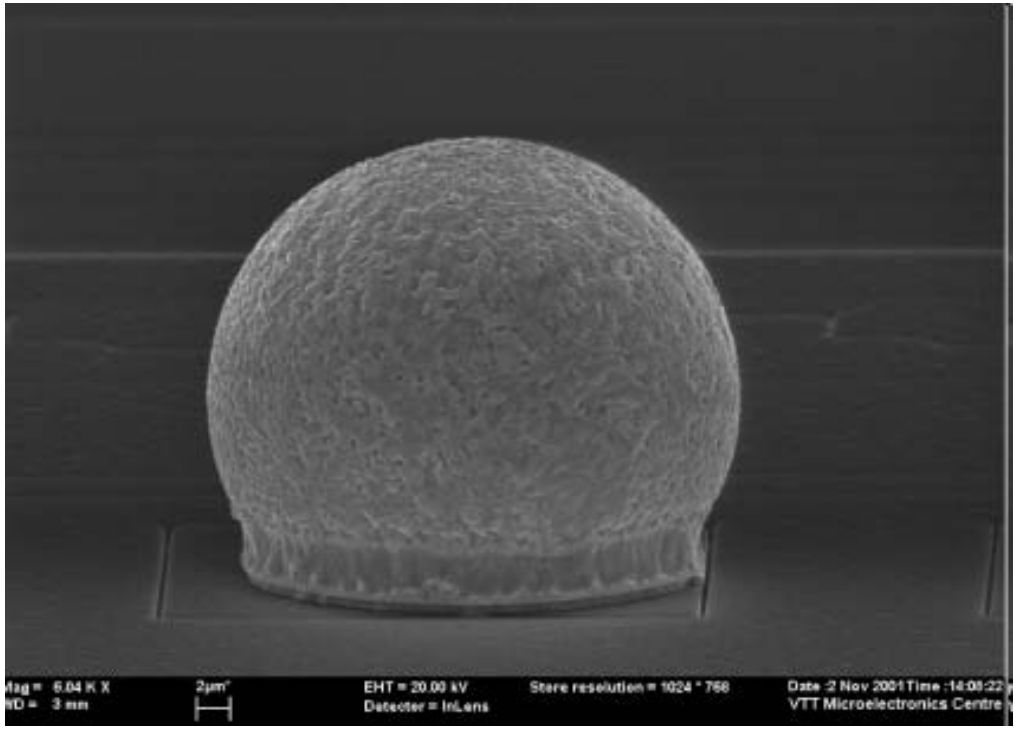
- Measurements that we are planning on making:
  - Frequency response
  - Timing variation between sampling cells
  - Timing jitter between two channels

Other test capabilities, system experience in later talk

Backup Slides

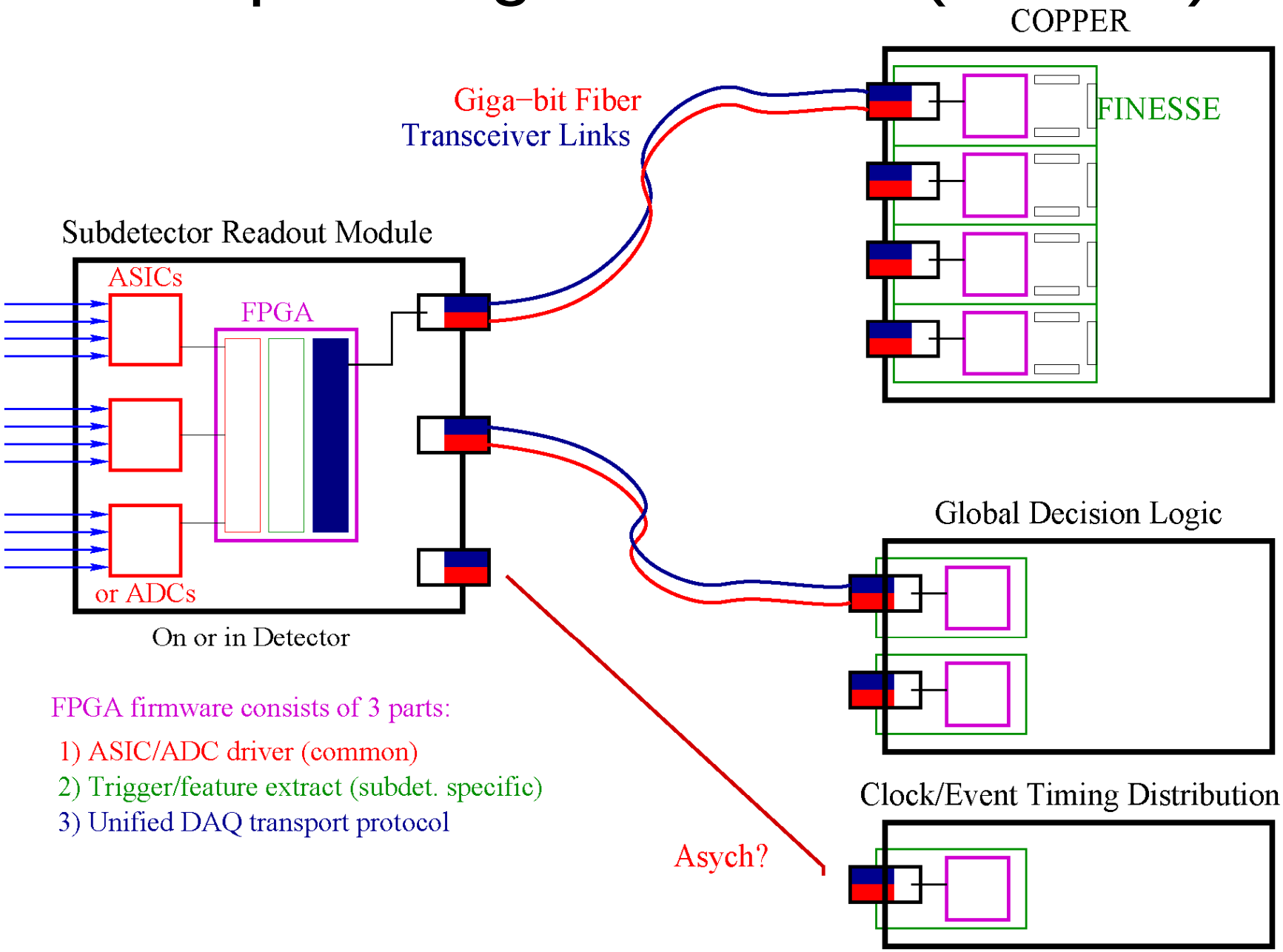
Flip Chip (Stud bonding)

- CVInc has agreed to do the stud bonding on to our PCB
- Lots of European vendors
- Very few USA vendors



CVInc

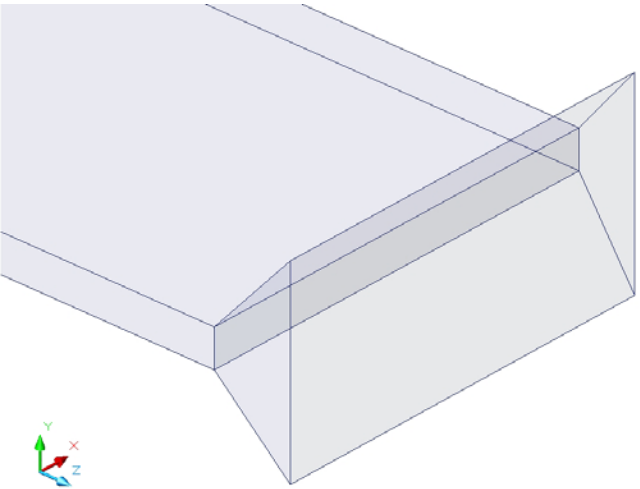
Example Large Readout (Belle II)

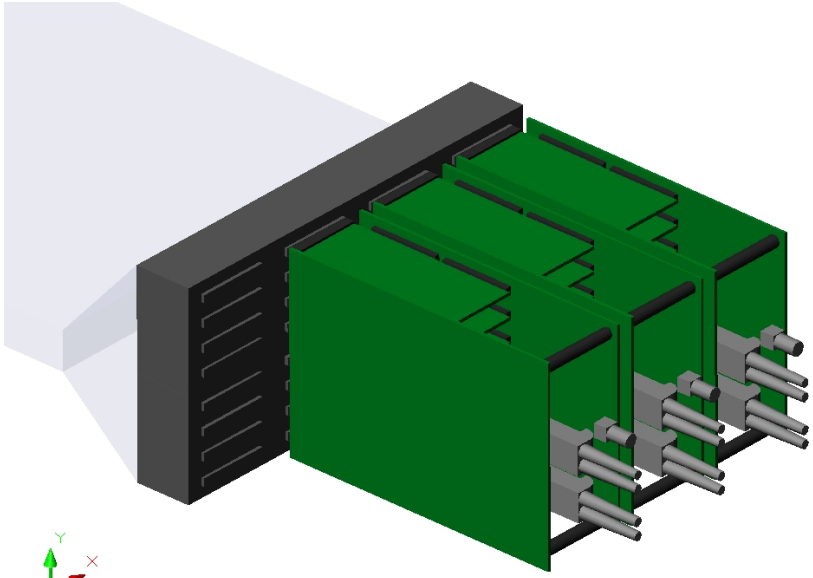


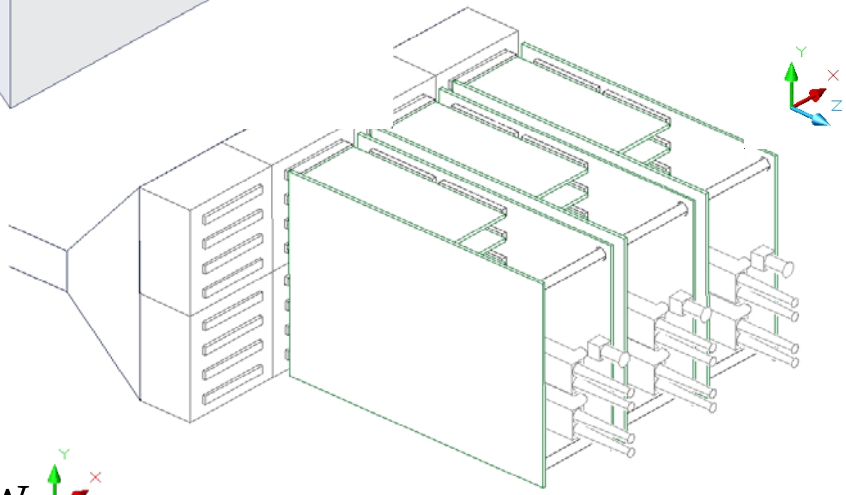
FPGA firmware consists of 3 parts:

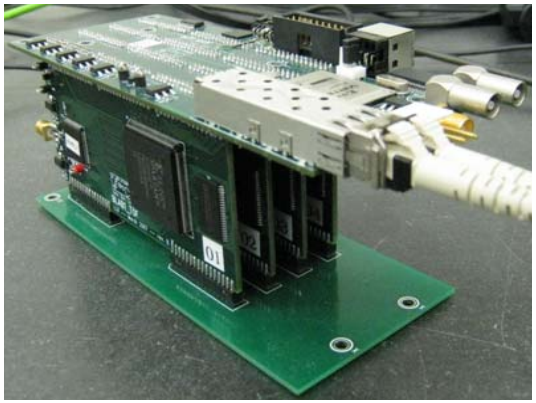
1) ASIC/ADC driver (common)
2) Trigger/feature extract (subdet. specific)
3) Unified DAQ transport protocol

Baseline image block

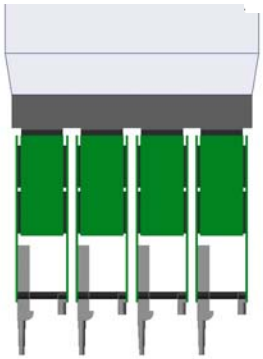






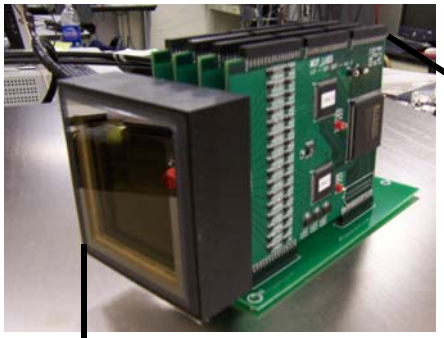


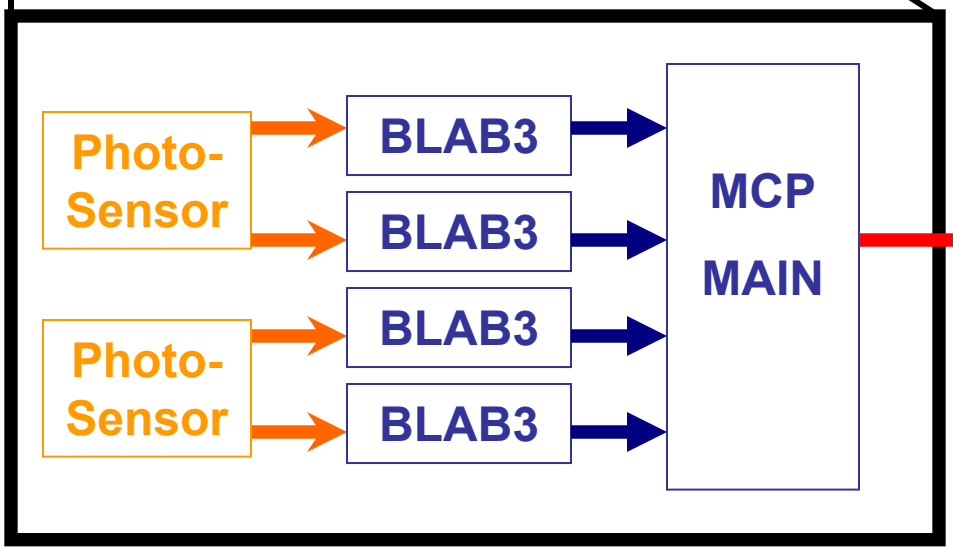
Top View

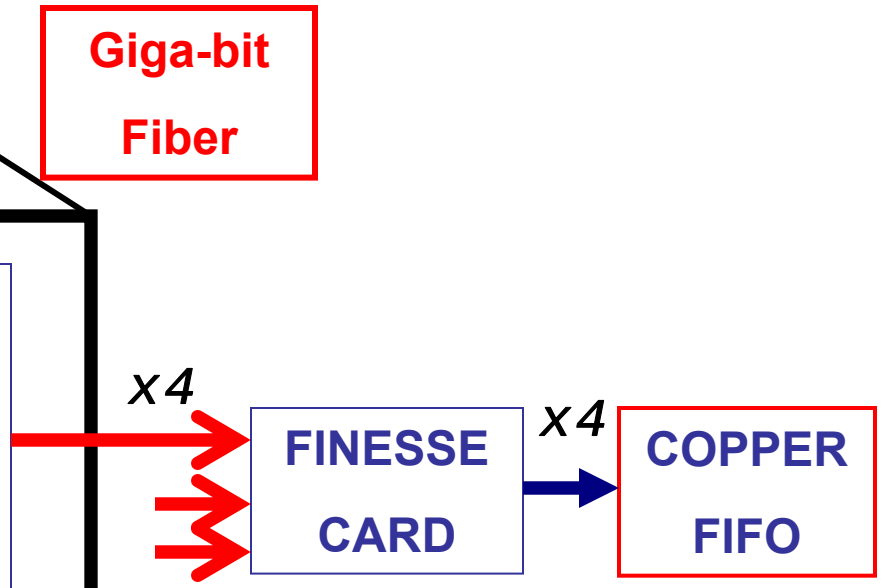


2x 64-channel PMTs per fiber link
7x BLAB3 daughtercards (112x BLAB3)
896 PMT channels/module (16 iTOP staves)
7 data, 7 trigger fiber pairs + HV power, LVDS
RF clock, Revolution marker pairs

Baseline System Components







- BLAB3 is 8 channels, each 32k samples deep
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Total channel numbers presented previously unchanged, partitioned slightly differently

Experiment 2: 13-Mar-09 – (~9 mo.)

- 448 channels readout at SLAC + few hundred UH [HI-TIDE]
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Experiment 3: winter – (~6+ mo.)

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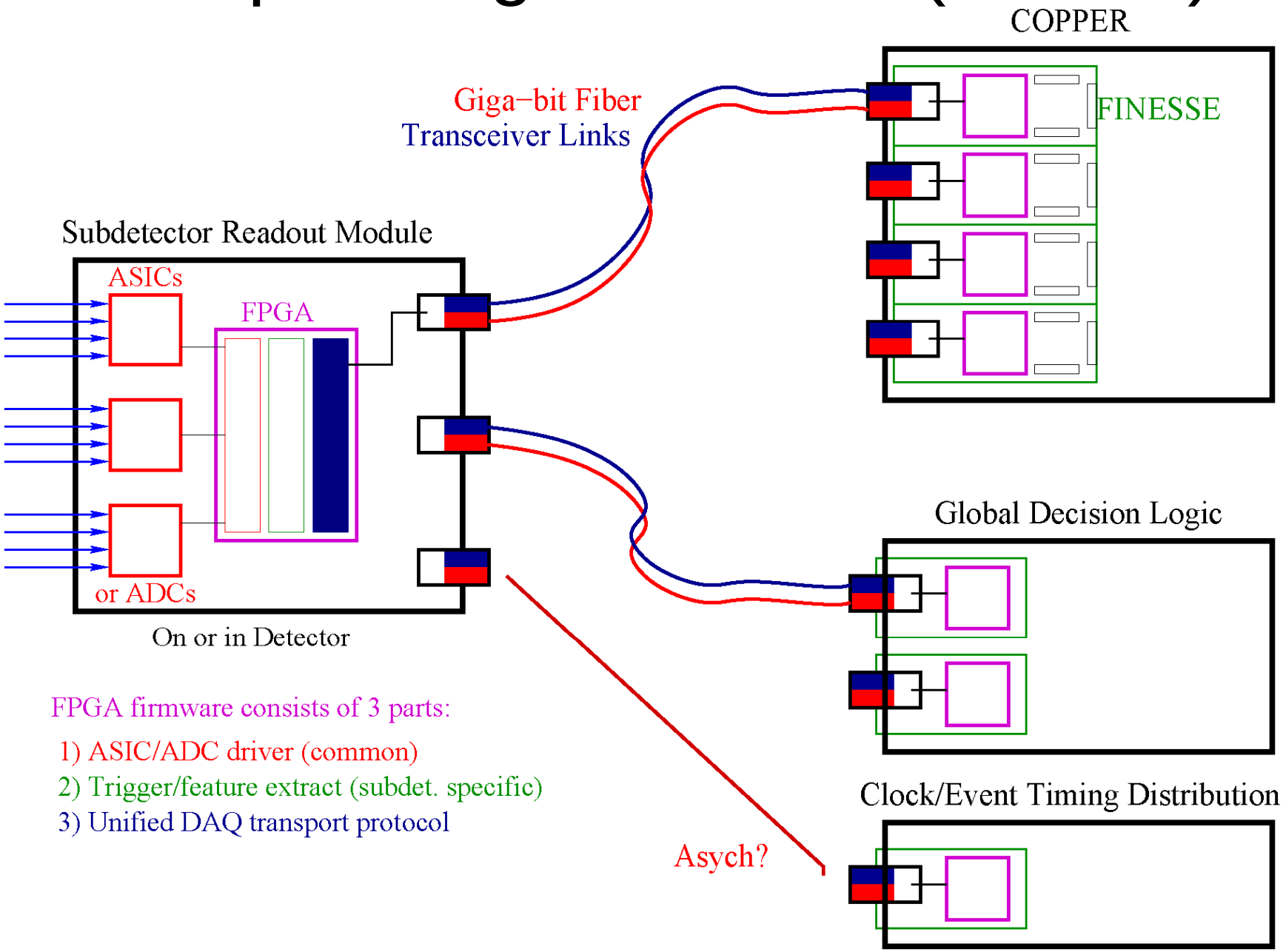
- At speed fast feature extraction

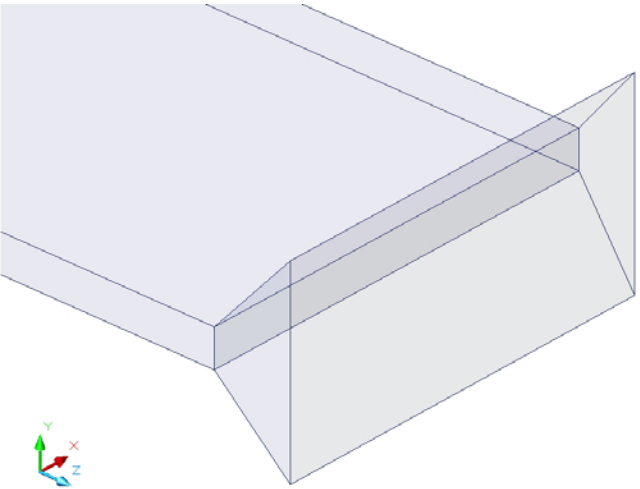
Example Large Readout (Belle II)

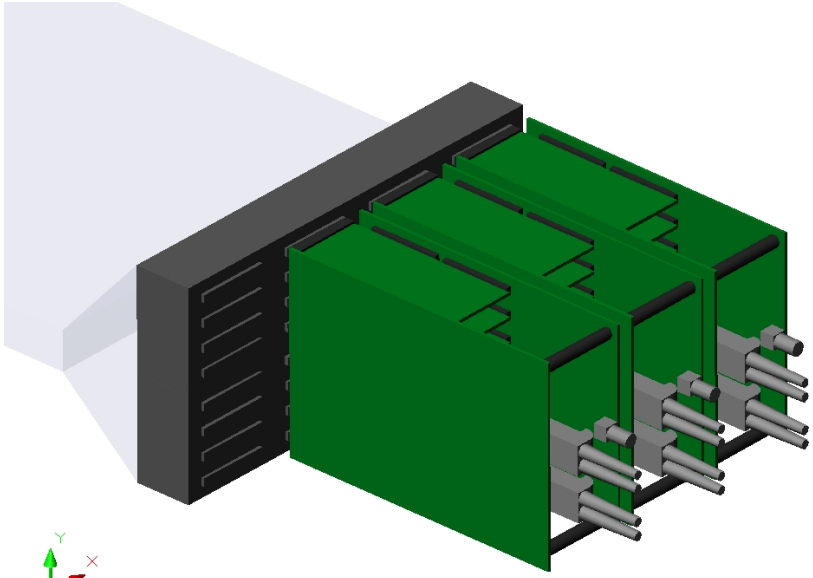


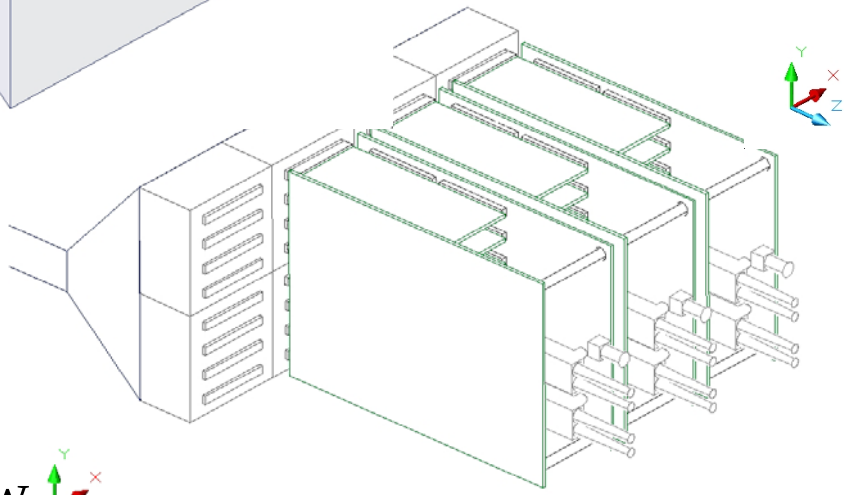
FPGA firmware consists of 3 parts:

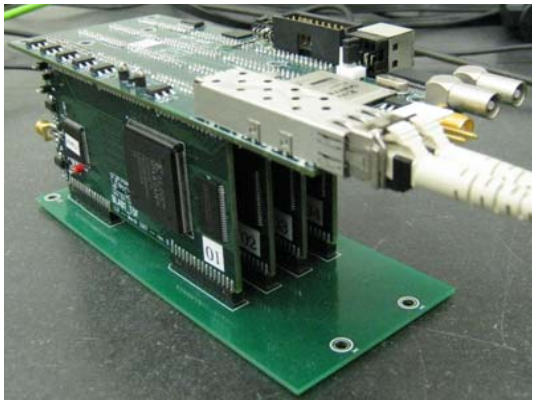
1) ASIC/ADC driver (common)
2) Trigger/feature extract (subdet. specific)
3) Unified DAQ transport protocol

Baseline image block









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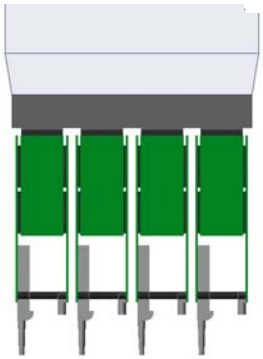

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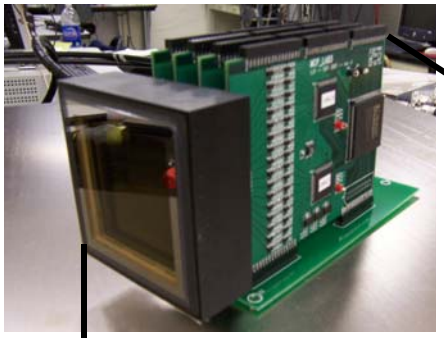

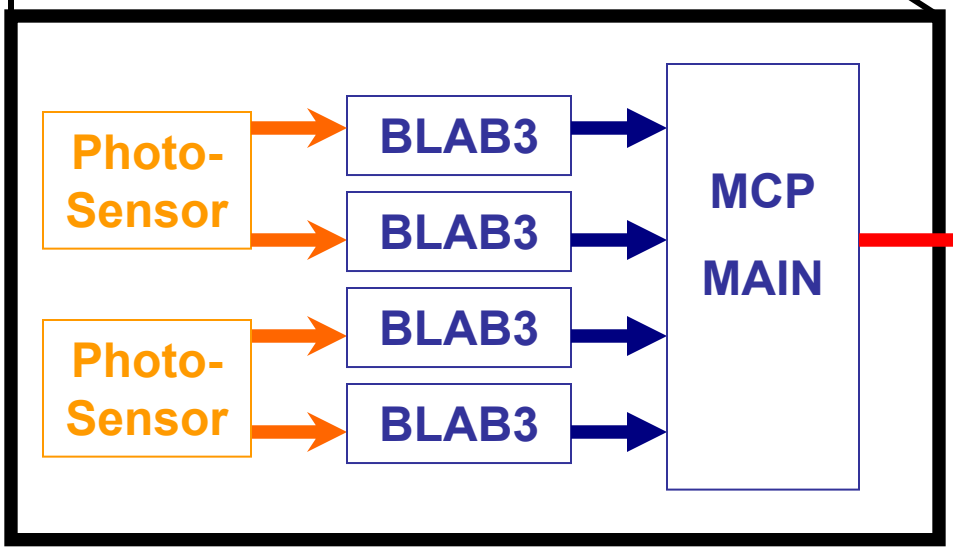

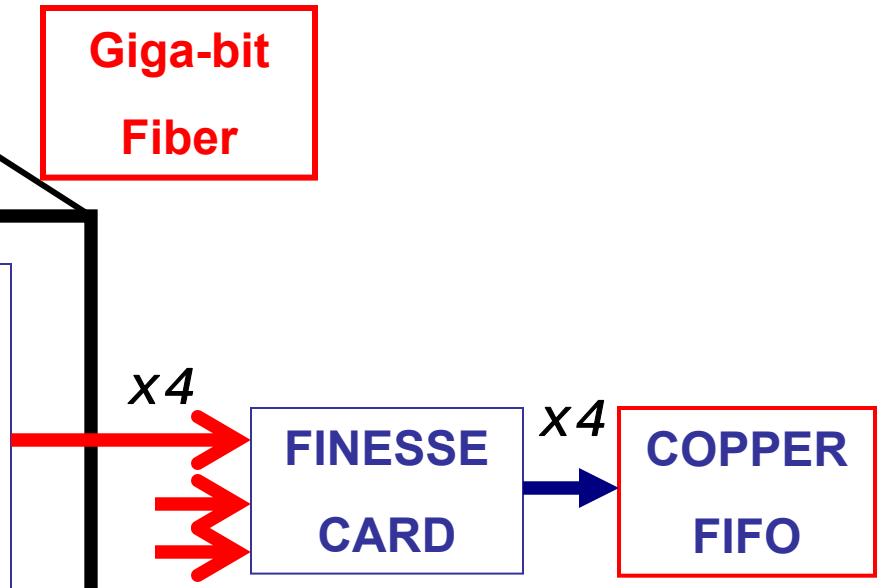

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