Hawaii (synergistic) Activities

- Experience from the fDIRC prototype
- A sample system – fiber optic based
- DSP Feature extraction
- Test facilities/ alternative ASICs/ readout

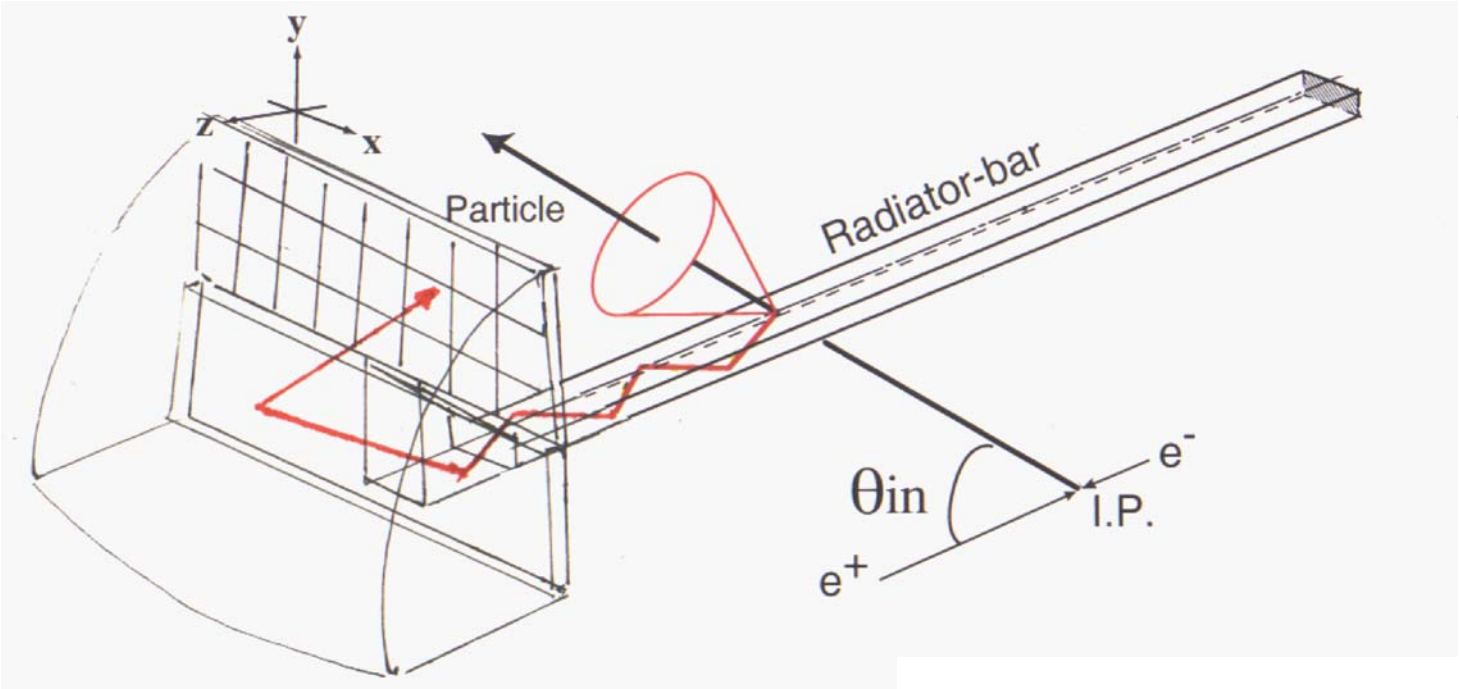
Juaquin Anderson
Matt Andrew
Tom Browder
Michael Cooney
Xin Gao
James Kennedy
Luca Macchiarulo
Kurtis Nishimura
Louis Ridley
Jamal Rorie
Larry Ruckman
Gary Varner

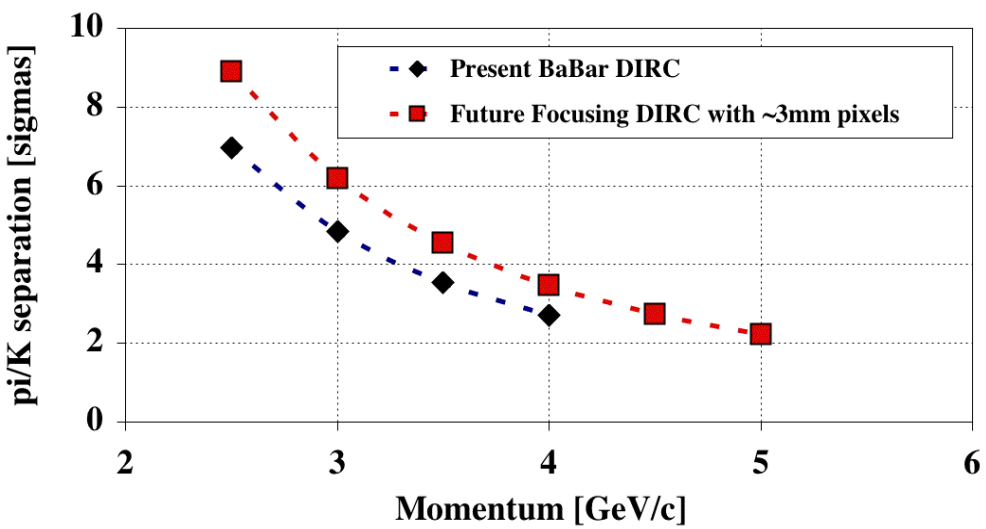
25-FEB-2010 LAPPD Meeting

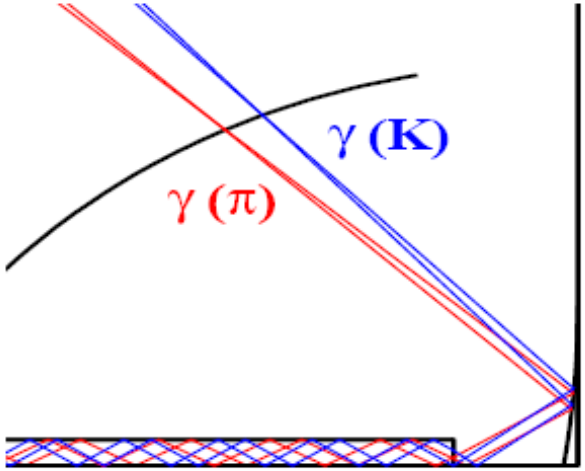
In addition to ASIC designs/ evaluation:

- System issues
- How to readout a large number of channels
- Timing and flow control
- Fast feature extraction (T,Q)
- Self-calibration (timing alignment) & overall calibration issues
- ps Xray source at UH

Fast Focusing DIRC Concept

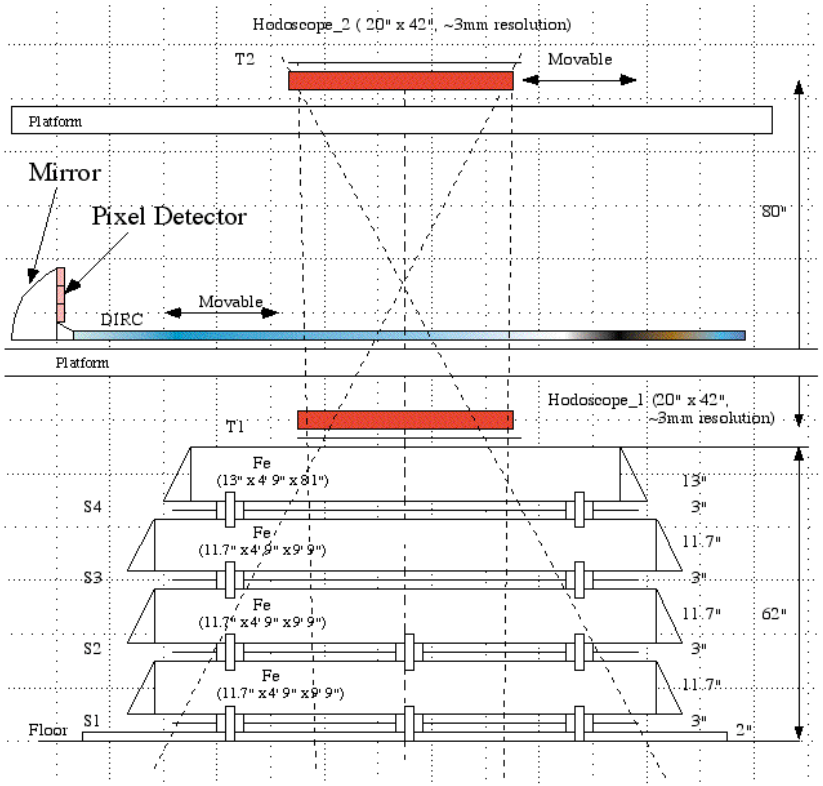






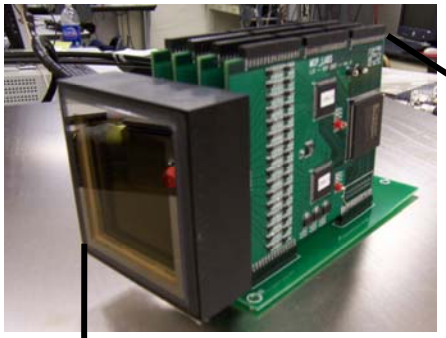
fDIRC: SLAC Cosmic Muon Telescope

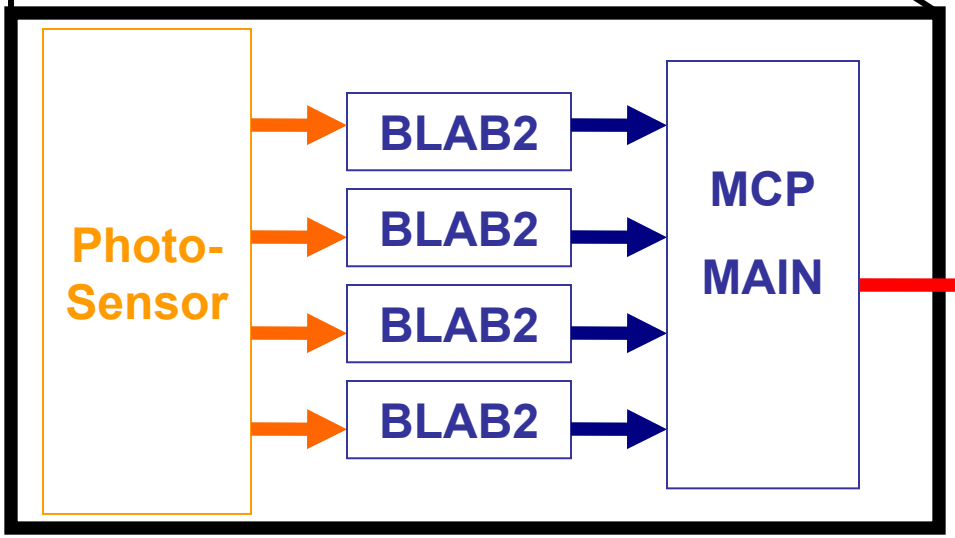
- Nice cosmic stand
  - 1 mrad resolution
  - Precision timing and further studies w/ new electronics
- Installed BLAB2-based readout in Jan. 2009
  - A year of experience operating



~1.5 GeV E_min through range stack

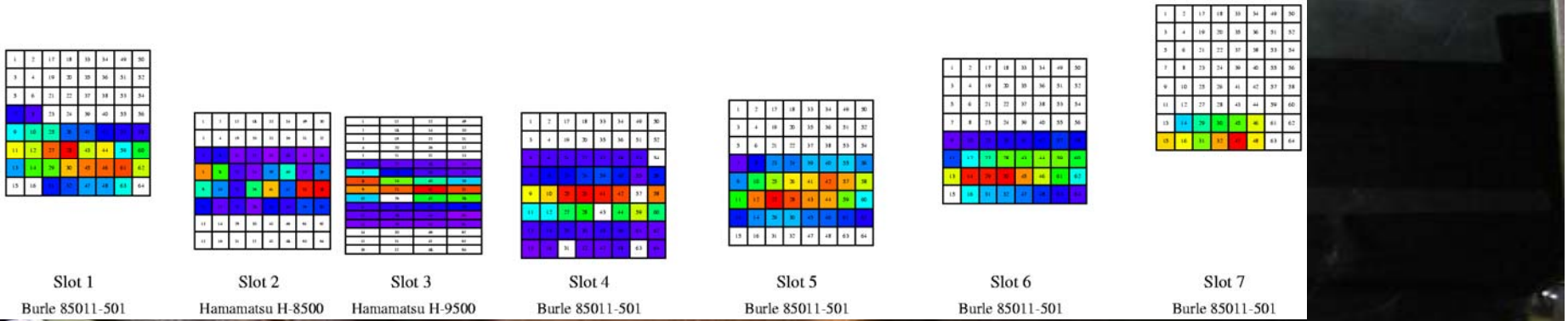
Readout System Components

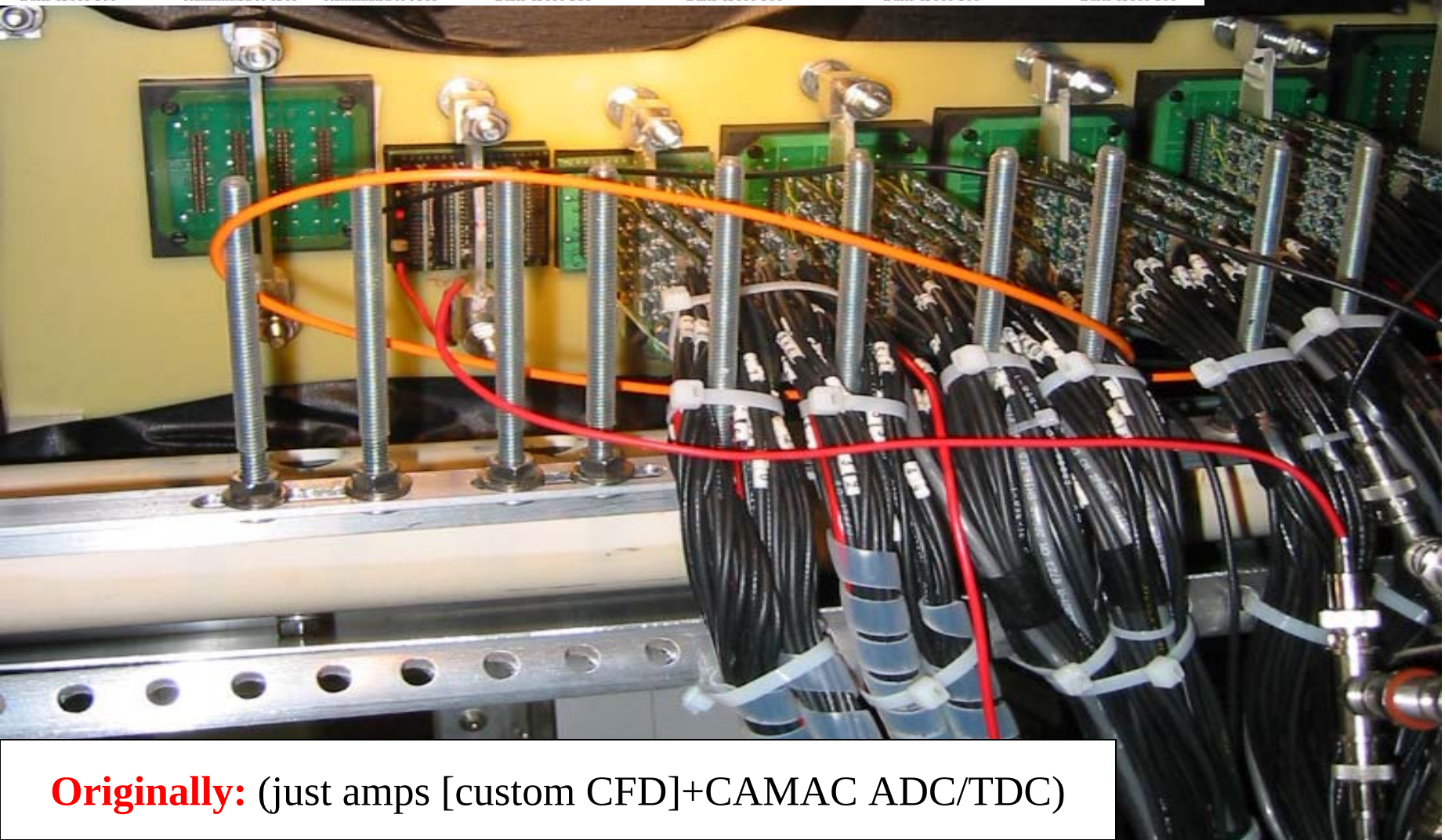




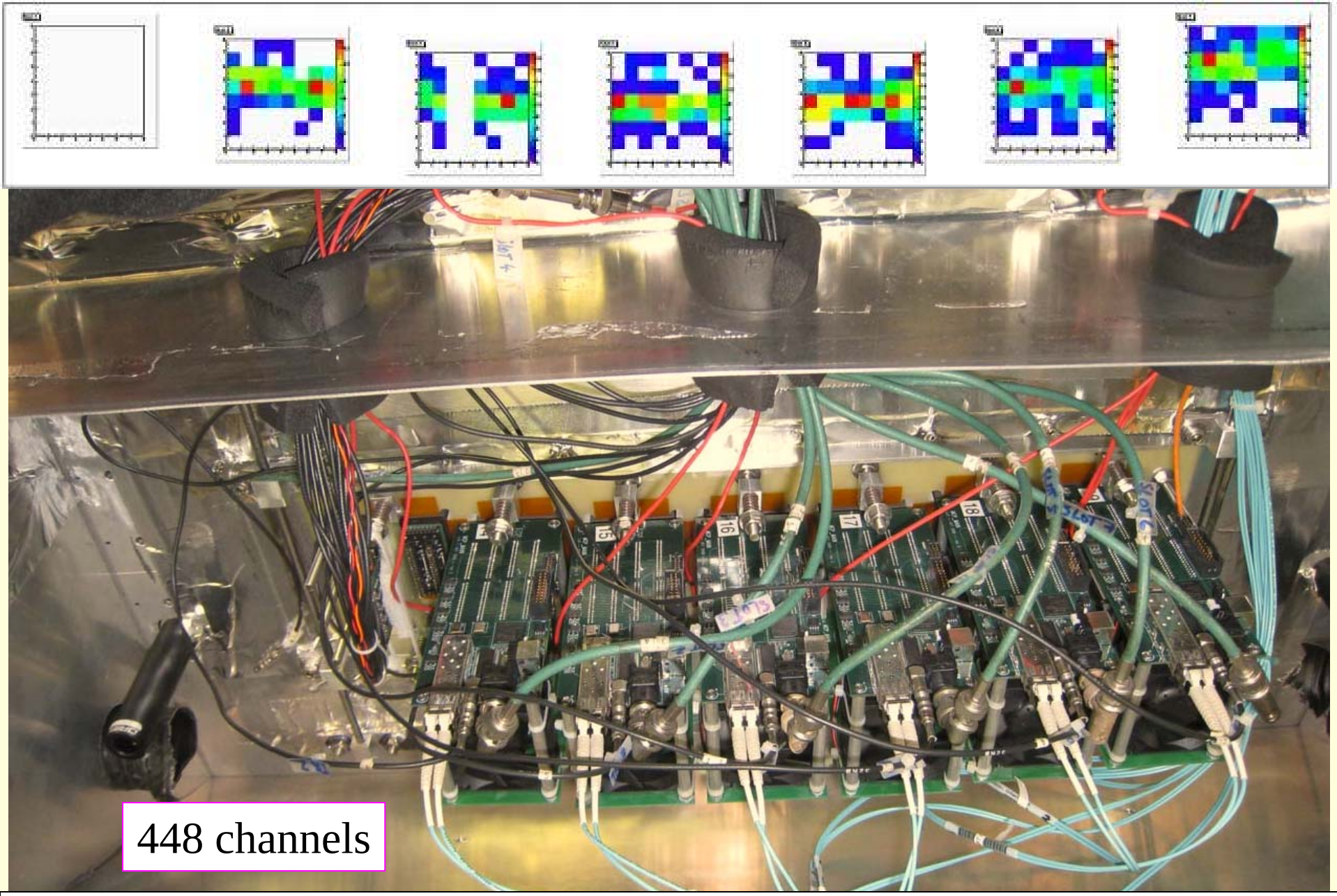
- Up to 8x64 channels per cPCI card
- Very portable DAQ
- Up to 3,584 channels/cPCI crate

Cheap, commodity backend



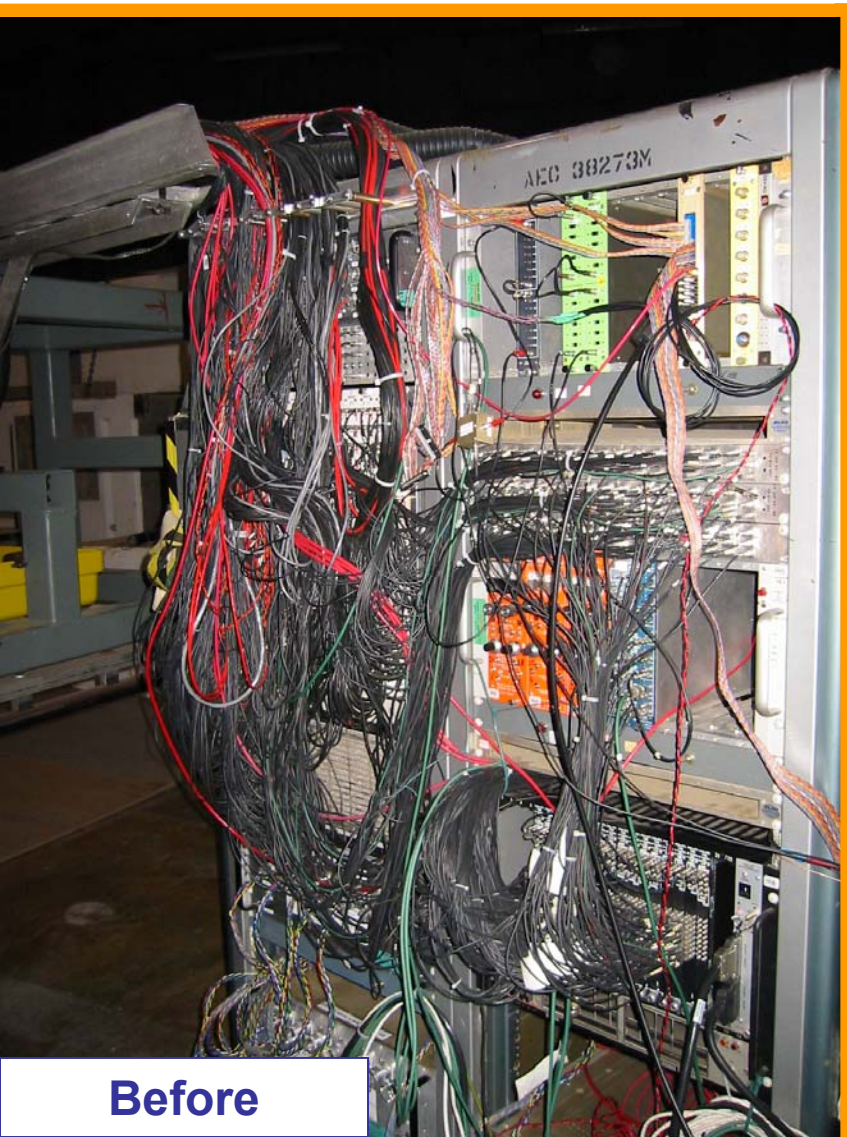


Originally: (just amps [custom CFD]+CAMAC ADC/TDC)

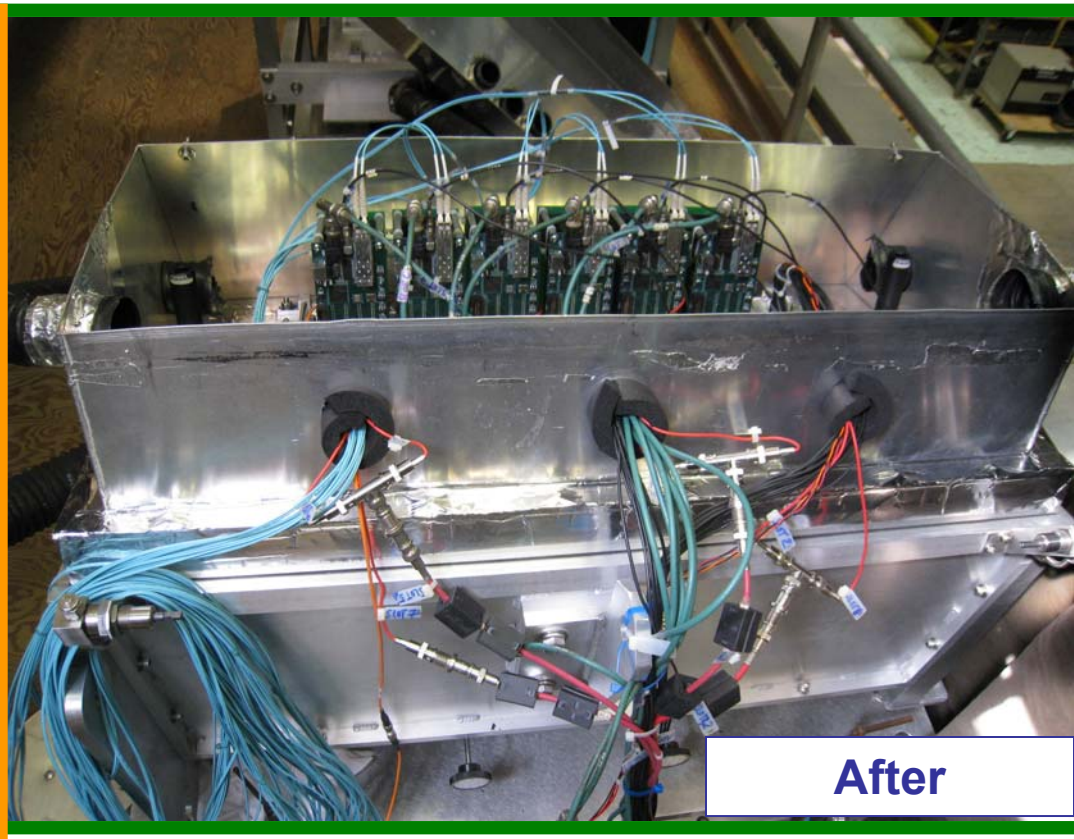


New: Integrated photodetector electronics with waveform sampling

Huge Reduction in Cable Management



Before

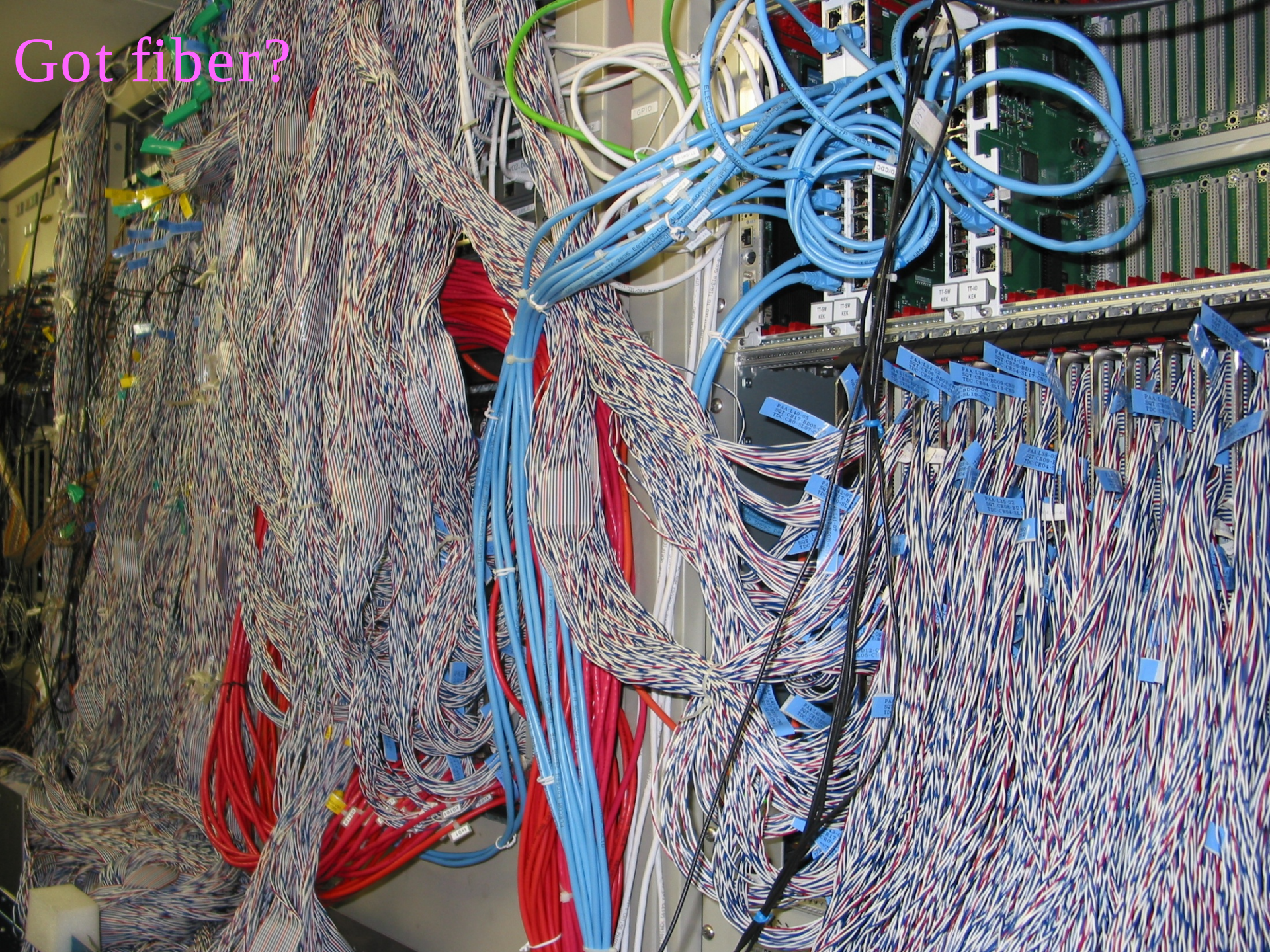


After

"Is that it?!?"

-Matt McCulloch (in surprise of how few cables were used in the electronic upgrade)

Got fiber?

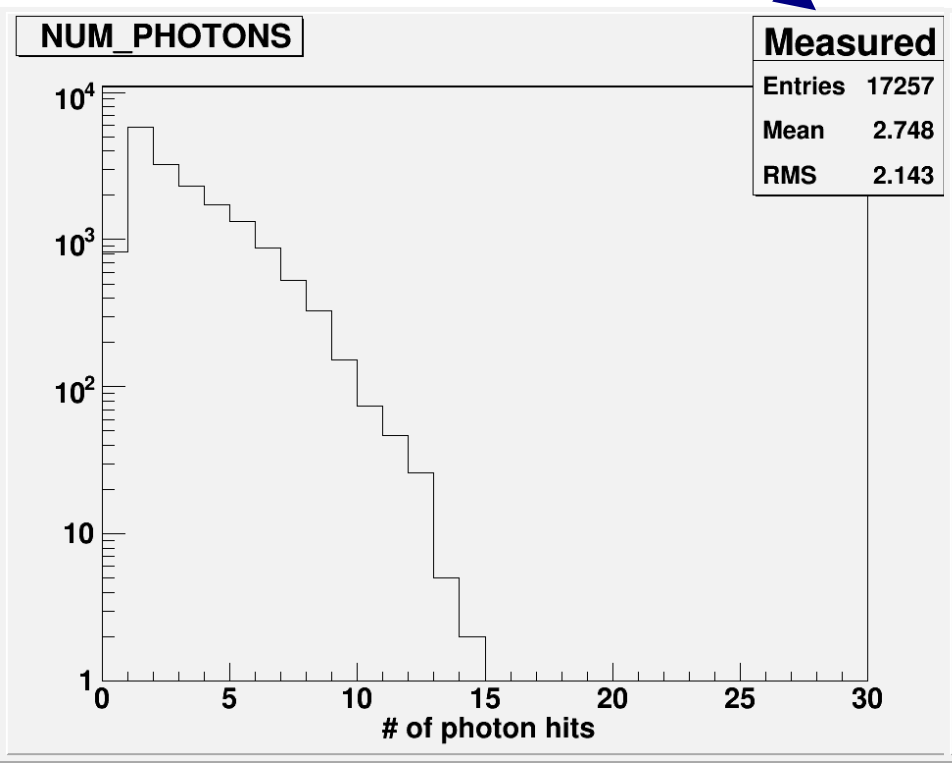


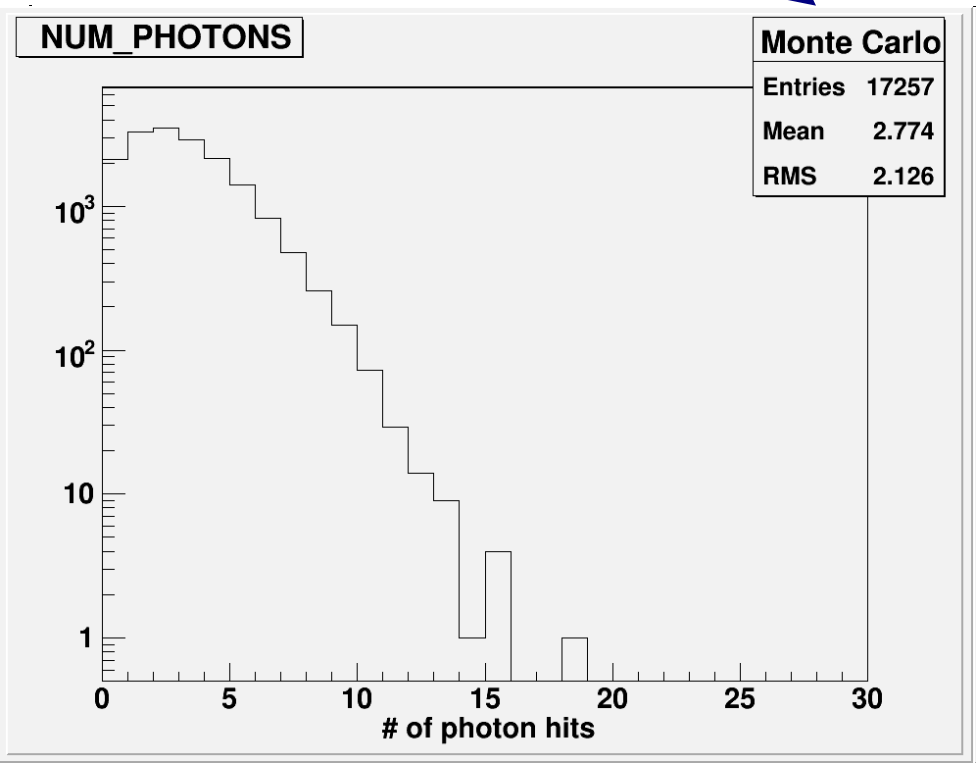
Data taking since Jan. 2009

Cosmic Muon Telescope: Number of Photo-electrons

Measured: Mean = 2.75

G4 Simulation: Mean = 2.77



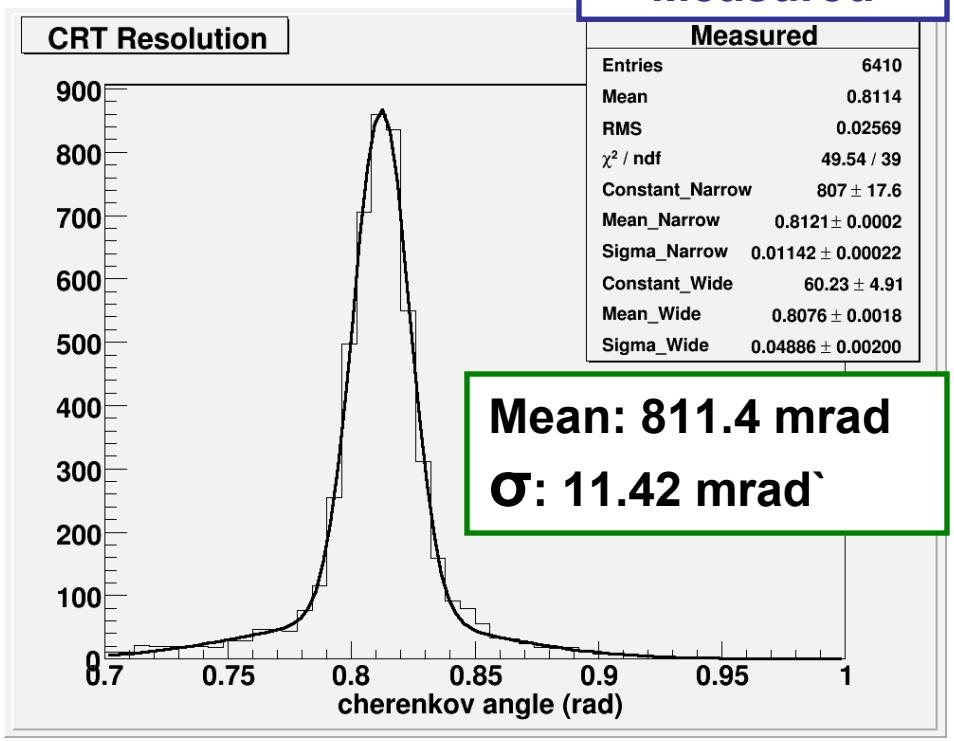


Cosmic Muon Telescope: Cherenkov Angular Resolution

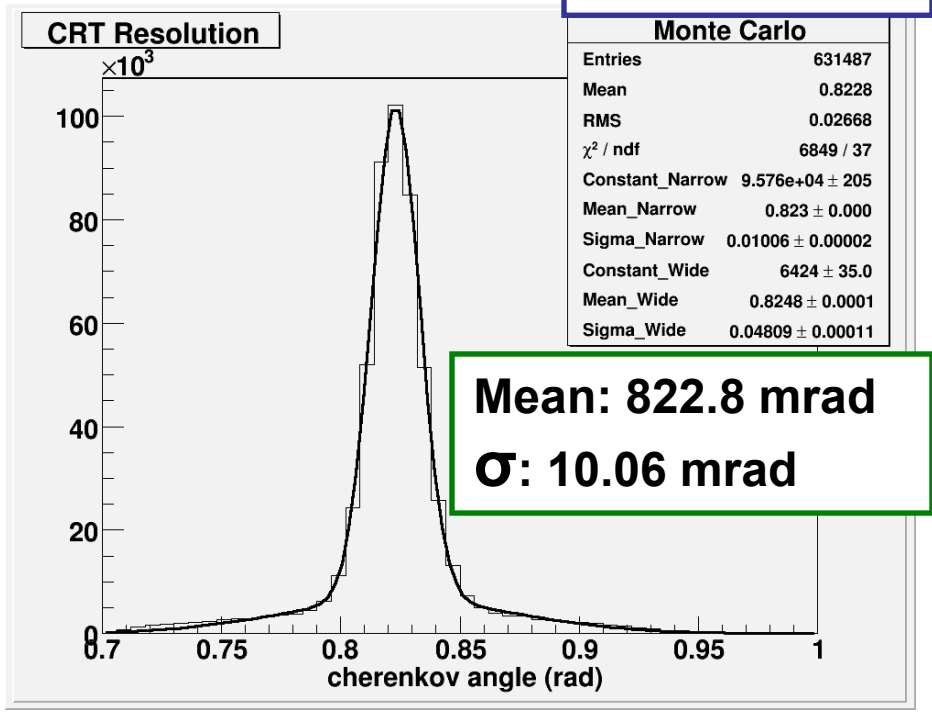
- Shift in mean due to systematic error in PMT holder survey
- Distribution shapes agree well with each
- **Chromatic correction next (T0)**

Larry Ruckman thesis

Measured



Simulation



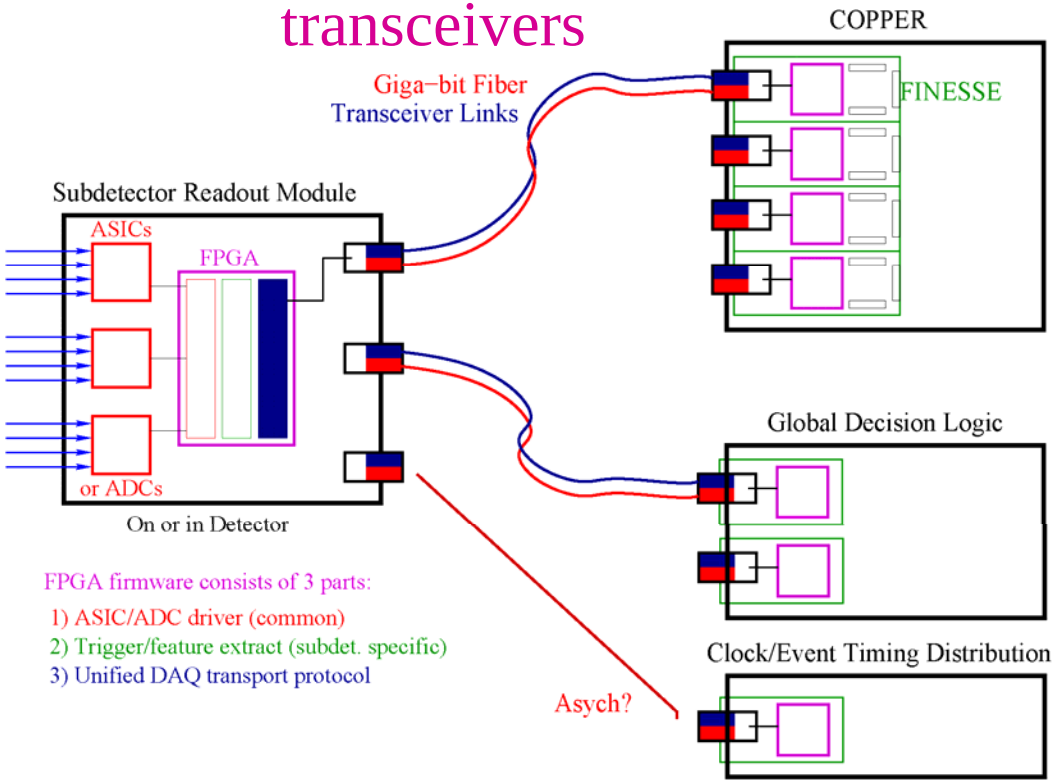
Summary of lessons learned

- Synchronize sampling (BLAB2 → BLAB3)
- Better timing distribution
- Better amplifier
- Need fast feature extraction
- Self-calibration (in situ) useful, individual channel offset timing calibration essential!

Belle II Barrel-PID DAQ Overview

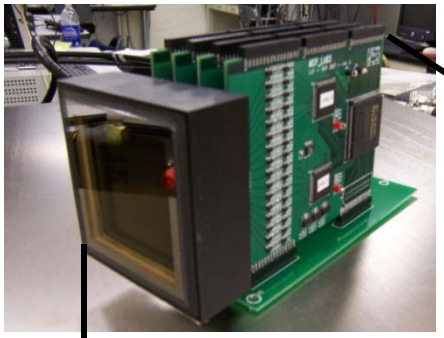
128 DAQ fiber transceivers

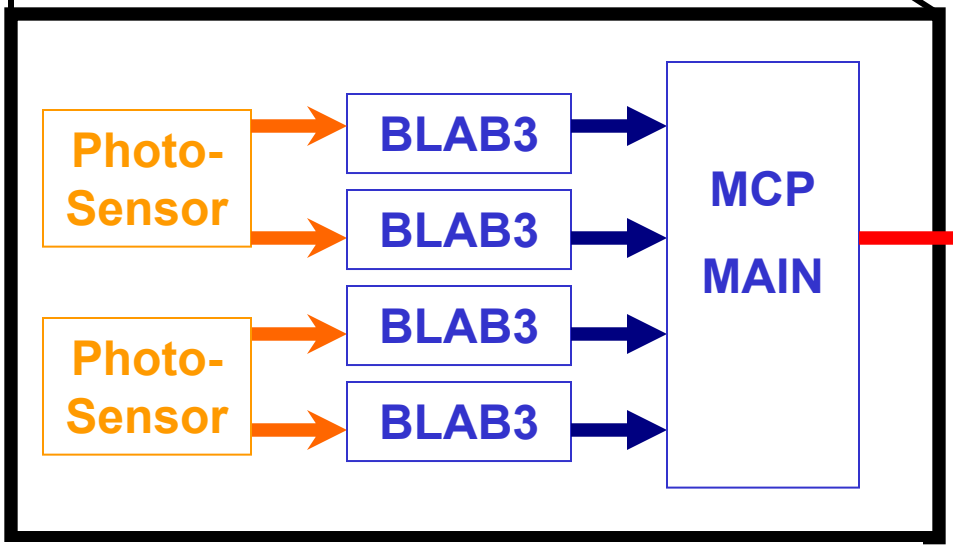
8k channels
1k BLAB3
128 SRM



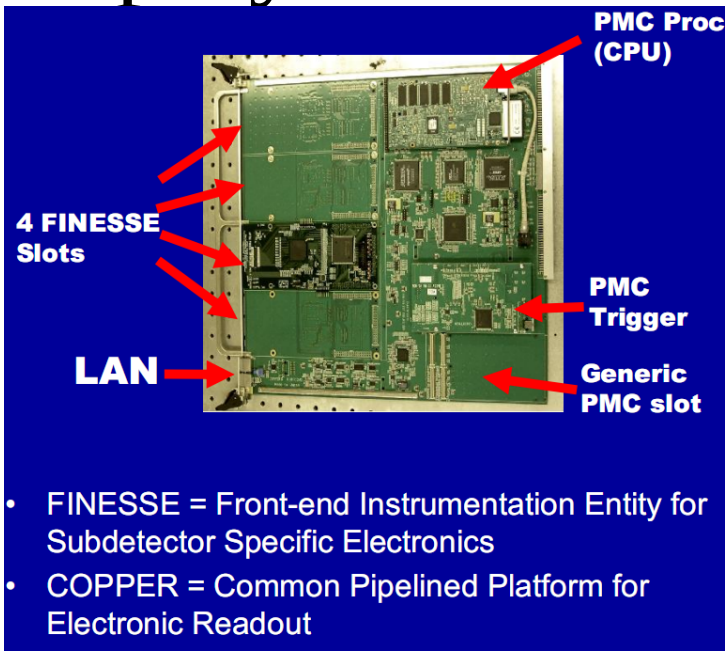
32 FINESSE
8 COPPER

Very similar to SLAC deployment





Giga-bit Fiber links



x4 → FINESSE CARD → x4 → COPPER FIFO

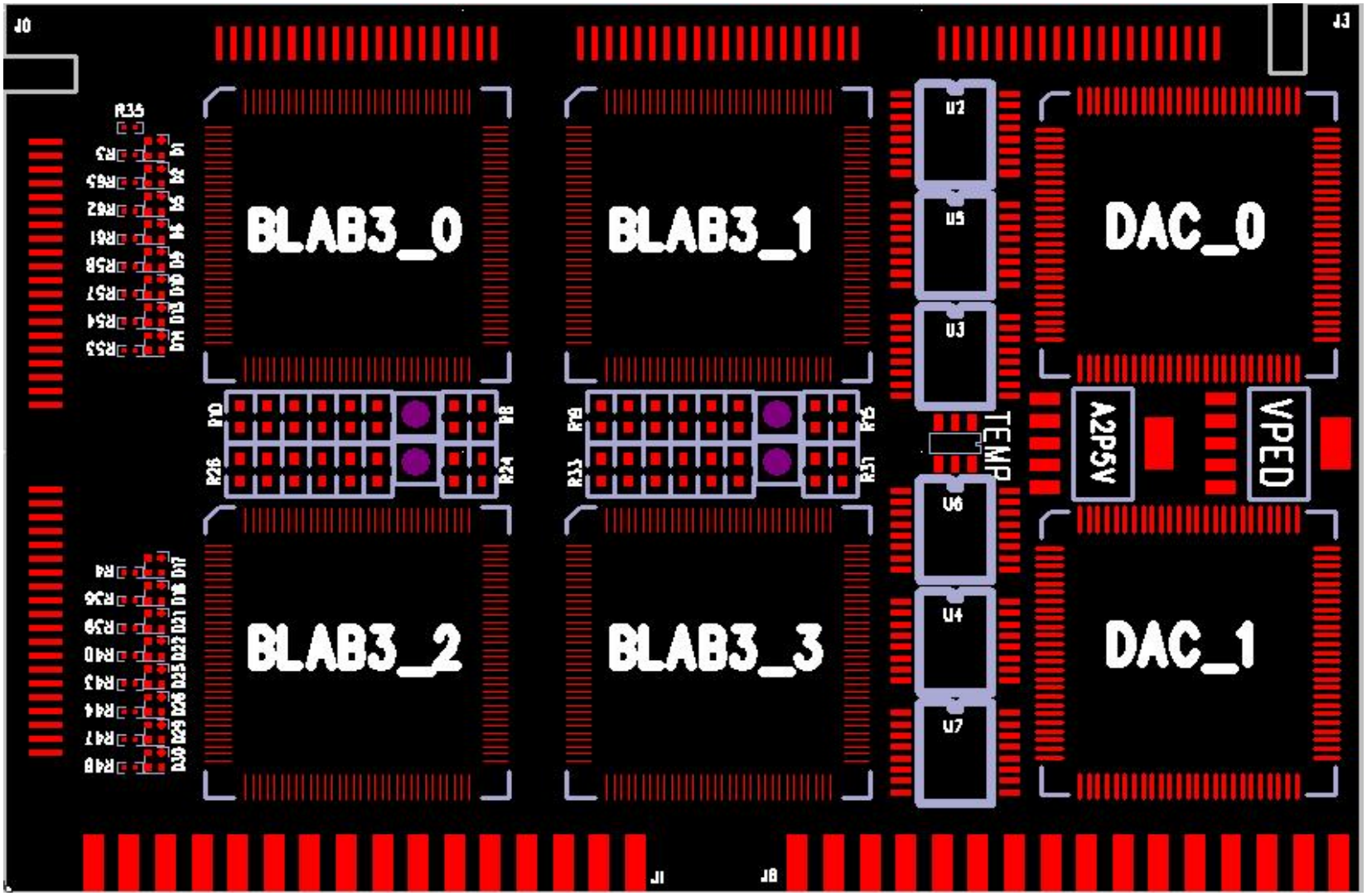
- BLAB3 is 8 channels, each 32k samples deep
- ~1us + 20ns/sample to read out (zero suppressed)

xTOP baseline has ~ 8k channels

14

75.1806 mm by 51.18055 mm

32 PMT channels input



4x 8-channel BLAB3 ASICs

Bias, sampling rate,
Trigger threshold DACs

BLAB3 Specifications

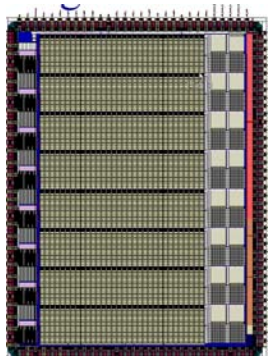
32768	samples/chan (>5us trig latency)
8	channels/BLAB3 ASIC
8	Trigger channels
~9	bits resolution (12[10]-bits logging)
64	samples convert window (~16ns)
4	GSa/s
1	word (RAM) chan, sample readout
1+n*0.02	us to read n samples (of same 64)
30	kHz sustained readout (multibuffer)

- Time alignment critical
  - Synchronize sampling to accelerator RF clock
  - >5us a must for trigger
- Gain ~ 60 (target 50:1 SNR)

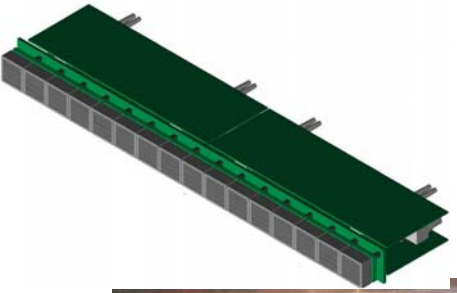
xTOP: DSP_FIN

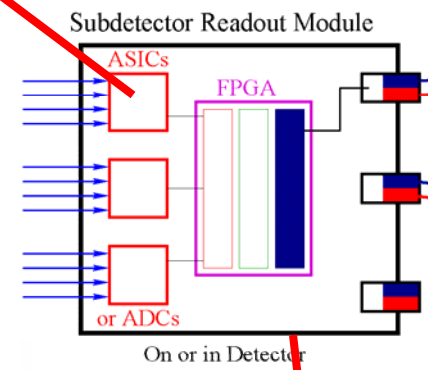
- each DSP core can process 60k waveforms/sec (measured)
- 30kHz L1 trigger rate and 2% occupancy:
  - each fiber brings in data from 96 PMT channels
  - each DSP_FIN board can handle 384 PMT channels

Almost ready for B-PID 1/16 test



BLAB3 received
Jan. 12

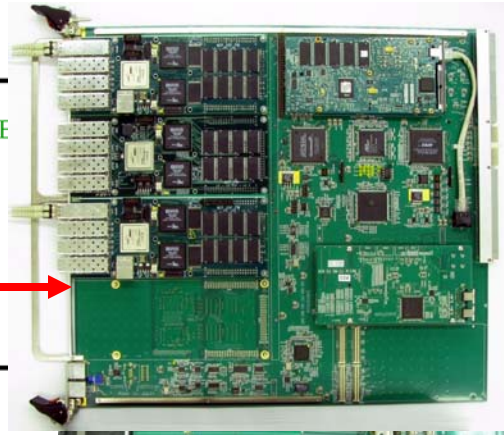




Giga−bit Fiber
Transceiver Links

COPPER

FINESSE



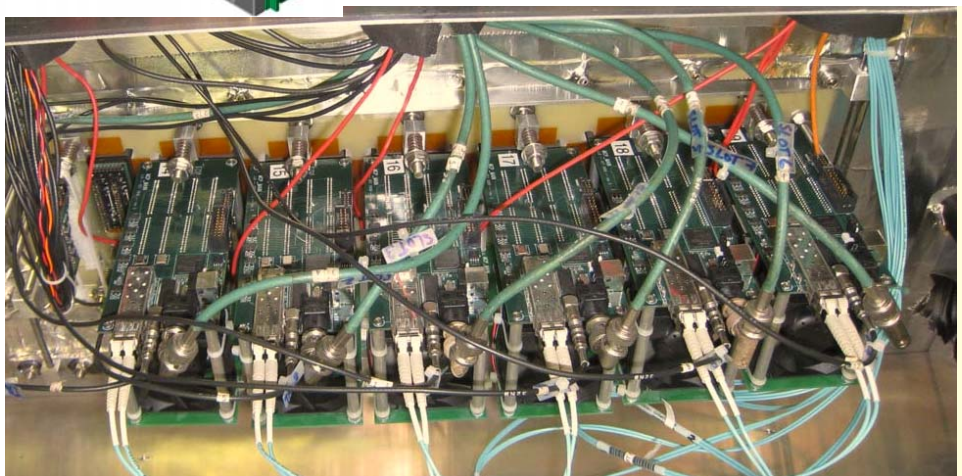
Global Decision Logic

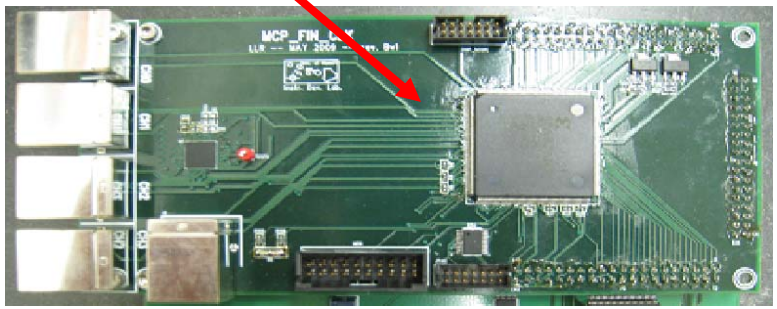
Clock/Event Timing Distribution

FPGA firmware consists of 3 parts:

1) ASIC/ADC driver (common)
2) Trigger/feature extract (subdet. specific)
3) Unified DAQ transport protocol

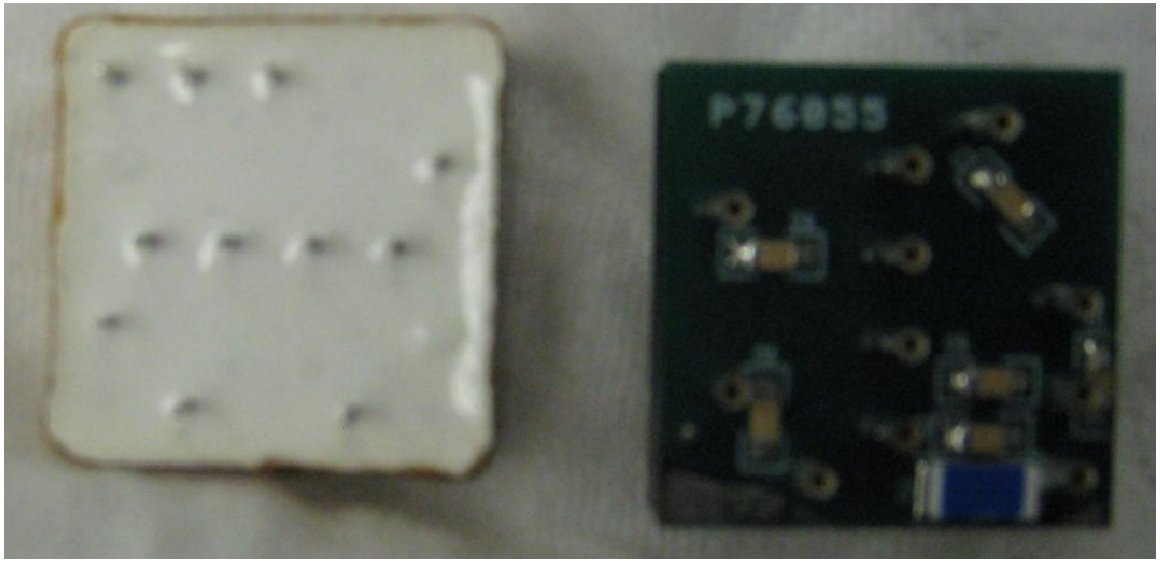
Asych?

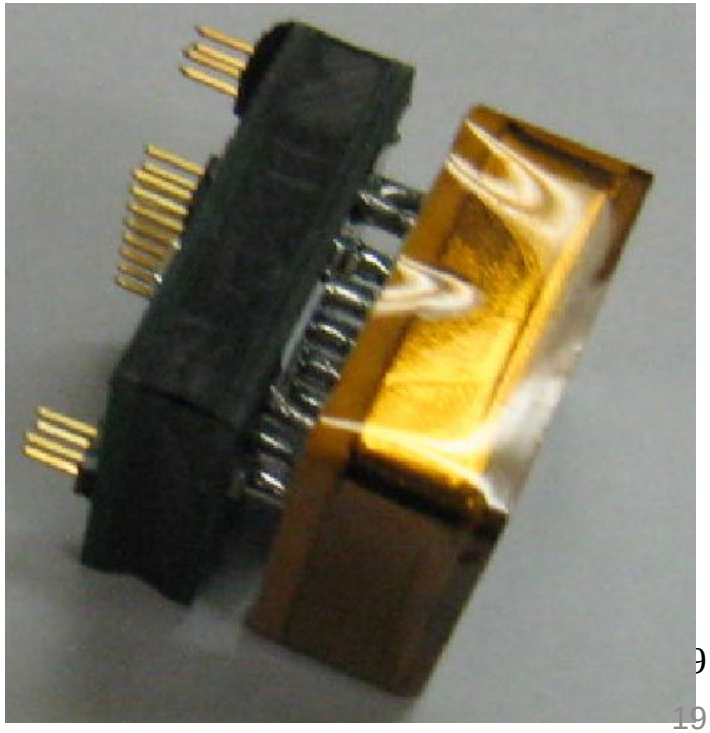


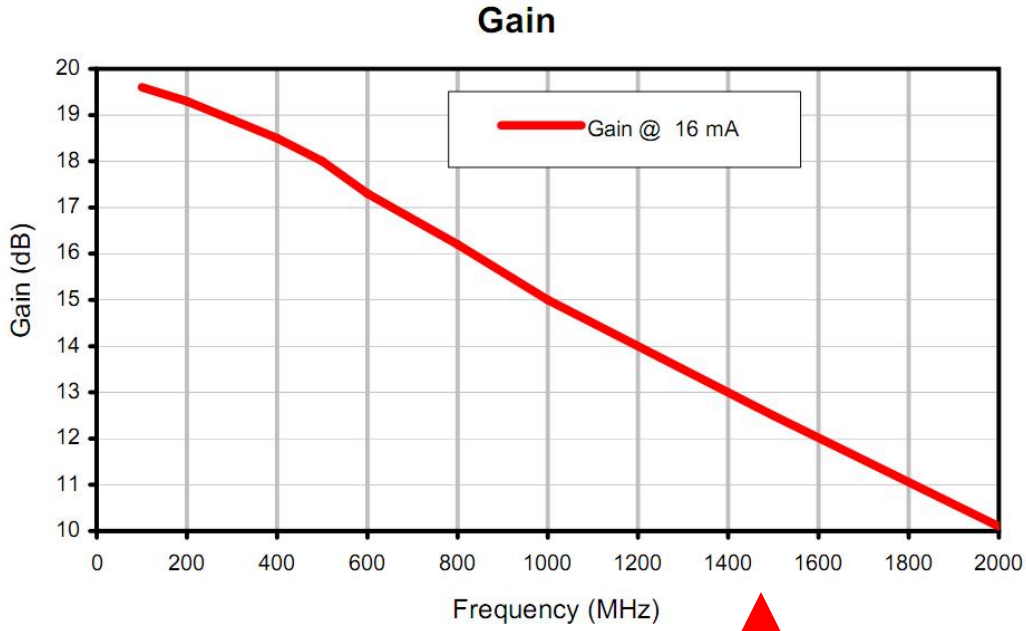


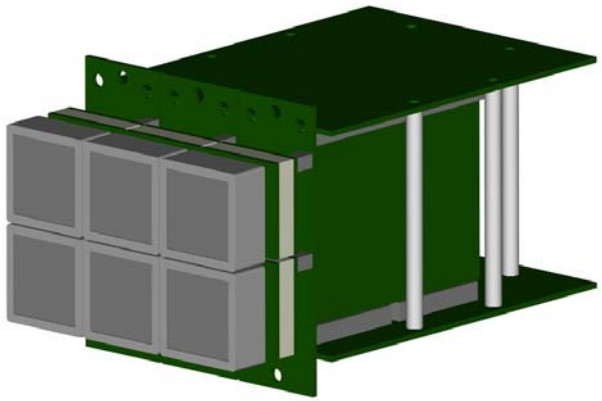
HPK SL10 & “Pluggable” Base board

- Socketed connector from SL10 to base board
- Standard 2mm pitched connectors from base board to readout electronics
- Only use SMD capacitors and resistors



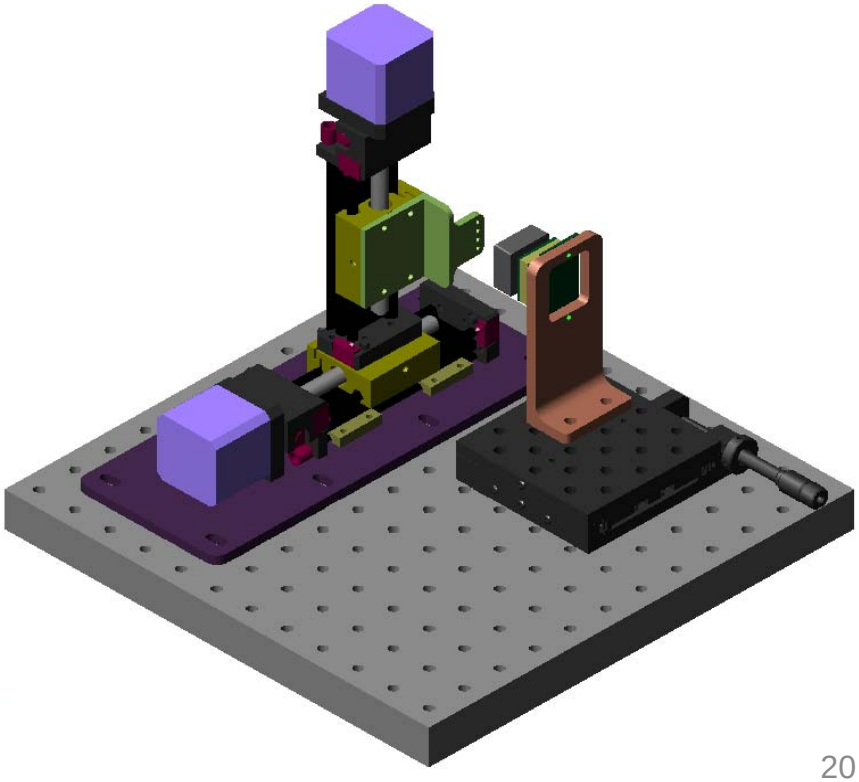




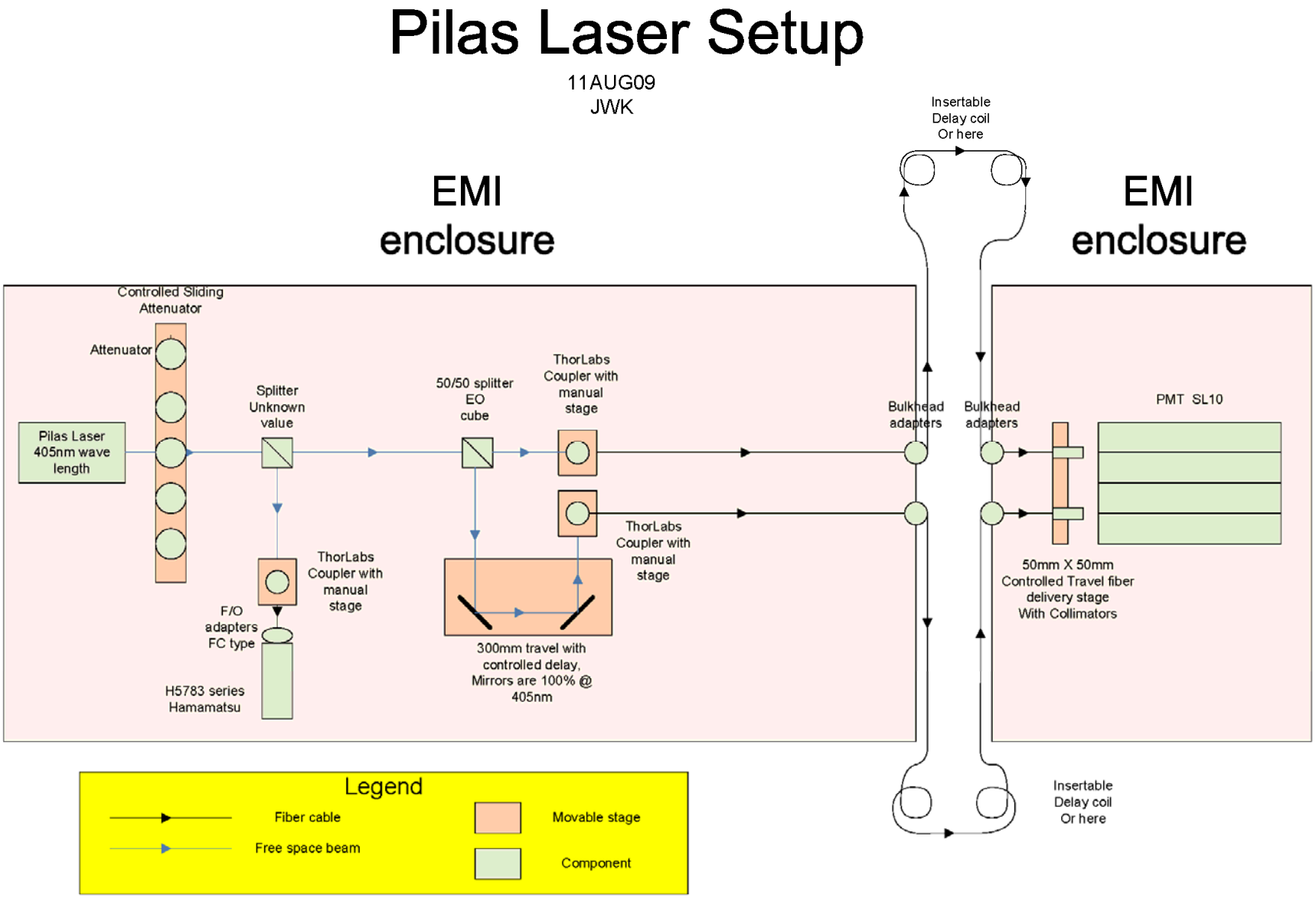


Laser Scan

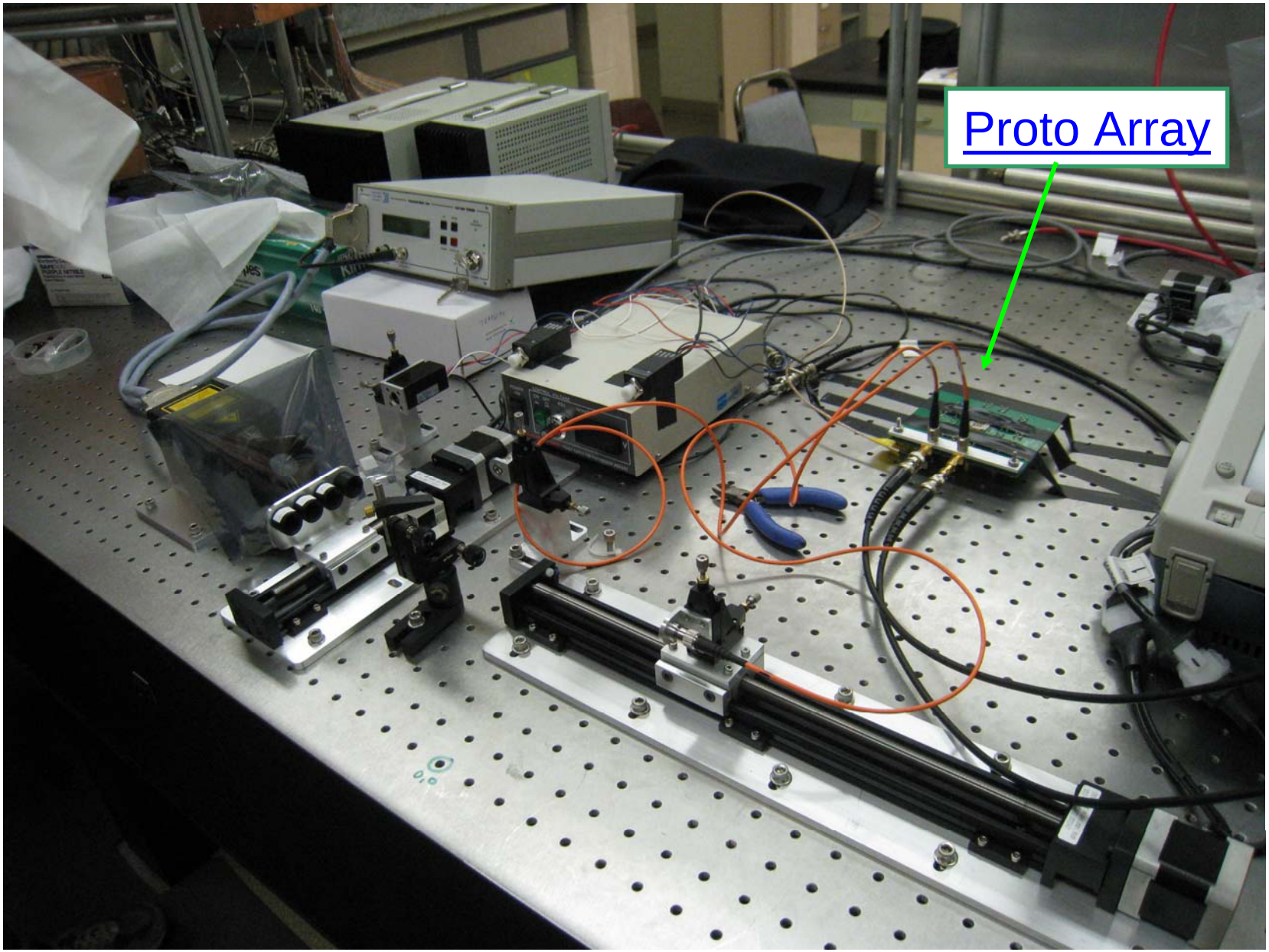
- Pilas ps pulsed laser (405nm)
- Additional gain from Minicircuit Vam-6 (~15 dB gain)
- Waveforms recorded with TDS6804B (20 GSa/s, 8 GHz)



Laser test stand – cross-talk testing



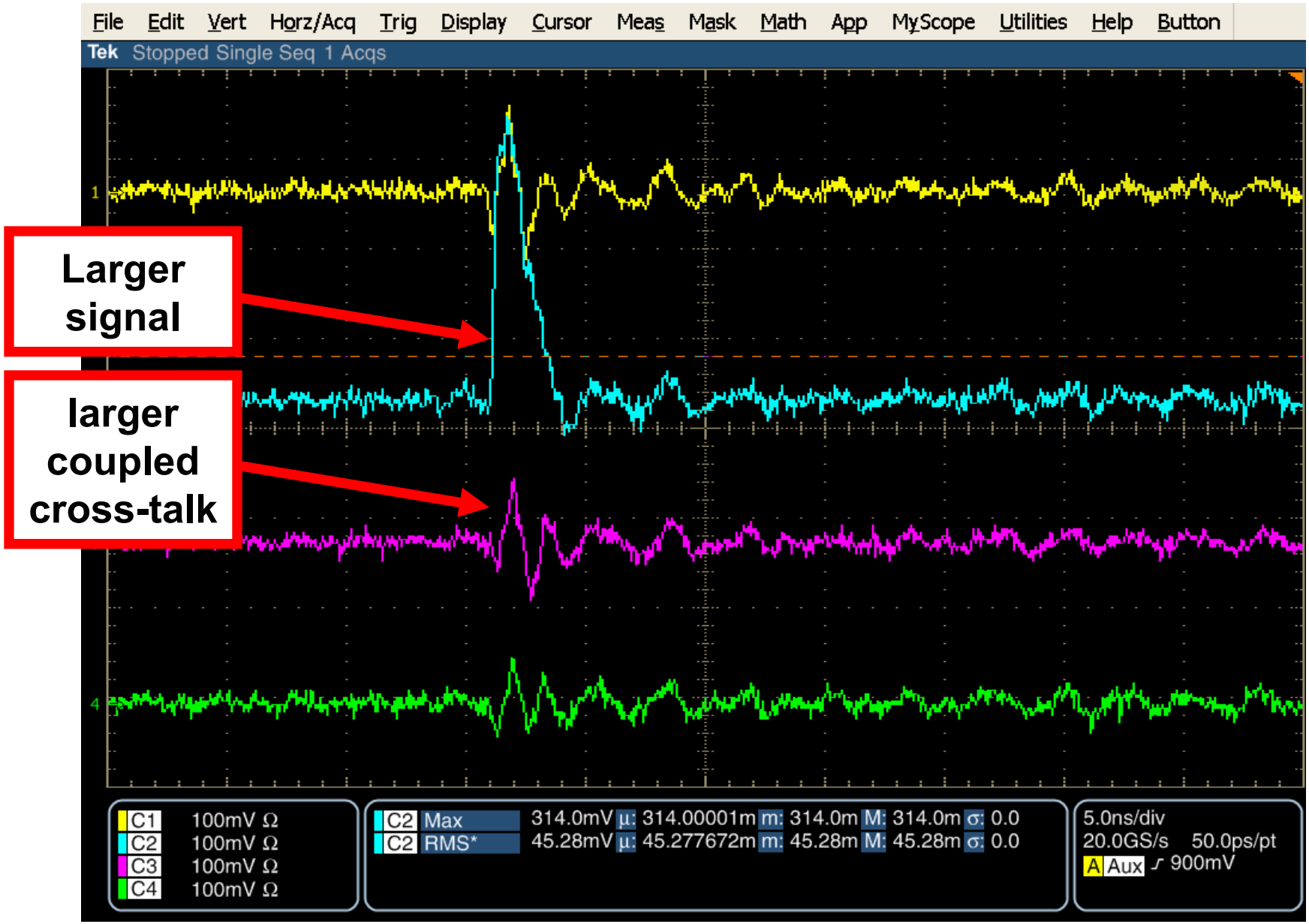
piLas test bench



Recorded Waveform example

23

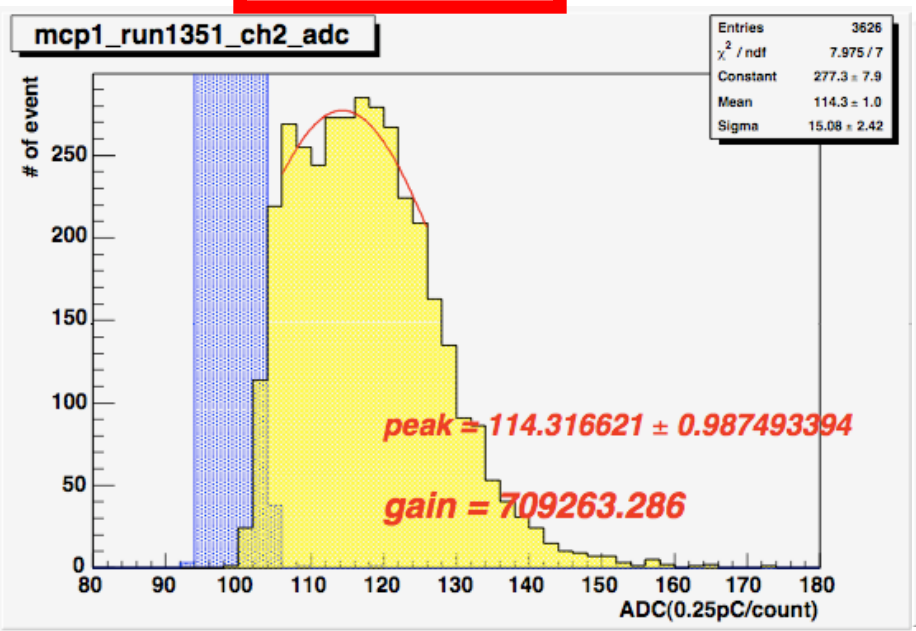
Cross-Talk



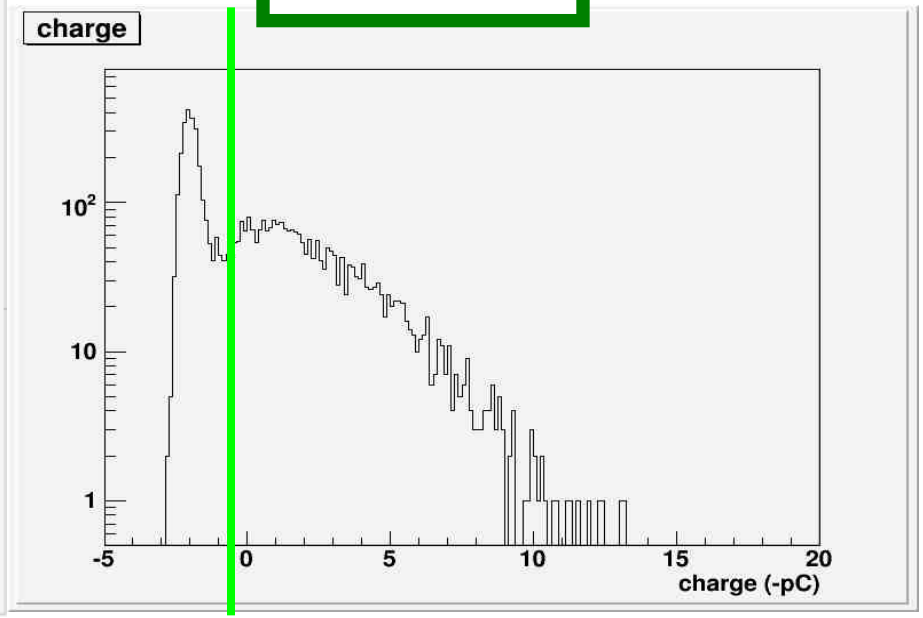
24

ADC Distributions

Nagoya



Hawai'i

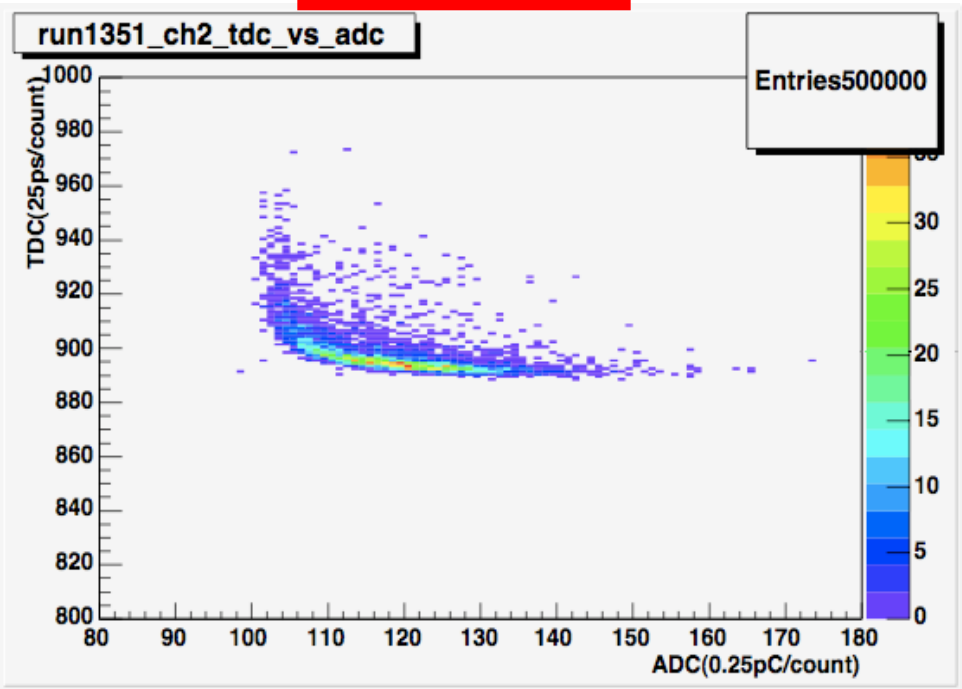


- Nagoya: larger gain for the external amplifier
- Hawai'i: recorded every waveform (even if no signal)

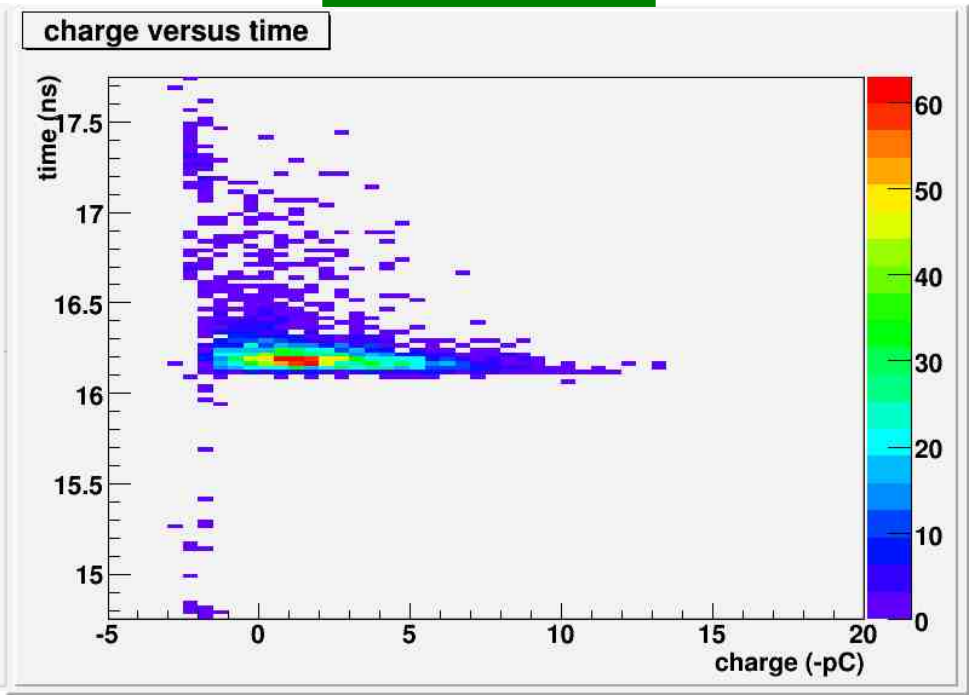
25

ADC vs TDC Distributions

Nagoya



Hawai'i

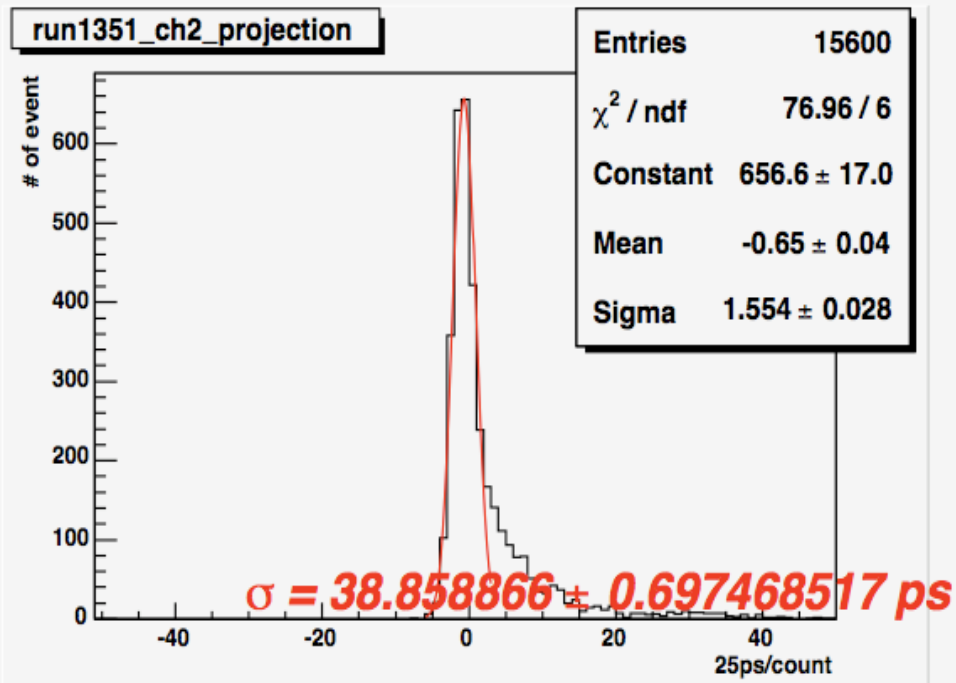


- Nagoya: time-walk correction performed
  - time is measured by CFD
- Hawai'i: no time-walk correction performed
  - time is measured by interpolating the leading edge threshold crossing using waveform data
  - Threshold set to 50% of the peak voltage for each event

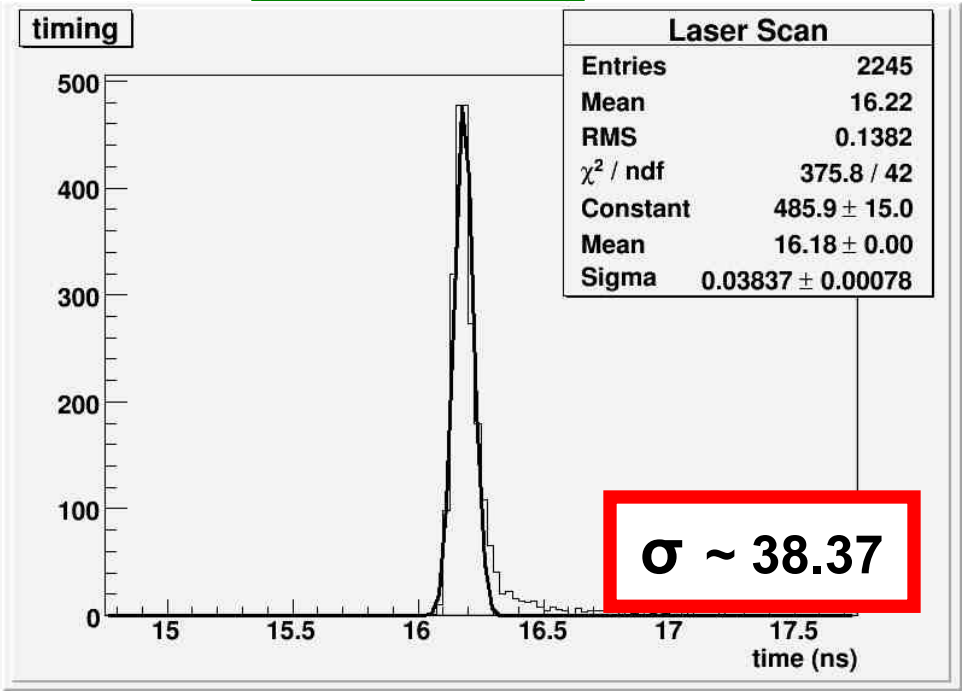
26

TDC Distributions

Nagoya

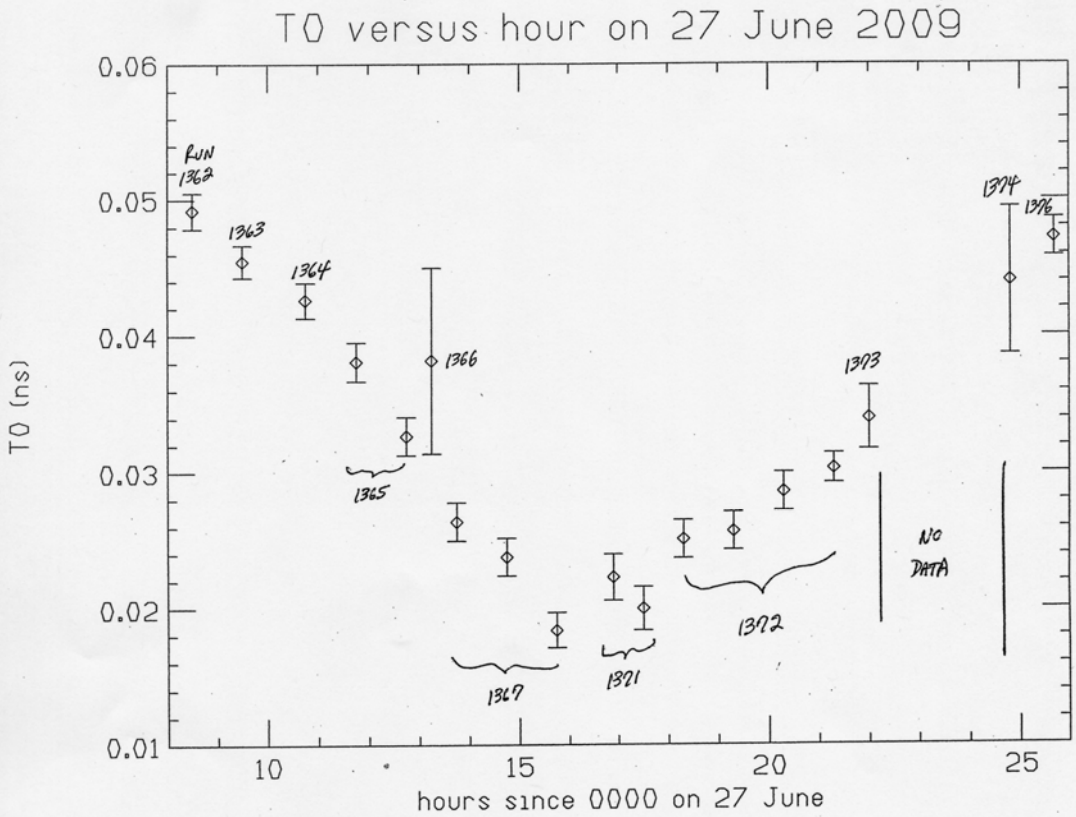


Hawai'i



- Nagoya & Hawai'i measurement agree with each other
- Hawai'i has less of a tail in distribution
  - Less overall TDC RMS

27



Estimate of timing error to use for MC

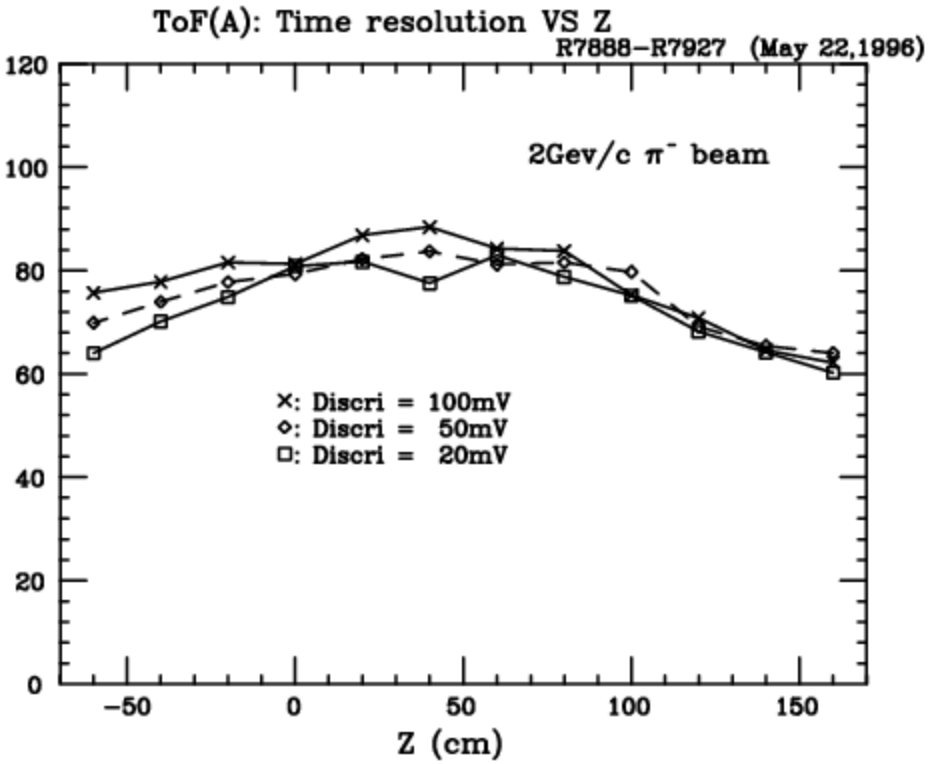
8-Apr-09 GSV

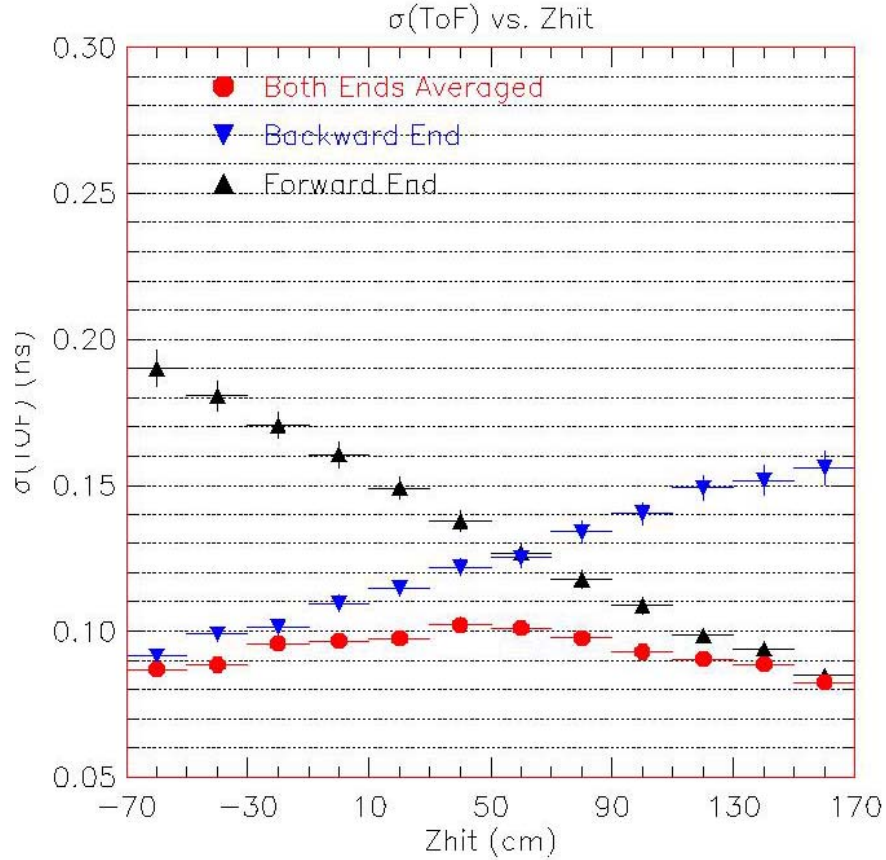
	Item	Est. param	unit	conv.	unit	Time [ps]	Item
1	Intrinsic bunch length (worst case)	5	mm	0.3	mm/ps	16.7	recent machine parameters
2	Jitter on RF clock @ electronics hut					10	Kichimi-san (from Tobiyama-san?)
3	Possible longitudinal osc @ higher I					0	if feedback does work?
4	Residual error after beam loading correction					2	W.A.G. currently
5	Error on predicted time (integral path length)					10	*Karim estimate*
6	Error on track impact position projection	1	mm	0.3	mm/ps	3.3	needs study
7	Jitter in clock system distribution					5	to be measured
8	Residual error in time encoding					10	to be measured
	TOTAL					**24.9**	best case?

>10 years experience at KEKB

Based on TOF experience…
25 ps "worst case or best case?"

(e.g. "80ps" TOF)





Very detailed MC study:
J.W.Nam *et. al*
hep-ex/0204030
NIM A491 (2002) 54-68

Difference?

σ^2_{fin} → 100ps – "known" ~ "physics" → 40ps

Summarized for BESIII meeting, June 2002

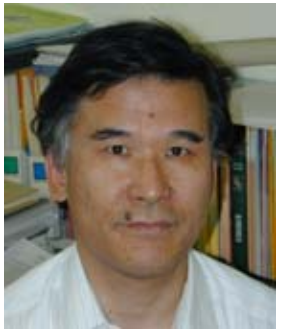
Care and Feeding: Manpower

- Jorge Rodriguez
  - CLEO Cal. Expertise
  - Original T_0

- Karim Trabelsi
  - Backward Kalman
  - "EXT",Σ path
  - Tracking group

- Mike Peters
  - RecTOF
  - Combining statistics (1-4 dof)

- Mike Jones
  - Daily monitoring
  - Always finding problems



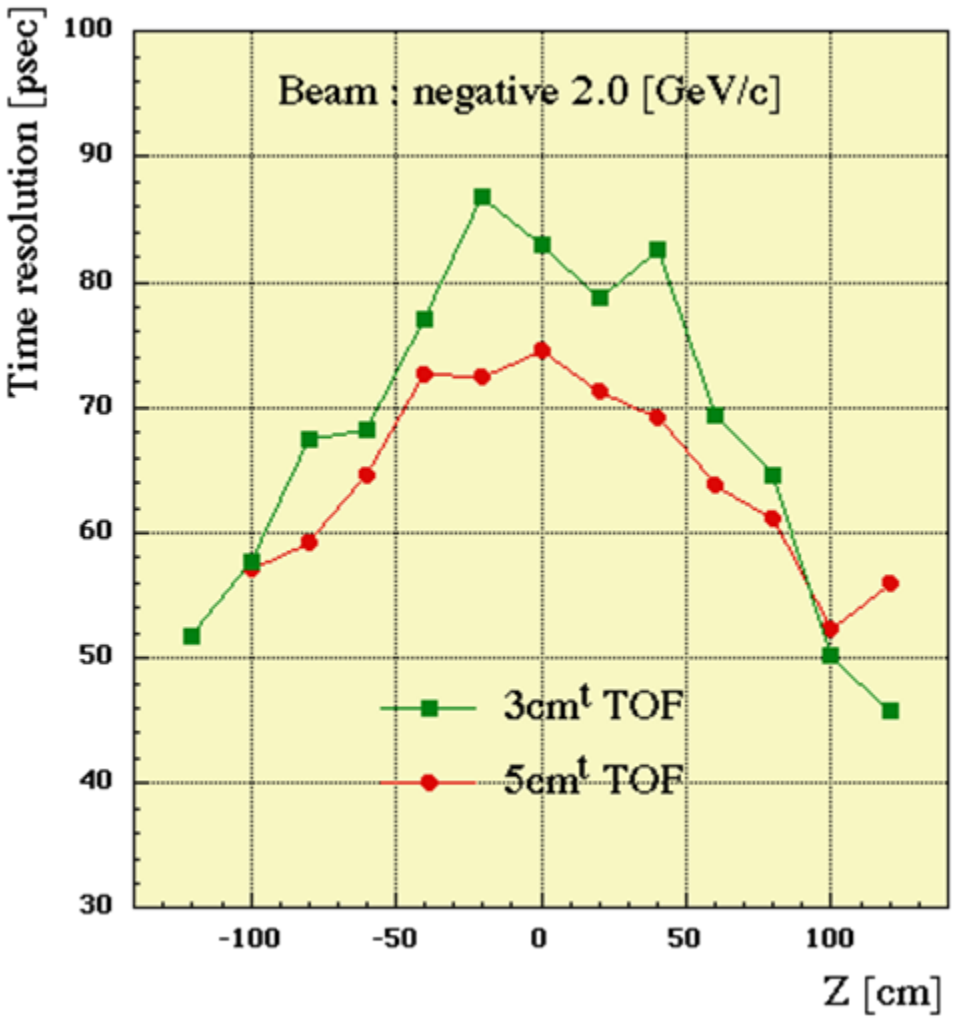
- H. Kichimi
  - TOF leader
  - Constant attention

- And many others!!
  - In particular many students who are based at KEK continually monitoring laser/Cal data

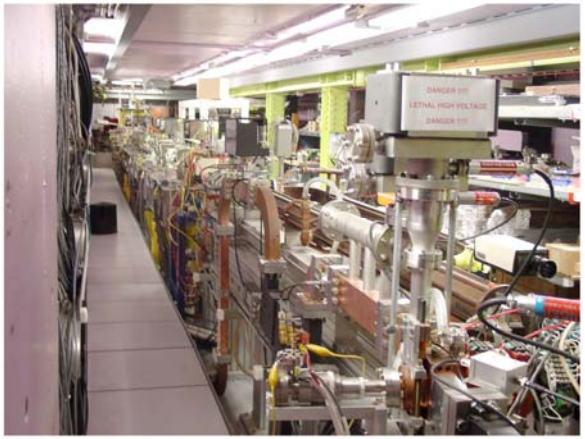
Lessons?

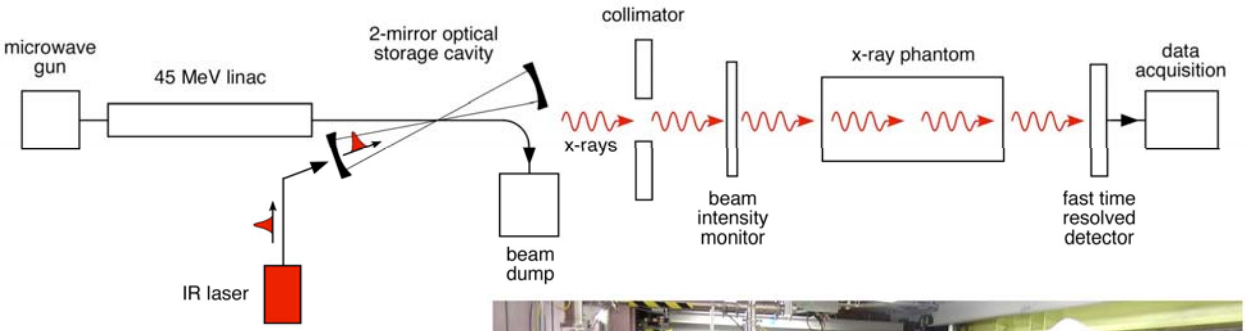
Be humble, design conservatively

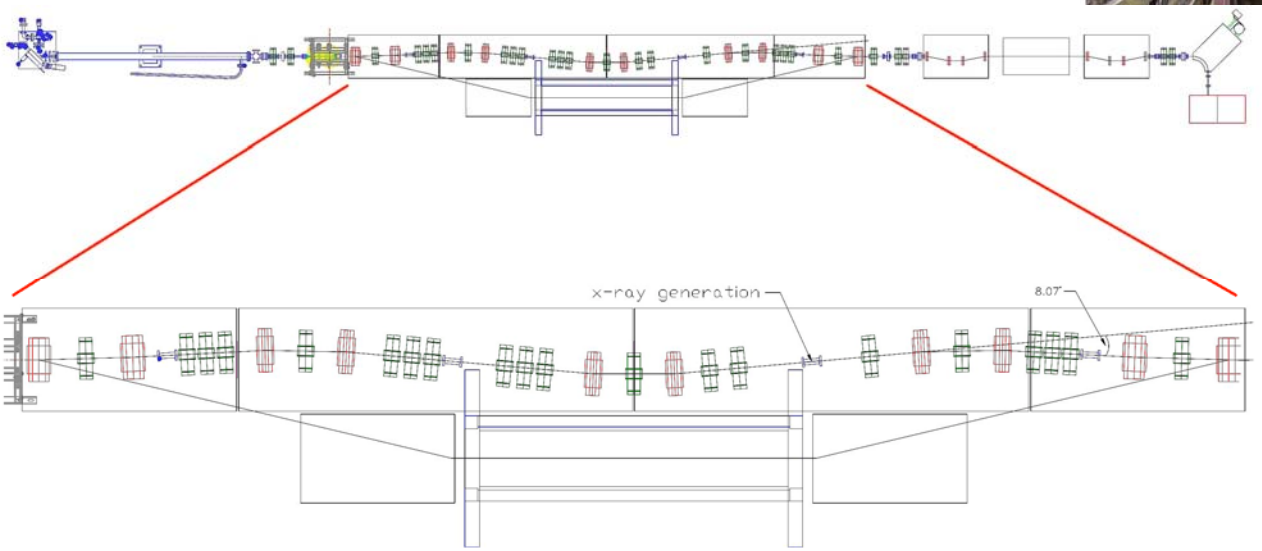
- Intrinsic Performance:
  - Tough to get
  - Beam tests don't require sustained operation
  - Hadronic Calibration!
    - Very important – details omitted due to space limitations
    - Much work, no fundamental understanding
    - Velocity dependent (dE/dx?) fudge
    - Systematic, so no SQRT(2)
    - May be TWC technique dependent
  - Sad history of underperformance:
    - CLEO, CPLEAR, BESII, …
  - Error Budget!!

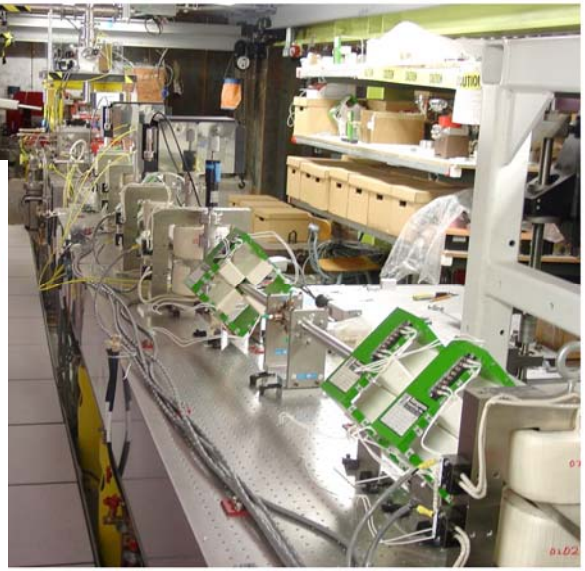


UH FEL as High intensity, pulsed x-ray source



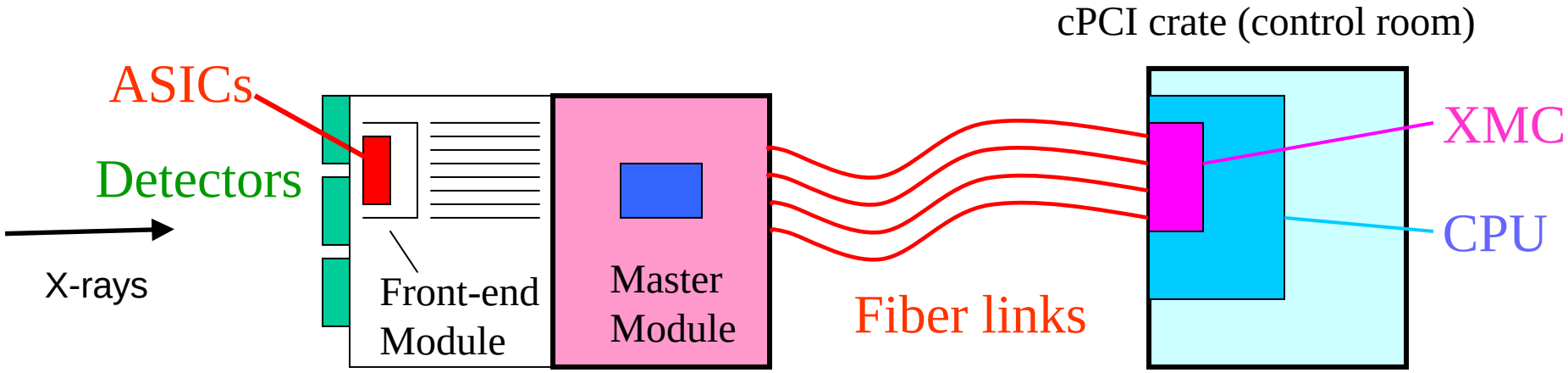




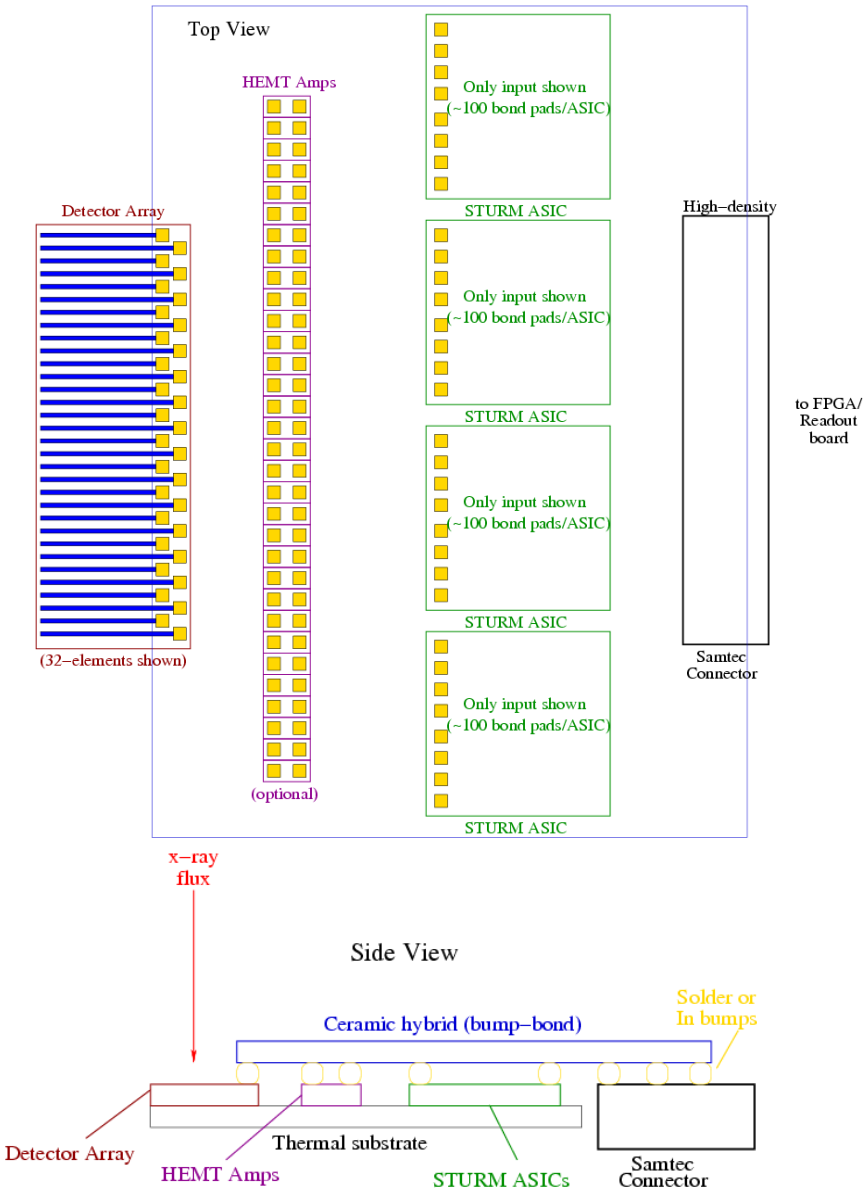


Readout for FEL x-ray beamline

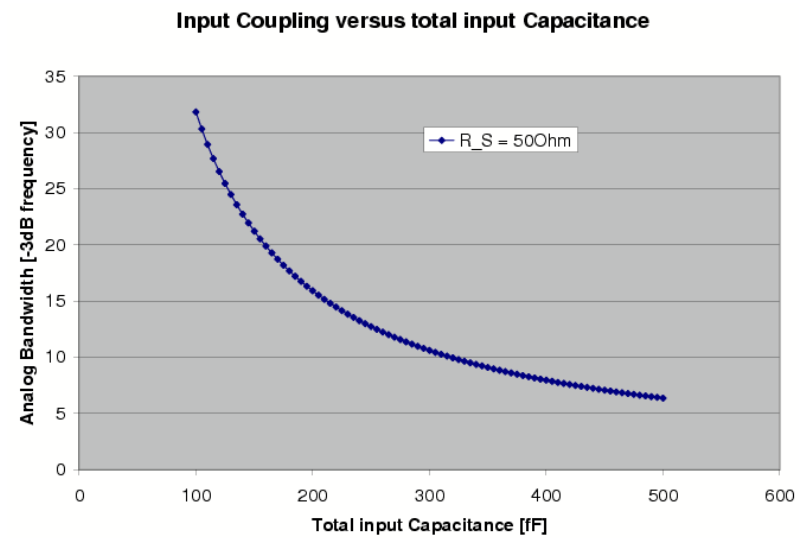
- 1-2 days running/week (1 floor down)
- 160 Channels
  - 16 detectors or detector channels/layer
  - 10 layers
- Modular system (expandable)
- 100 GSa/s during 10μs spill (10Hz rep rate)
  - 10μs/10ps = 10^6 samples/channel
  - Fiber: 12 Gb/s (4x 3.0Gb/s)

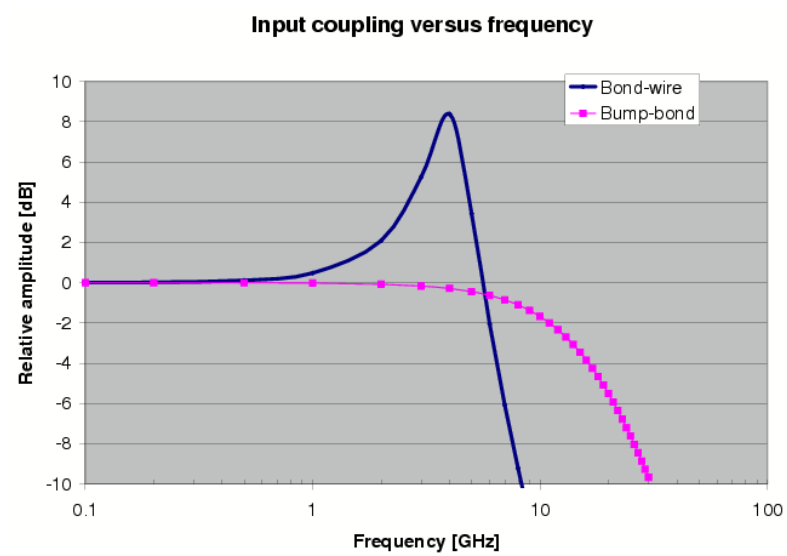


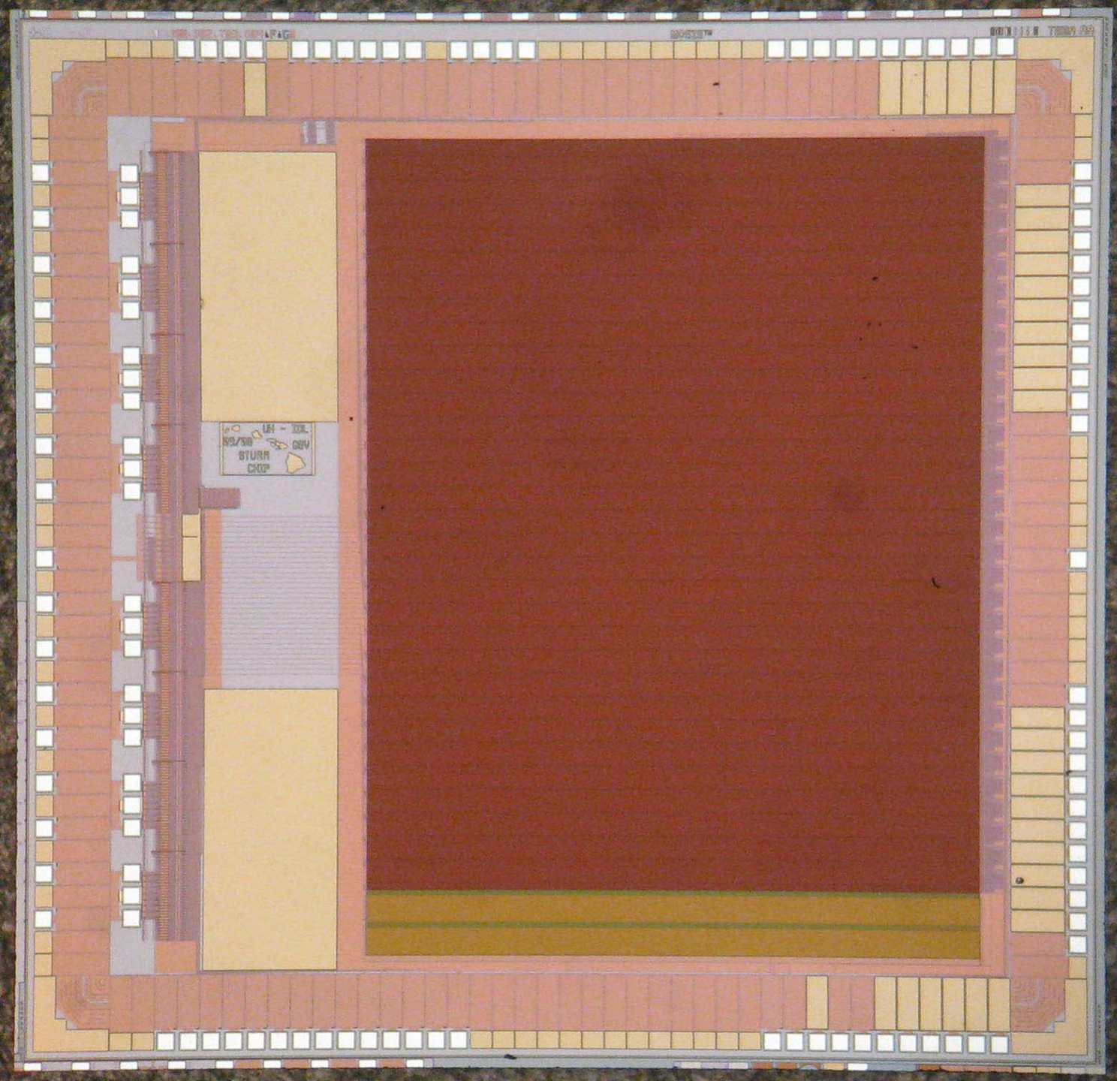
Sampler of Transients for Uniformly Redundant array Mask (STURM)



Push envelope on Bandwidth







STURM ASIC

~3.3 x 3.3 mm

8x channels

4x 8 flash samples/chan

200 GSa/s

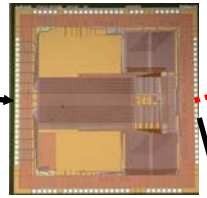
On chip ADC conversion (~5us/256 samples)

TSMC 0.25µm CMOS process

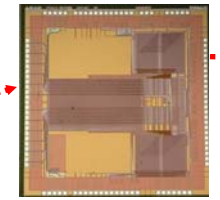
LABRADOR Family

STRAW1

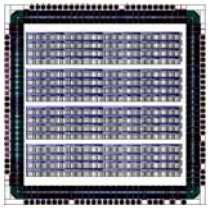
STRAW2



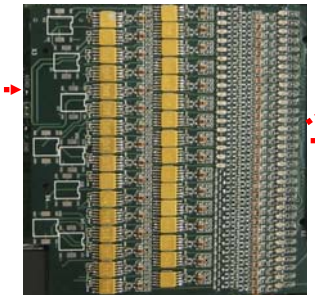
STRAW3



TARGET

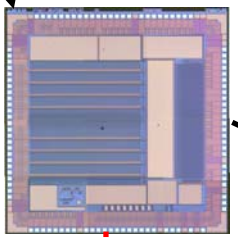


GLUE



SHORT2

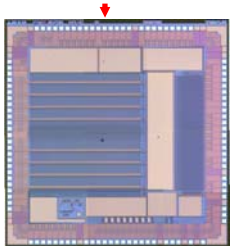
LABRADOR



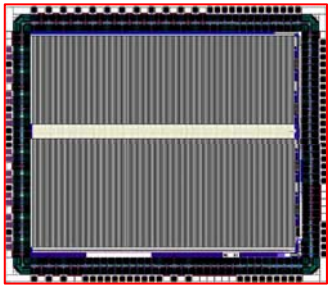
Comb.

Trig

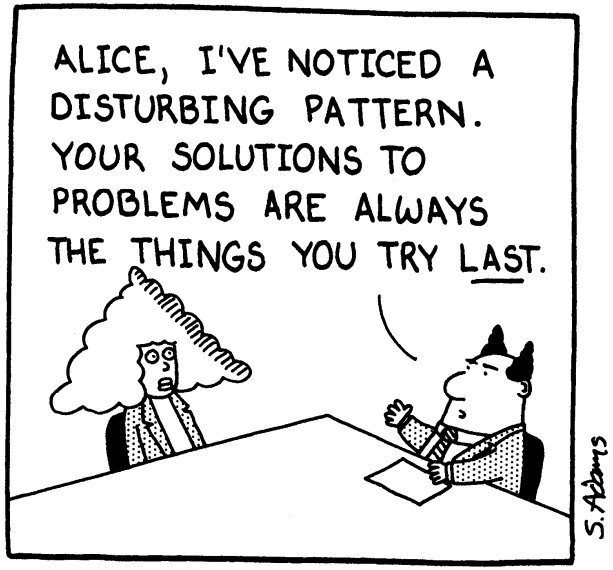
Sampling



LABRADOR2



LABRADOR3



What's next?

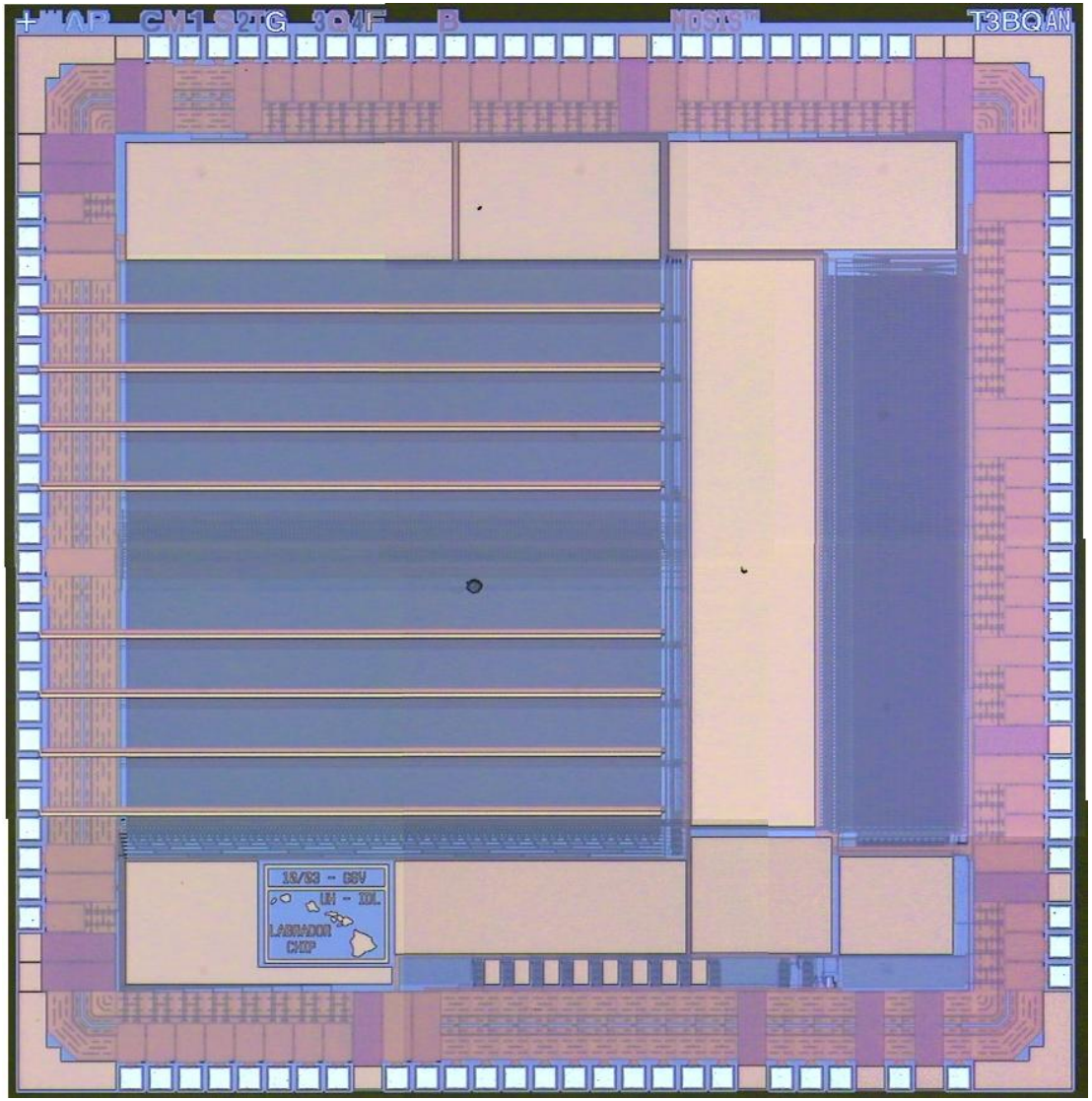
- Experience with chromatic correction in fDIRC prototype (upgrade to BLAB3 + DSP feature extraction)

- 1/16th test system iTOP (25ps system timing?)

- Evaluation of IRS/BLAB3/STURM2 ASICs

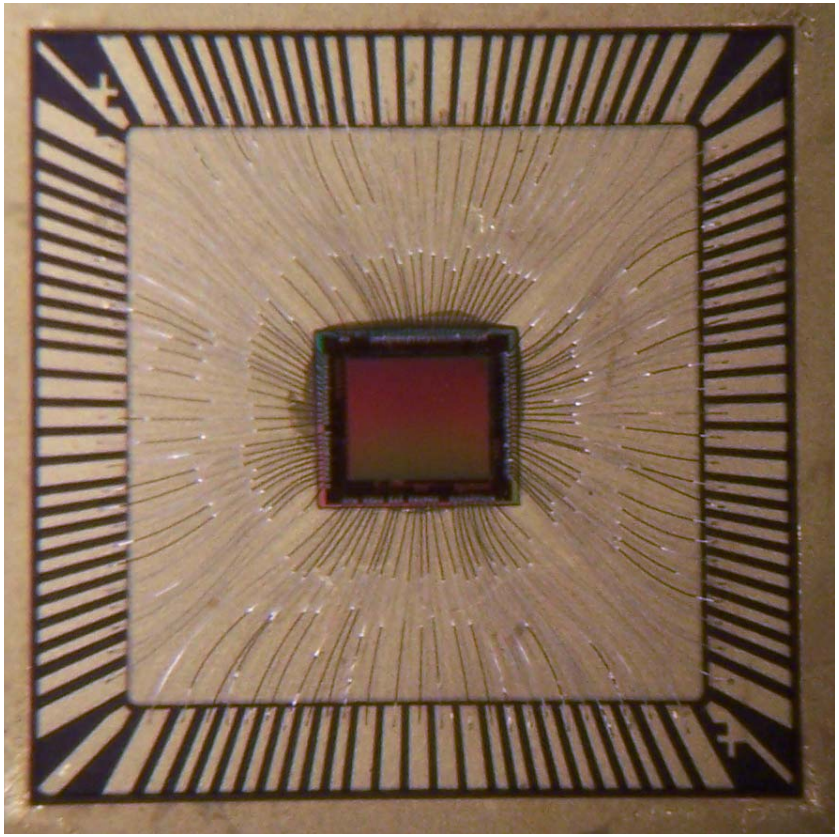
- Prepare readout boards for psTDC2, system architecture prototypes

Back-up slides



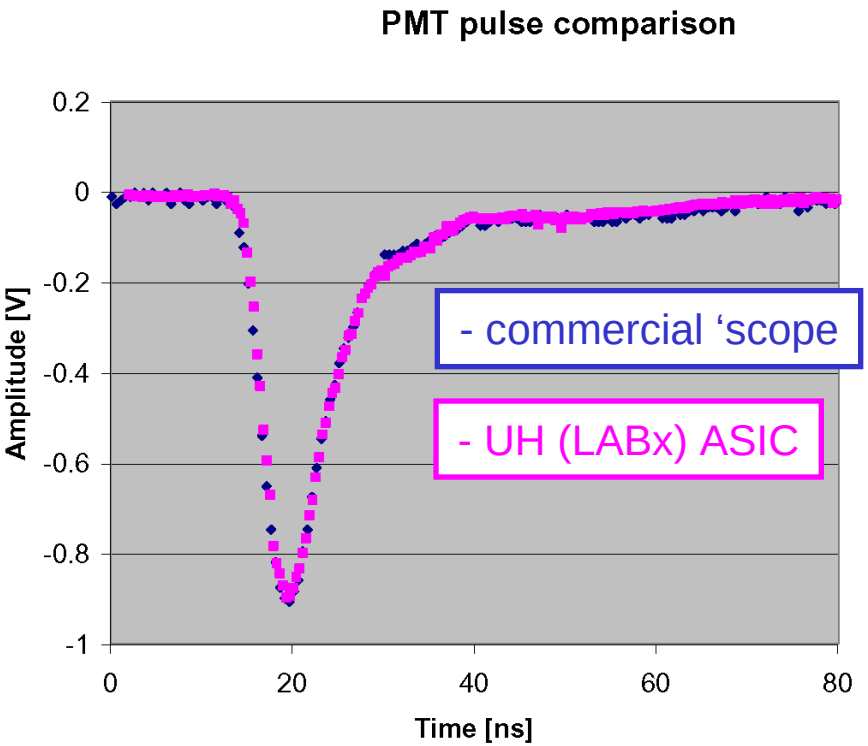
NIM A591 (2008) 534

Photo-detector ReadOut



BLAB1 Die floorplan: 128 x 512 samples
Single channel

3mm x 2.8mm, TSMC 0.25um



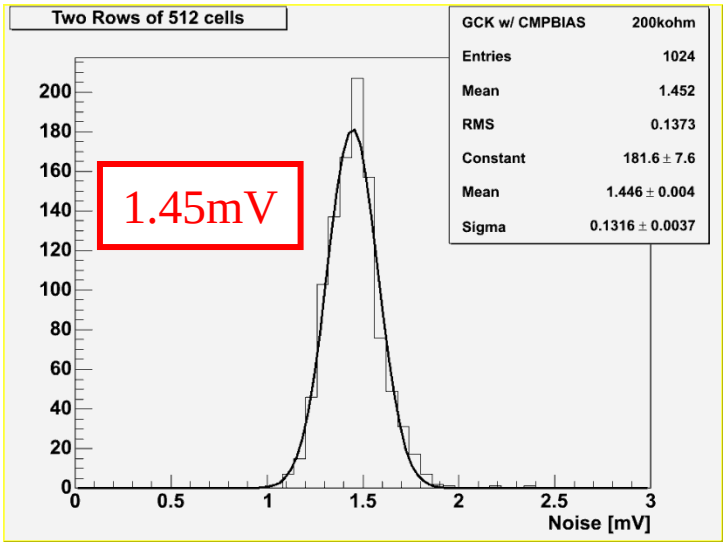
→Use large bandwidth capability developed for ANITA to improve timing
→ Advanced Detector Research award

"Oscilloscope on chip"

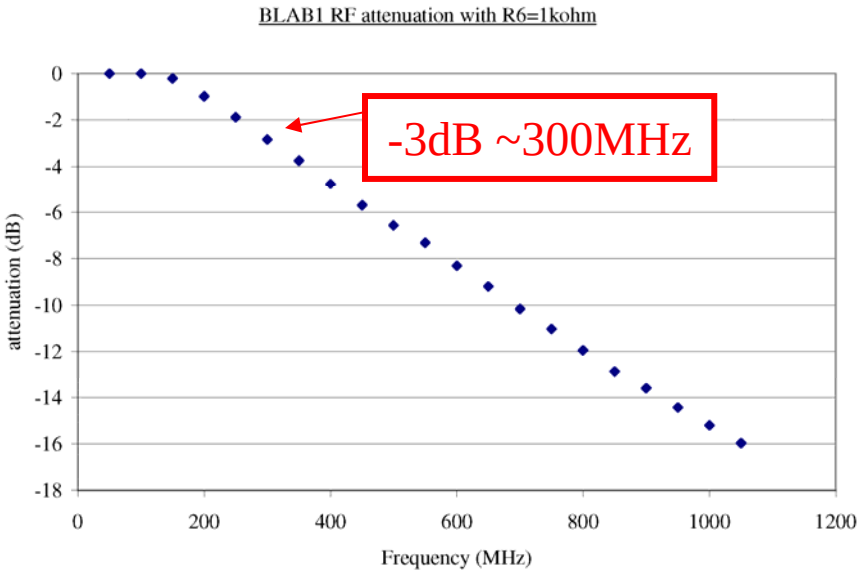
39

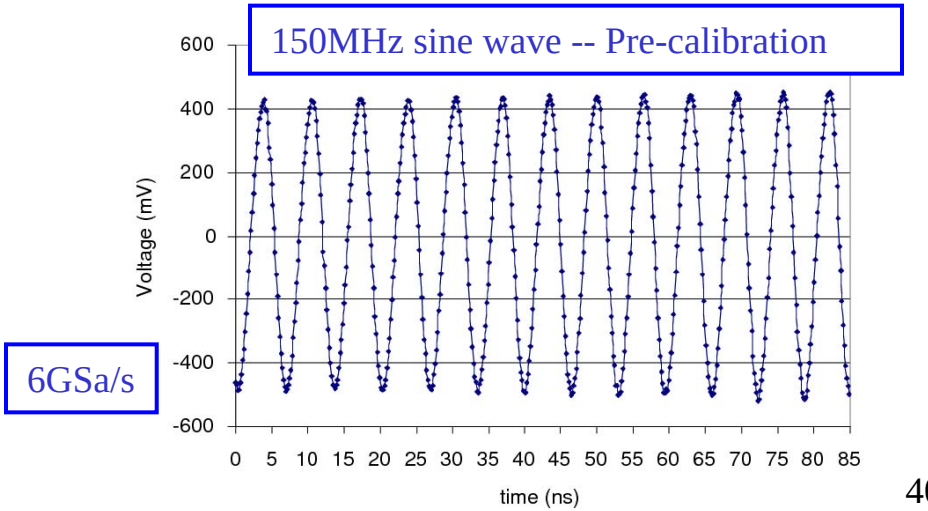
Buffered LABRADOR (BLAB1) ASIC

Measured Noise



1.8V dynamic range



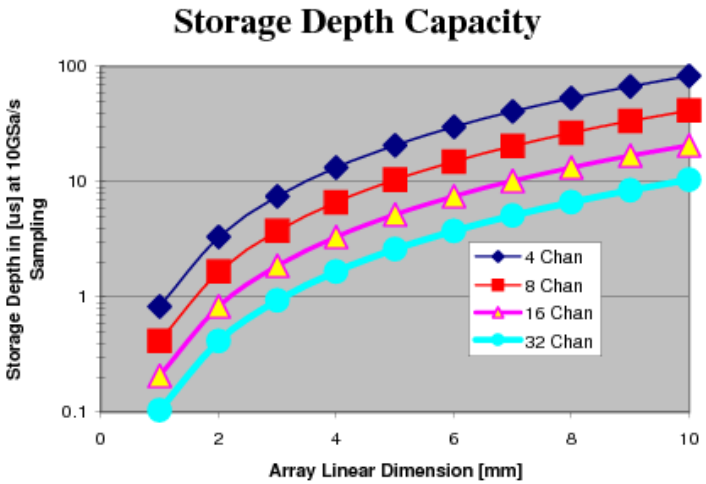


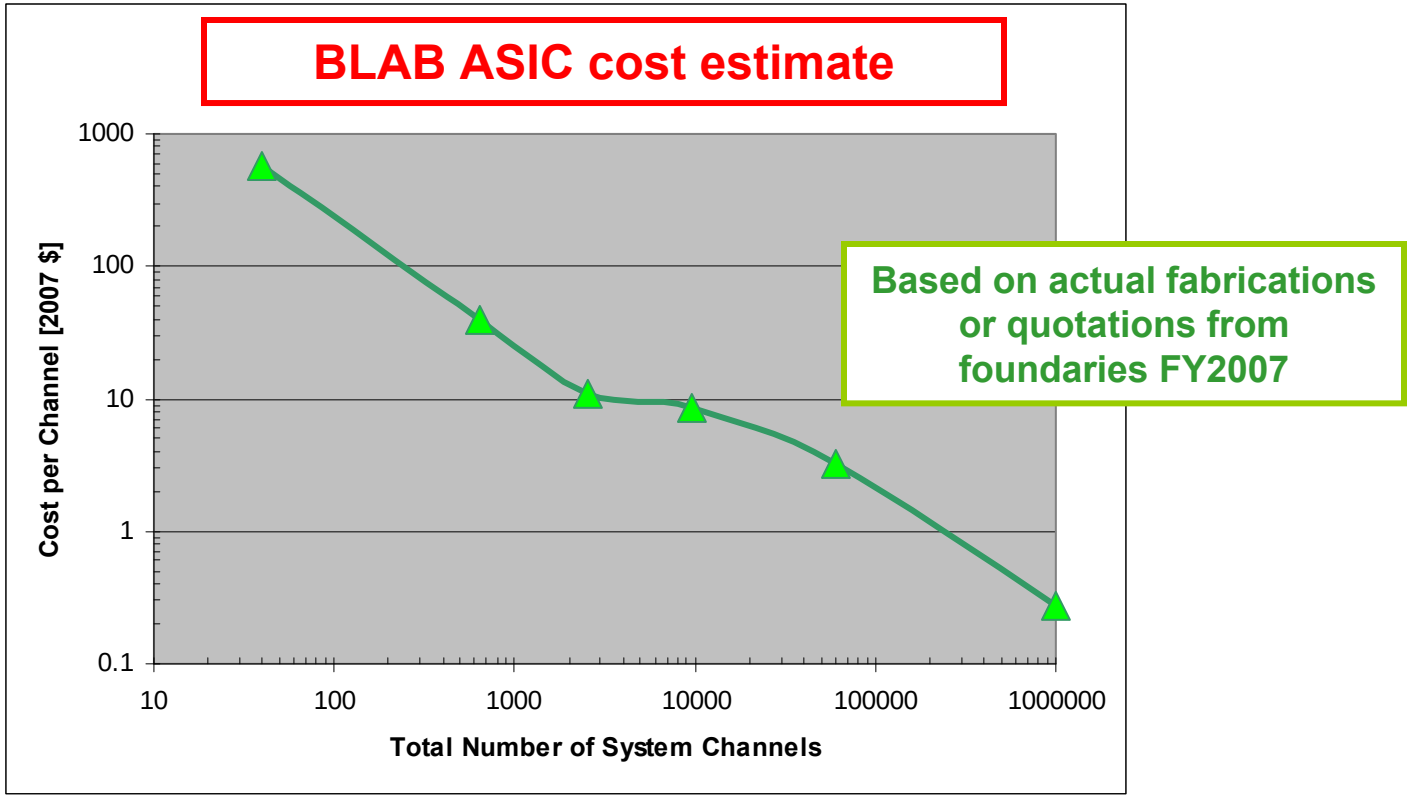
- 10 real bits of dynamic range, single-shot
- Target few $$/channel
- Low power

40

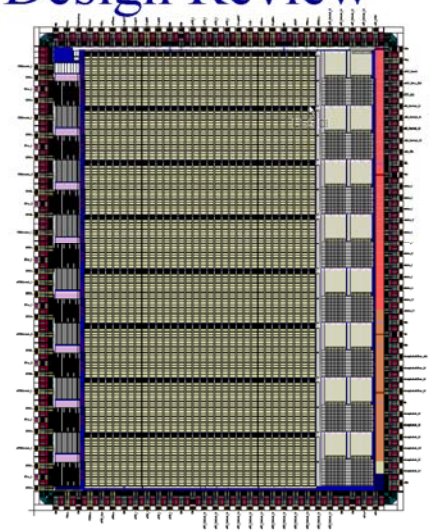
BLAB Density and Cost

- For large-scale systems, cost very competetive





Buffered LABRADOR (BLAB3) Design Review



Gary S. Varner 4 NOV 09

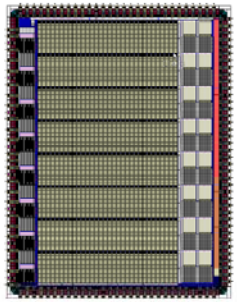
Review held with
University of Chicago engineers

All issues addressed – in fabrication

Due back 20-JAN-2010

Details:

Buffered LABRADOR v3 (BLAB3) ASIC



Design Reference Page

All information tentative and provided for informational reasons.

Note that the BLAB3 design has significant overlap with the IRS ASIC, and many details regarding the sampling, storage array performance simulations, and readout simulations were addressed previously and reviewed here.

A design Design Review is scheduled for Wednesday, Nov. 4th at 11:00 in the ID Lab.

Tentative MOSIS submission date: 26-OCT-09

Reference Documents:

- *Full set of BLAB3 schematics* 3-NOV-09 version [GSV]
- *Specification Review Slides* 21-SEP-09
- *Design Review Slides* -- 4-NOV-09

To be posted:

- Final schematics

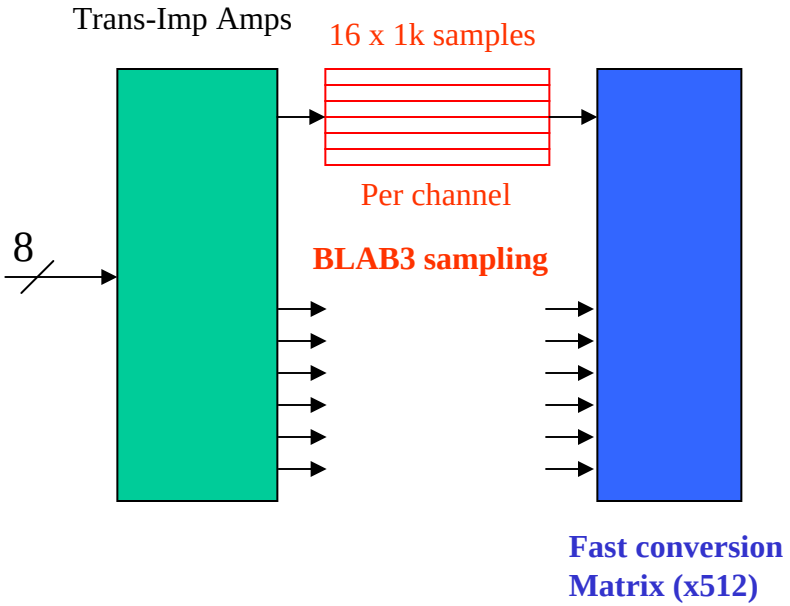
Review team:

- Jean-Francois Genat, Herve Grabas, Eric Oberla -- psTDC basis comparison
- Larry Ruckman -- logic interface and overall functionality

http://www.phys.hawaii.edu/~varner/BLAB3_homepage.html

Hit Processing latency

BLAB3 ASIC



Improvements based upon
Lessons learned from BLAB2

Assume:

100kHz charged track hits on each bar

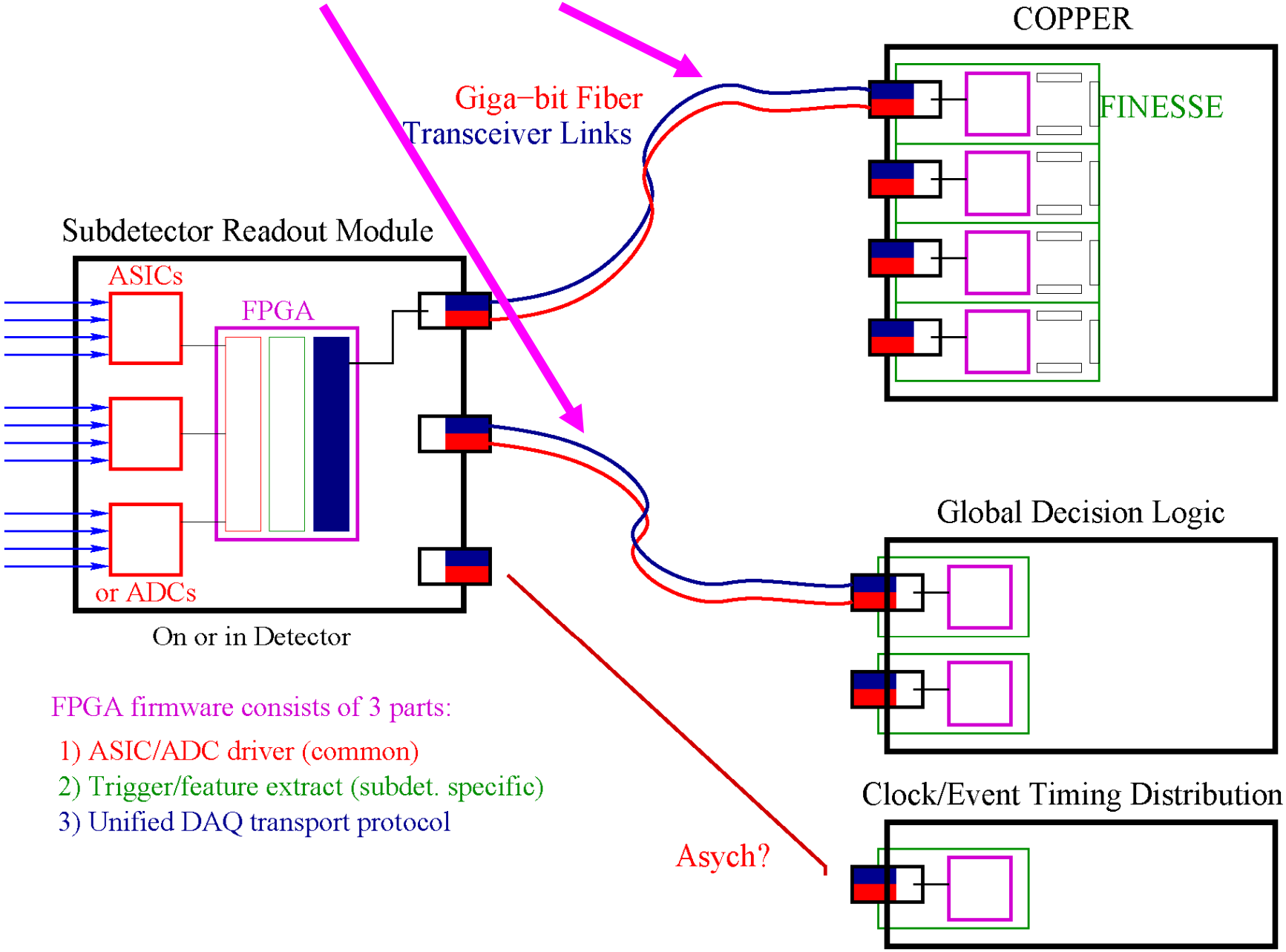
~32 p.e./track (1% of 100ns windows)
30kHz trigger rate
Each PMT pair sees <8> hits
240k hits/s
Each BLAB3 has an average occupancy
<1 hit (assume 1)
800ns to convert 512 samples
16ns/sample to transfer
At least 16 deep buffering
(Markov overflow probability
est. < 10^{-38})

Each hit = 64samples * 8bits = 512bits
➔~125Mbits/s
(link is 1.2Gb/s ~ x10 margin)

Plan to model in standard queuing simulator, but looks like no problem

Goals: prove system timing, full “at speed” T,Q extraction

Links are a crucial element

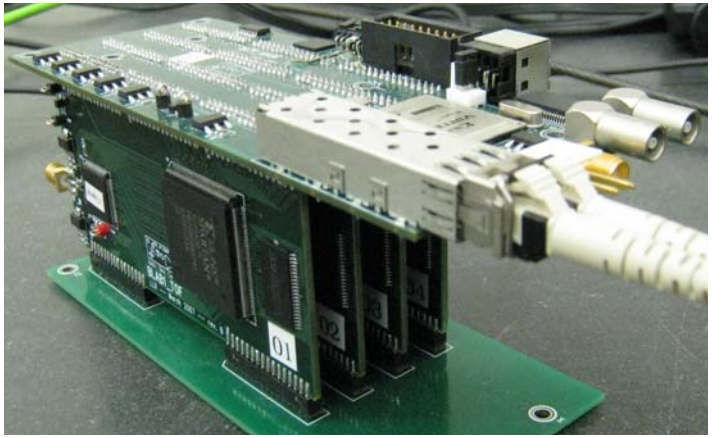


FPGA firmware consists of 3 parts:

1) ASIC/ADC driver (common)
2) Trigger/feature extract (subdet. specific)
3) Unified DAQ transport protocol

Continued Rad hard testing

Significant cost and performance benefit if can use commercially available components. One option is to qualify them.



~25 m
Fiber link

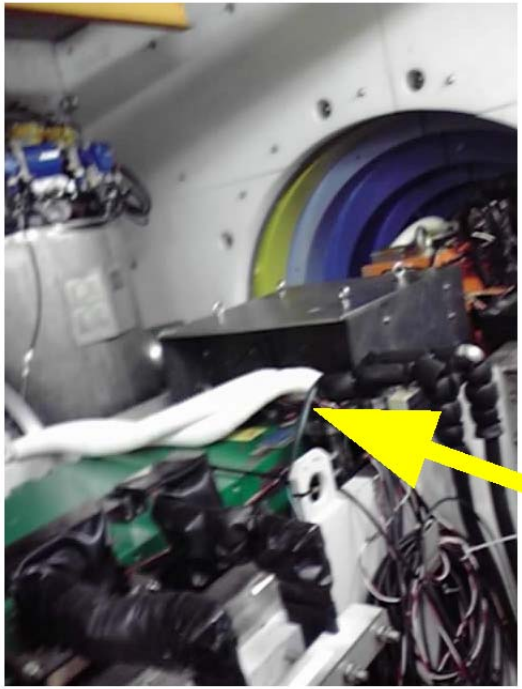
In tunnel
(rad area simulating expected CDC/PID dose)

Spring run
→ ~11kRad
→ 1 soft Reg error
→ no RAM bit errors

Monitor continuously BER remotely (loopback of pseudo-random pattern)

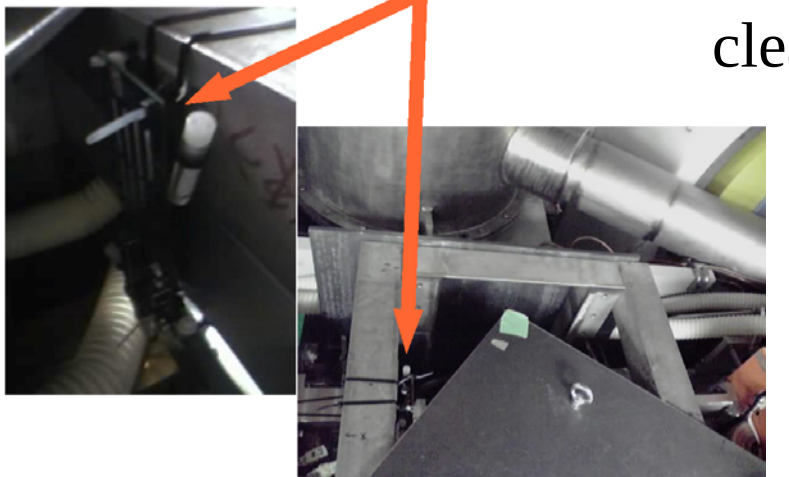
フラナガン@KCG
2009.10.9

Autumn Test Location



- BelleのVarner氏が作ったBelle II 放射線テスト用のボード。春にイオンチェンバーに付いていたが、現在QC2RPの上流側の鉛箱に入っています。
- 秋の運転終了までIR付近で作業する場合は光ファイバーに気を付けてください。

RADTEST board

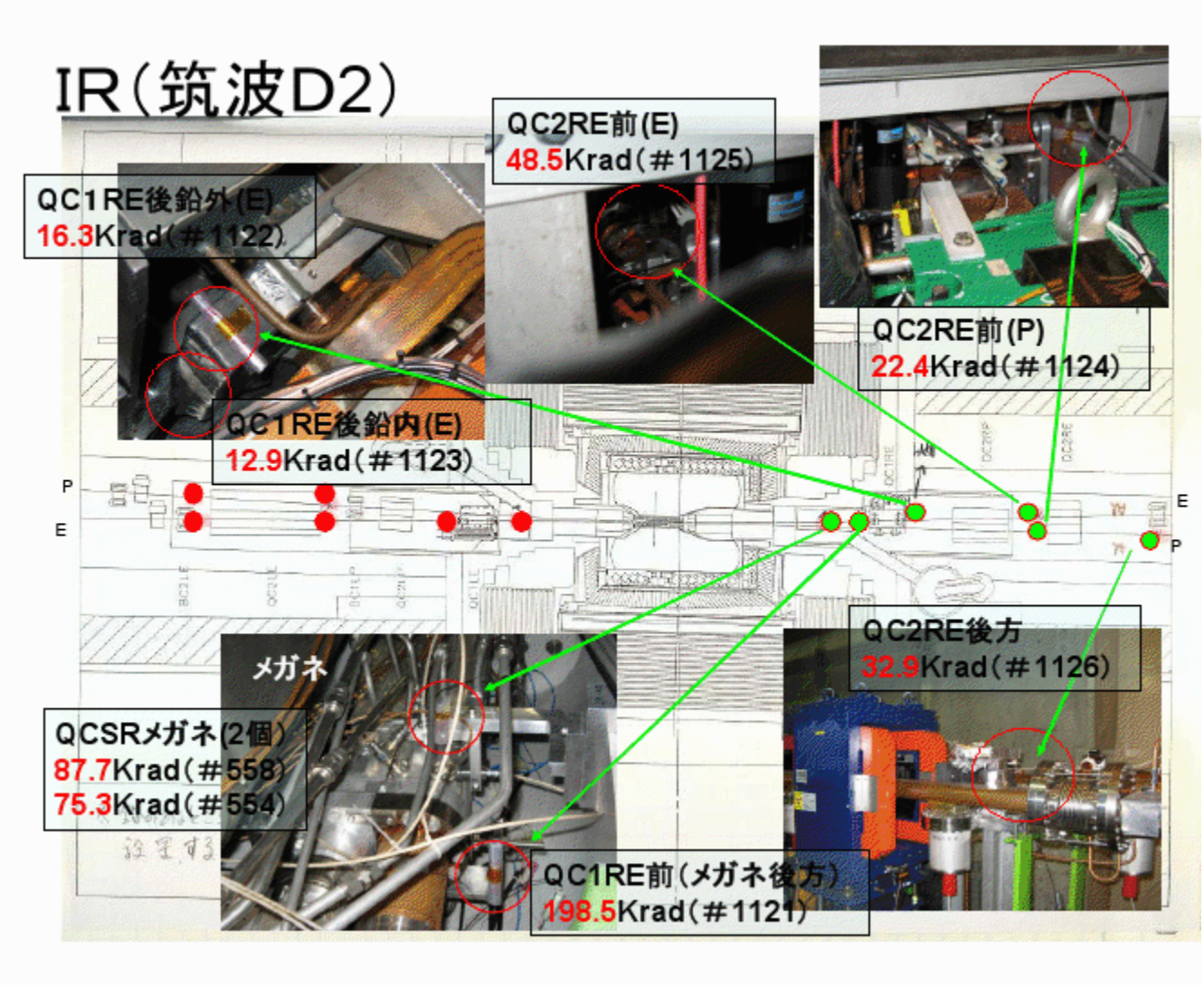


- much higher rate
- 4x RAM bit errors
- 5x 8/16 Reg bit persistent errors
- 1x data link hang
- Power cycle clear

Fiber link still runs Through existing Cable tray infrastructure and to loss monitor rack in room below

Update

Operation continued until almost end of fall run
Dec. 14 reprogram (to clear reg error)



2 aminograys located nearest to test module:
86kRad
48kRad
Average:
68kRad

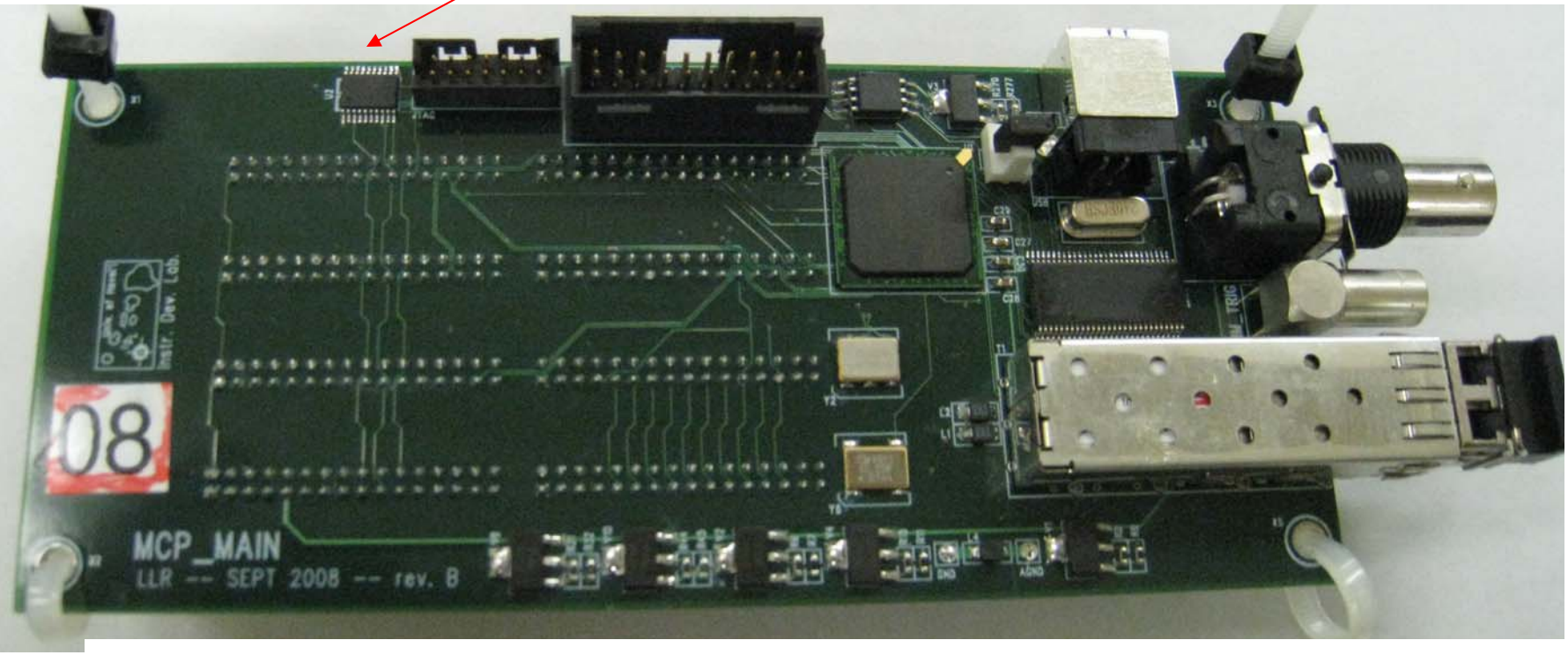
(minus 5-10%)

Problem debug

Board sent back

Vreg OK, initial EEPROM verify OK, but failed when try to clear or reprogram -- replaced and link works fine

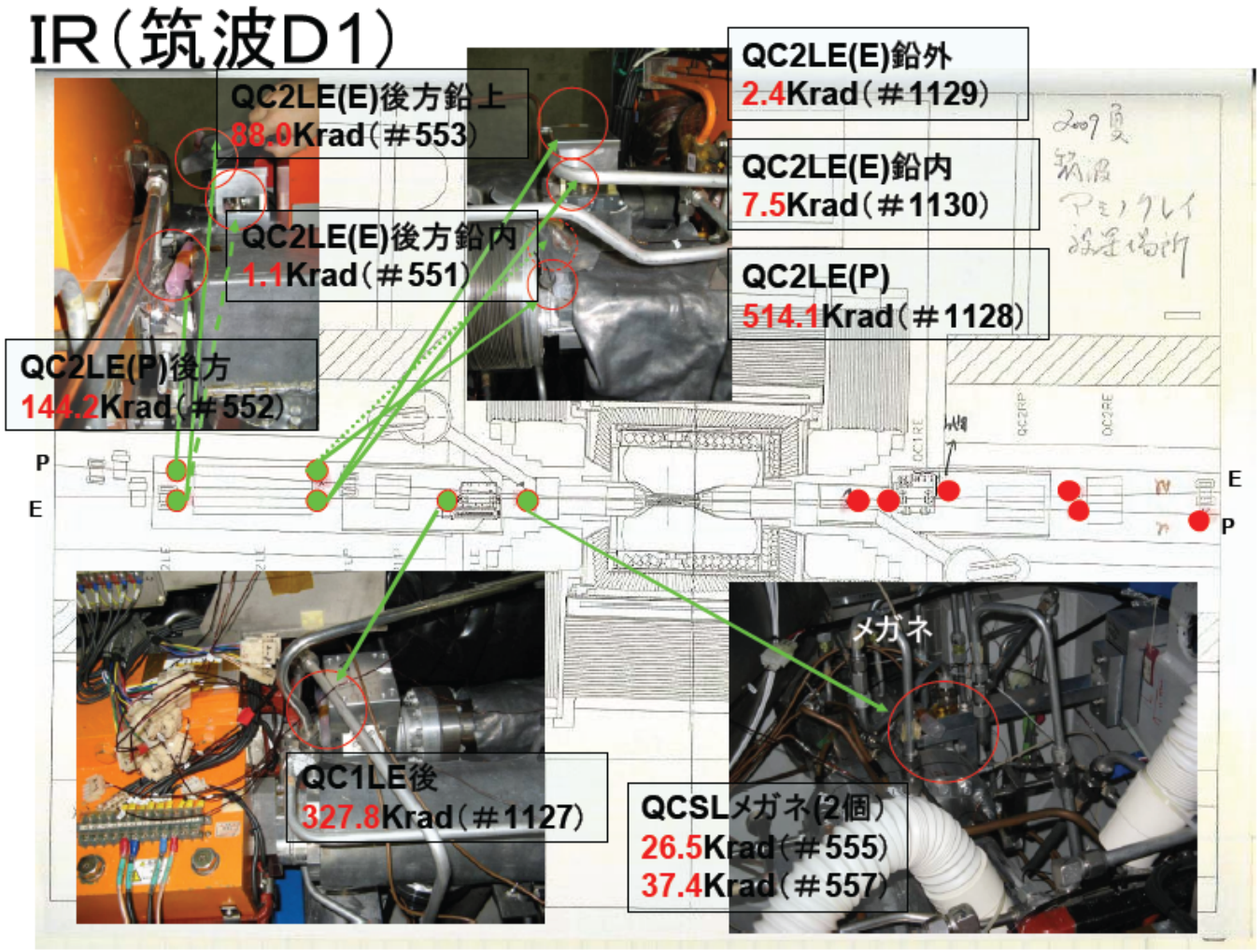
Not needed for final system



Continue the abuse in the Spring? (from ~70kRad dose)

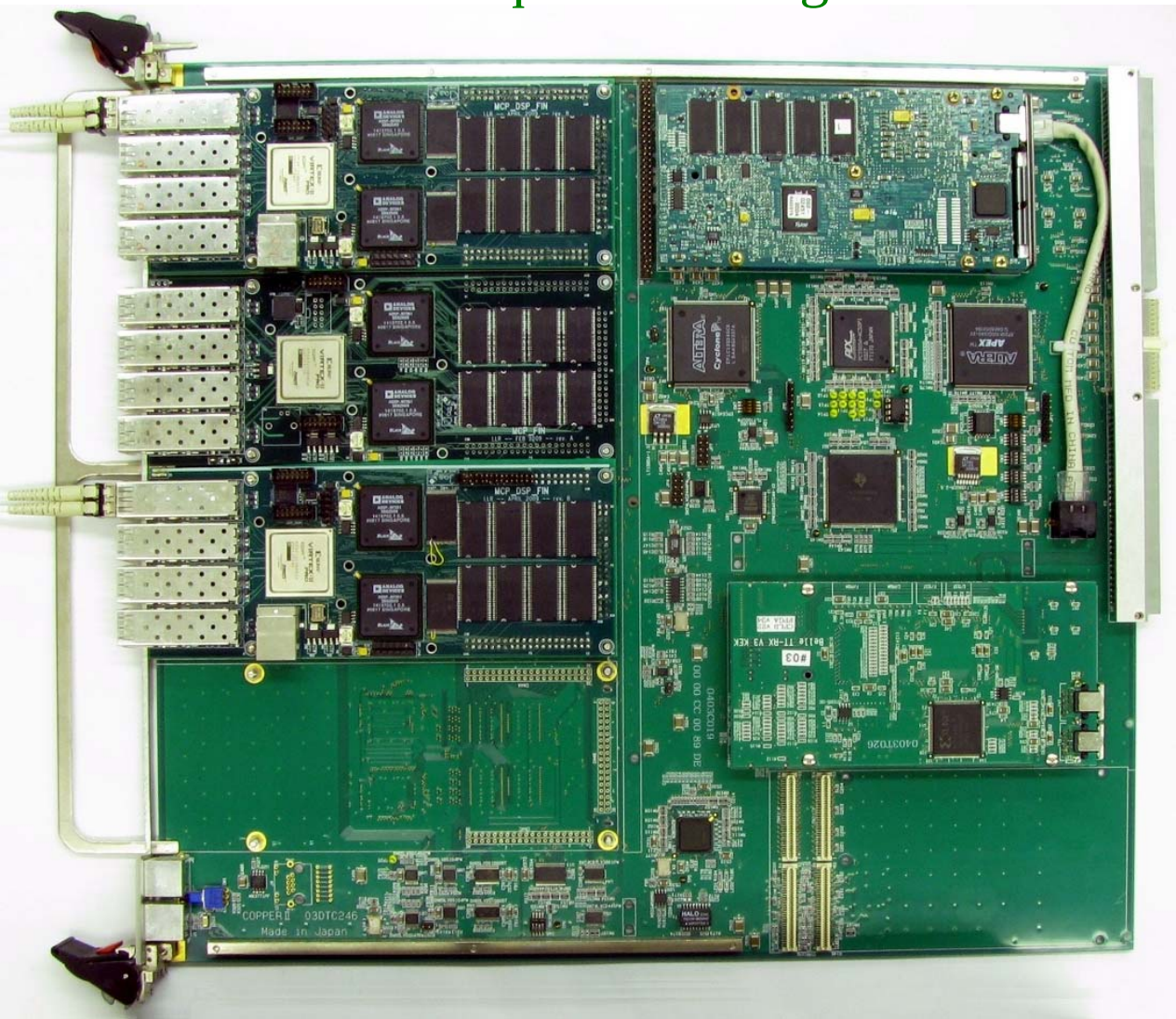
Next run – hotter spot?

Use production boards – including BLAB3 ASICs



With 100m cables, can reach

xTOP: DSP_FIN / COPPER

- each COPPER module can handle 1024 PMT channels (with 4 DSP_FIN boards per COPPER)
- need just 8 COPPER modules to do all SL-10 xTOP waveform processing in real time (8192 PMT channels)

Continuing studies of optimal signal extraction – requires real signals