

Waveform analysis vs analog techniques

- **Waveform sampling records all the information from the detector pulse** provided:

Sufficient sampling frequency ($> 2 \times$ upper limit of the signal's spectrum)

Sufficient ADC resolution (8-bit ok in most cases)

- **Timing resolution** depends mainly upon **signal slope** and **signal to noise**

- **Waveform sampling followed by Constant Fraction algorithm optimum:**

See:

Baptiste Joly: Ph.D dissertation and publication (Fast timing for in-beam PET)

<https://edms.in2p3.fr/document/I-019613/1>

<http://hal.in2p3.fr/docs/00/33/95/73/PDF/Dresden.pdf>

- **Sampling ASICs reach a few picosecond timing resolution:**

Stefan Ritt:

<http://clrwww.in2p3.fr/www2008/WTDMPPA/Session%202/Ritt%20Picosecond%20Clermont%202010.pdf>

Gary Varner:

http://arxiv.org/PS_cache/arxiv/pdf/0805/0805.2225v1.pdf

130nm CMOS sampling ASIC

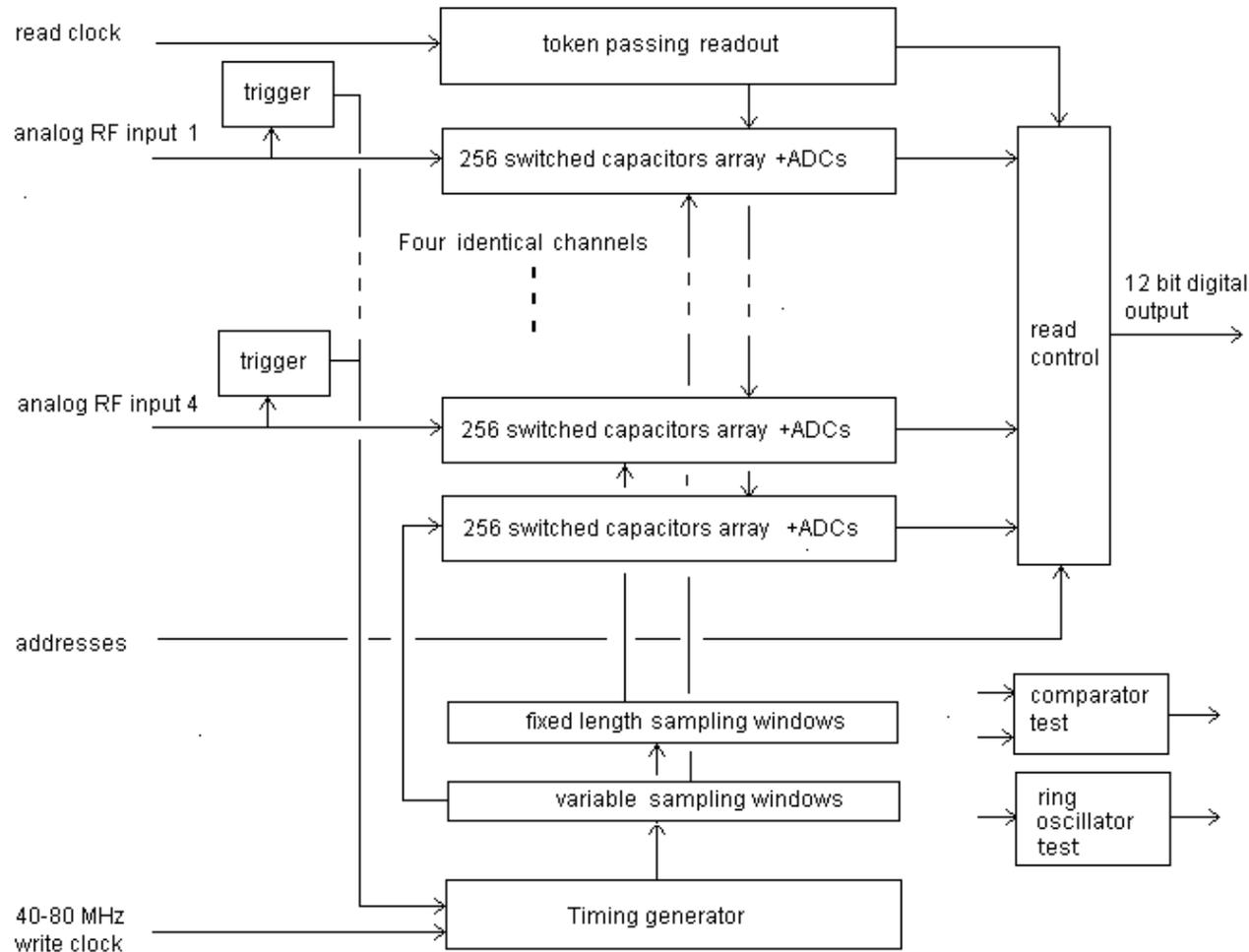
- First version tested: chip not functional, but most of the test structures ok.
 - Lack of internal buffering
 - Resistors missing (still not understood)
 - Too strong protections on pads

See Herve Grabas talk

- Second version launched last week with:
 - Input triggering discriminators,
 - Fixed and variable length sampling window,
 - Buffers wherever needed, no resistors.
 - Pads protections from the library

See Herve Grabas talk

130nm CMOS sampling ASIC version 2



MCP readout

- Chicago's ASIC back from foundry in May
- Impedance control: match 50 Ohms up to the sampling ASIC
Signal integrity, time and space resolution
- Clock jitter cleaner chip
Sampling jitter cannot be recovered by calibration
- Clock phase adjustment
There is no clock phase lock in the sampling ASIC
- FPGA for control and on-detector pre-processing
- Optical interfaces
Reduced digital to analog crosstalk, improved throughput
- Bump bonding
Bandwidth, room, power

First order sketch

(see Herve's presentation)



On PCB:

Sampling ASICs (bump bonded)

FPGA (bump bonded)

Opto: Clock in, Trigger in, Data out

Clock chip (phase, jitter)

Power: Voltage regulators, High voltage

Power planes