

## SUMMARY OF THE ELECTRONICS AND INTEGRATION GODPARENT REVIEW 2/25/2010

*Committee Members: Zikri Yusof (Chair – ANL), Bernhard Adams (ANL), Marcel Demarteau (Fermilab), Gary Drake (ANL), Ted Liu (Fermilab), Igor Veryovkin (ANL), Steve Ross (ANL).*

The review was held on Feb. 25, 2010 in Bldg. 362, Argonne National Laboratory. The following are a few recommendations and concerns made by the committee following the review:

1. There needs to be a better input protection to the chip.
2. Emphasis was placed on the importance of simulations. While the committee empathized with the possibility that it may take a rather long time to execute a rather complex simulation, access to better/more powerful computing resources such as a high-end workstation might address this issue. A full understanding of “features” of the chip was considered a worthwhile investment.
3. Clock distribution in-phase for one device. Furthermore, a clock tree appears to be necessary.
4. Better modeling of the leakage current, or better calibration.
5. Decide if FPGA will go on the PCB bottom.
6. Be really careful on how 'eager' the trigger/threshold is on the self-trigger circuit.
7. Should decide sooner rather than later on a date to be chosen on the final architecture of the chip (see also bullet 12)
8. Should start a clear plan on how to characterize the actual device when it is ready. Is there a time line on testing the full device?
9. What essential equipment is needed to test the chip? What are the tests? What needs to be purchased?
10. Have any considerations been made on testing the stripline without the chip?
11. There should be some urgency on coming up with the specifications for the Version 3 of the chip. It need not have everything.
12. Some consideration should be given to the possibility that future funding may be reduced (thus, the necessity in deciding on the architecture and other important issues), considering that other parts of the collaboration will go online and may demand greater

resources and funding. The electronics and integration effort is well positioned to deal with this since the work done is considerably further ahead than other parts of the collaboration.